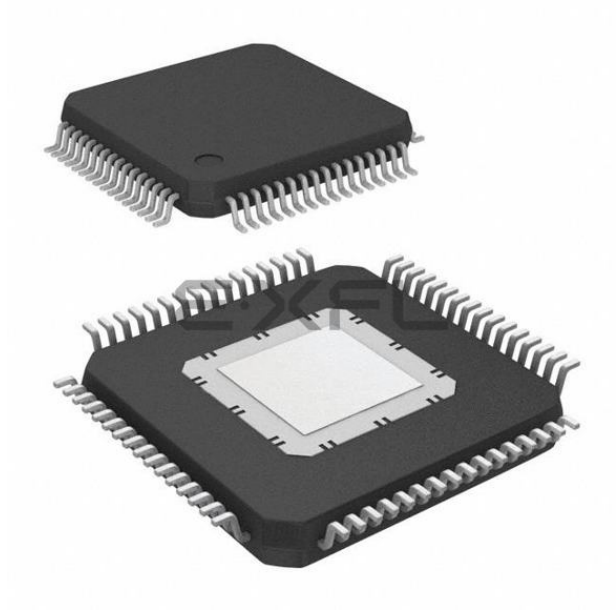

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Connectivity	CANbus, SCI, SPI
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Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
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Chapter 3
Memory Mapping Control (S12ZMMCV1)

Chapter 4
Interrupt (S12ZINTV0)

Table 1-9. Pin Summary For 80-Pin Package Option (ZVMC256 Only) (Sheet 3 of 5)

Pin #	Pin Name	Function (Priority and routing options defined in PIM chapter)							Supply	Internal Pull Resistor	
		1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.		CTRL	Reset State
28	VDDA	VRH0_0	VRH1_0	—	—	—	—		V_{DDA}	—	—
29	VSSA	VRL0_ [1:0]	VRL1_ [1:0]	—	—	—	—	—	V_{DDA}	—	—
30	PAD9	KWAD9	AN1_4	—	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
31	PAD10	KWAD10	AN1_5	—	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
32	PAD11	KWAD11	AN1_6	—	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
33	PAD12	KWAD12	AN1_7	—	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
34	PAD13	KWAD13	AN0_5	PTURE	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
35	PAD14	KWAD14	AN0_6	PDO	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
36	PAD15	KWAD15	AN0_7	PDOCLK	—	—	—	—	V_{DDA}	PERADH/PPSADH	Off
37	BCTLC	—	—	—	—	—	—	—	V_{DDC}	—	—
38	VDDC	—	—	—	—	—	—	—	V_{DDC}	—	—
39	CANH0	—	—	—	—	—	—	—	V_{DDC}	—	—
40	VSSC	—	—	—	—	—	—	—	V_{DDC}	—	—
41	CANL0	—	—	—	—	—	—	—	V_{DDC}	—	—
42	SPLIT0	—	—	—	—	—	—	—	V_{DDC}	—	—
43	LS0	—	—	—	—	—	—	—	—	—	—
44	LG0	—	—	—	—	—	—	—	—	—	—
45	VLS0	—	—	—	—	—	—	—	—	—	—
46	VBS0	—	—	—	—	—	—	—	—	—	—
47	HG0	—	—	—	—	—	—	—	—	—	—

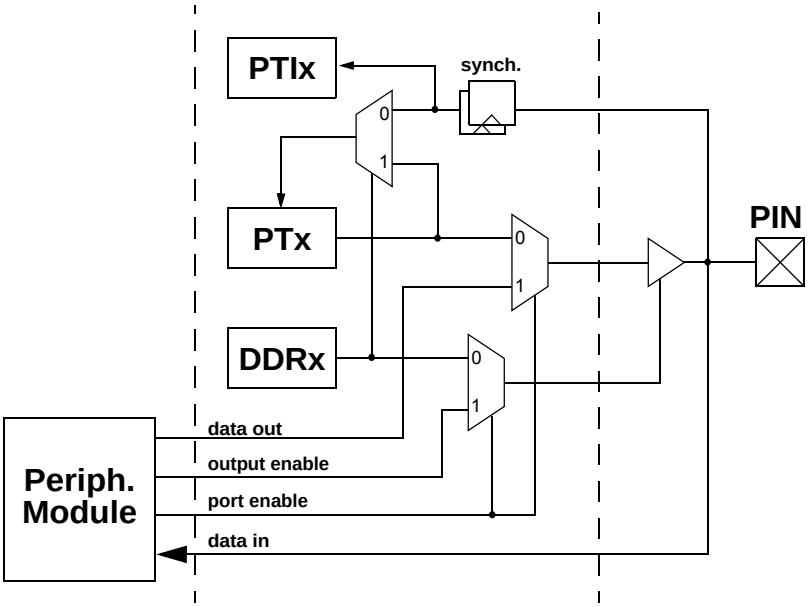

Figure 2-35. Illustration of I/O pin functionality

This section describes the interrupts generated by the PIM and their individual sources. Vector addresses and interrupt priorities are defined at MCU level.

Table 2-41. PIM Interrupt Sources

Module Interrupt Sources	Local Enable
$\overline{\text{XIRQ}}$	None
$\overline{\text{IRQ}}$	IRQCR[IRQEN]
Port AD pin interrupt	PIEADH[PIEADH7-PIEADH0] PIEADL[PIEADL7-PIEADL0]
Port S pin interrupt	PIES[PIES5-PIES0]
Port P pin interrupt	PIEP[PIEP2-PIEP0]
Port L pin interrupt	PIEL[PIEL0]
PP0 over-current interrupt	PIEP[OCIE1]

2.4.3.1 XIRQ, IRQ Interrupts

The $\overline{\text{XIRQ}}$ pin allows requesting non-maskable interrupts after reset initialization. During reset, the X bit in the condition code register is set and any interrupts are masked until software enables them.

The $\overline{\text{IRQ}}$ pin allows requesting asynchronous interrupts. The interrupt input is disabled out of reset. To enable the interrupt the IRQCR[IRQEN] bit must be set and the I bit cleared in the condition code register. The interrupt can be configured for level-sensitive or falling-edge-sensitive triggering. If IRQCR[IRQEN] is cleared while an interrupt is pending, the request will deassert.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x010C-0x010F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0110	DBGACTL	R	0	NDB	INST	0	RW	RWE	reserved	COMPE
		W								
0x0111-0x0114	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0115	DBGAAH	R	DBGAA[23:16]							
		W								
0x0116	DBGAAM	R	DBGAA[15:8]							
		W								
0x0117	DBGAAL	R	DBGAA[7:0]							
		W								
0x0118	DBGAD0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x0119	DBGAD1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x011A	DBGAD2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x011B	DBGAD3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x011C	DBGADM0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x011D	DBGADM1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x011E	DBGADM2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x011F	DBGADM3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0120	DBGBCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0121-0x0124	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0125	DBGBAH	R	DBGBA[23:16]							
		W								
0x0126	DBGBAM	R	DBGBA[15:8]							
		W								
0x0127	DBGBAL	R	DBGBA[7:0]							
		W								

Figure 6-2. Quick Reference to DBG Registers

7.2.2.7 ECC Debug Command (ECCDCMD)

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime, in special mode only

Figure 7-8. ECC Debug Command (ECCDCMD)

Table 7-8. ECCDCMD Field Description

Field	Description
7 ECCDRR	ECC Disable Read Repair Function— Writing one to this register bit will disable the automatic single bit ECC error repair function during read access; see also chapter 7.3.7, “ECC Debug Behavior”. 0 Automatic single ECC error repair function is enabled 1 Automatic single ECC error repair function is disabled
1 ECCDW	ECC Debug Write Command — Writing one to this register bit will perform a debug write access, to the system memory. During this access the debug data word (DDATA) and the debug ECC value (DECC) will be written to the system memory address defined by DPTR. If the debug write access is done, this bit is cleared. Writing 0 has no effect. It is not possible to set this bit if the previous debug access is ongoing (ECCDW or ECCDR bit set).
0 ECCDR	ECC Debug Read Command — Writing one to this register bit will perform a debug read access from the system memory address defined by DPTR. If the debug read access is done, this bit is cleared and the raw memory read data are available in register DDATA and the raw ECC value is available in register DECC. Writing 0 has no effect. If the ECCDW and ECCDR bit are set at the same time, then only the ECCDW bit is set and the Debug Write Command is performed. It is not possible to set this bit if the previous debug access is ongoing (ECCDW or ECCDR bit set).

7.3 Functional Description

The bus system allows 1, 2, 3 and 4 byte write access to a 4 byte aligned memory address, but the ECC value is generated based on an aligned 2 byte data word. Depending on the access type, the access is separated into different access cycles. Table 7-9 shows the different access types with the expected number of access cycles and the performed internal operations.

Table 7-9. Memory access cycles

Access type	ECC error	access cycle	Internal operation	Memory content	Error indication
2 and 4 byte aligned write access	—	1	write to memory	new data	—

If XOSCLCP is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If XOSCLCP is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

The REFFRQ[1:0] bits are used to configure the internal PLL filter for optimal stability and lock time. For correct PLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Table 8-4.

If IRC1M is selected as REFCLK (OSCE=0) the PLL filter is fixed configured for the 1MHz <= f_{REF} <= 2MHz range. The bits can still be written but will have no effect on the PLL filter configuration.

For OSCE=1, setting the REFFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

Table 8-4. Reference Clock Frequency Selection if OSC_LCP is enabled

REFCLK Frequency Ranges (OSCE=1)	REFFRQ[1:0]
1MHz <= f_{REF} <= 2MHz	00
2MHz < f_{REF} <= 6MHz	01
6MHz < f_{REF} <= 12MHz	10
f_{REF} >12MHz	11

Table 8-33. CPMUVDDS Field Descriptions (continued)

Field	Description
3 SCS2IF	**Short circuit VDDS2 Interrupt Flag** — SCS2IF is set to 1 when SCS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS2IF causes an interrupt request. 0 No change in SCS2 bit. 1 SCS2 bit has changed.
2 SCS1IF	**Short circuit VDDS1 Interrupt Flag** — SCS1IF is set to 1 when SCS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS1IF causes an interrupt request. 0 No change in SCS1 bit. 1 SCS1 bit has changed.
1 LVS2IF	**Low-Voltage VDDS2 Interrupt Flag** — LVS2IF is set to 1 when LVDS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS2IF causes an interrupt request. 0 No change in LVDS2 bit. 1 LVDS2 bit has changed.
0 LVS1IF	**Low-Voltage VDDS1 Interrupt Flag** — LVS1IF is set to 1 when LVDS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS1IF causes an interrupt request. 0 No change in LVDS1 bit. 1 LVDS1 bit has changed.

9.5.2.4 ADC Timing Register (ADCTIM)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	PRS[6:0]						
W								
Reset	0	0	0	0	0	1	0	1

= Unimplemented or Reserved

Figure 9-7. ADC Timing Register (ADCTIM))

Read: Anytime

Write: These bits are writable if bit ADC_EN is clear or bit SMOD_ACC is set

Table 9-7. ADCTIM Field Descriptions

Field	Description
6-0 PRS[6:0]	**ADC Clock Prescaler** — These 7bits are the binary prescaler value PRS. The ADC conversion clock frequency is calculated as follows: $f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK}.

Table 9-21. Conversion Command Type Select

CMD_SEL[1]	CMD_SEL[0]	Conversion Command Type Description
1	0	End Of List (Automatic wrap to top of CSL and Continue Conversion)
1	1	End Of List (Wrap to top of CSL and: - In “Restart Mode” wait for Restart Event followed by a Trigger - In “Trigger Mode” wait for Trigger or Restart Event)

11.3.2.13 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 11-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 11-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	Output Compare Pin Disconnect Bits 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

11.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 11-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

Setting OCPDx to zero allows the internal register to drive the programmed state to OCx. This allows a glitch free switch over of port from general purpose I/O to timer output once the OCPDx bit is set to zero.

11.5 Resets

The reset state of each individual bit is listed within Section 11.3, “Memory Map and Register Definition” which details the registers and their bit fields

11.6 Interrupts

This section describes interrupts originated by the TIM16B4CV3 block. Table 11-18 lists the interrupts generated by the TIM16B4CV3 to communicate with the MCU.

Table 11-18. TIM16B4CV3 **Interrupts**

Interrupt	Offset	Vector	Priority	Source	Description
C[3:0]F	—	—	—	Timer Channel 3–0	Active high timer channel interrupts 3–0
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

The TIM16B4CV3 could use up to 5 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

11.6.1 Channel [3:0] Interrupt (C[3:0]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 0 interrupt. The TIM block only generates the interrupt and does not service it. Only bits related to implemented channels are valid.

11.6.2 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt. The TIM block only generates the interrupt and does not service it.

15.4 Functional Description

15.4.1 Block Diagram

A block diagram of the PMF is shown in Figure 15-1**.** The MTG bit allows the use of multiple PWM generators (A, B, and C) or just a single generator (A). PWM0 and PWM1 constitute Pair A, PWM2 and PWM3 constitute Pair B, and PWM4 and PWM5 constitute Pair C.

Figure 15-41 depicts Pair A signal paths of PWM0 and PWM1. Pairs B and C have the same structure.

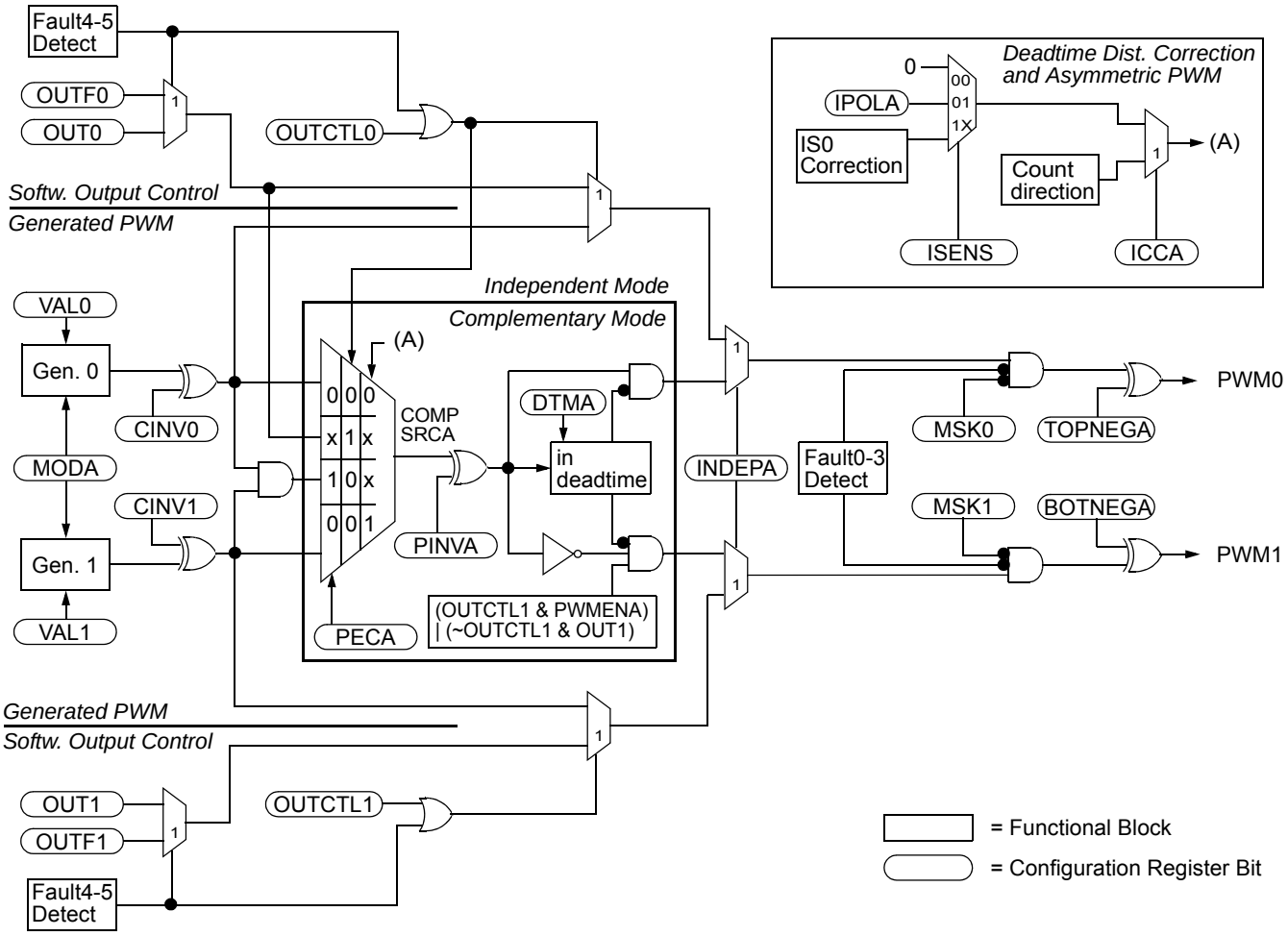

Figure 15-41. Detail of PWM0 and PWM1 Signal Paths

NOTE

It is possible to have both channels of a complementary pair to be high. For example, if the TOPNEGA (negative polarity for PWM0), BOTNEGA (negative polarity for PWM1), MSK0 and MSK1 bits are set, both the PWM complementary outputs of generator A will be high. See Section 15.3.2.2, “PMF Configure 1 Register (PMFCFG1)” for the description of TOPNEG and BOTNEG bits, and Section 15.3.2.3, “PMF Configure 2 Register (PMFCFG2)” for the description of the MSK0 and MSK1 bits.

16.5.3.1 Description of Interrupt Operation

The SCI only originates interrupt requests. The following is a description of how the SCI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent. The SCI only has a single interrupt line (SCI Interrupt Signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

16.5.3.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission.Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

16.5.3.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed. Transmission is completed when all bits including the stop bit (if transmitted) have been shifted out and no data is queued to be transmitted. No stop bit is transmitted when sending a break character and the TC flag is set (providing there is no more data queued for transmission) when the break character has been shifted out. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL).TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

16.5.3.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

16.5.3.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

16.5.3.1.5 IDLE Description

The IDLE interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. Once the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register will continue to operate, the rest of the SPI is shut down (i.e., a SPIF interrupt will **not** be generated until exiting stop or wait mode). Also, the byte from the shift register will not be copied into the SPIDR register until after the slave SPI has exited wait or stop mode. In slave mode, a received byte pending in the receive shift register will be lost when entering wait or stop mode. An SPIF flag and SPIDR copy is generated only if wait mode is entered or exited during a tranmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy will occur.

17.4.7.3 SPI in Stop Mode

Stop mode is dependent on the system. The SPI enters stop mode when the module clock is disabled (held high or low). If the SPI is in master mode and exchanging data when the CPU enters stop mode, the transmission is frozen until the CPU exits stop mode. After stop, data to and from the external SPI is exchanged correctly. In slave mode, the SPI will stay synchronized with the master.

The stop mode is not dependent on the SPISWAI bit.

17.4.7.4 Reset

The reset values of registers and signals are described in Section 17.3, “Memory Map and Register Definition”, which details the registers and their bit fields.

- If a data transmission occurs in slave mode after reset without a write to SPIDR, it will transmit garbage, or the data last received from the master before the reset.
- Reading from the SPIDR after reset will always read zeros.

17.4.7.5 Interrupts

The SPI only originates interrupt requests when SPI is enabled (SPE bit in SPICR1 set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

The interrupt flags MODF, SPIF, and SPTEF are logically ORed to generate an interrupt request.

17.4.7.5.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see Table 17-3). After MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR = 0, The master bit in SPICR1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 17.3.2.4, “SPI Status Register (SPISR)”.

18.3.2.16 GDU Overcurrent Register 1 (GDUOC1)

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GOCA1	GOCE1	0	GOCT1[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-18. GDU Overcurrent Register 1 (GDUOC1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-20. GDUOC1 Register Field Descriptions

Field	Description
7 GOCA1	GDU Overcurrent Action — This bit cannot be modified after GWP bit is set. This bit controls the action in case of an overcurrent event or overvoltage event. See Table 18-24 and Table 18-23
6 GOCE1	GDU Overcurrent Enable — This bit cannot be modified after GWP bit is set. 0 Overcurrent Comparator 1 is disabled 1 Overcurrent Comparator 1 is enabled
GDUV4 (includes GOCT1 bits 3:0)	
3:0 GOCT1[3:0]	GDU Overcurrent Comparator Threshold — These bits cannot be modified after GWP bit is set. The overcurrent comparator threshold voltage is the output of a 6-bit digital-to-analog converter. The upper two bits of the digital inputs are tied to one. The other bits of the digital inputs are driven by GOCT1. The overcurrent comparator threshold voltage can be calculated from equation below. $$Voct1 = (48 + GOCT1) \cdot \frac{VDDA}{64}$$
GDUV5 and V6 (includes GOCT1 bits 4:0)	
4:0 GOCT1[4:0]	GDU Overcurrent Comparator Threshold — These bits cannot be modified after GWP bit is set. The overcurrent comparator threshold voltage is the output of a 6-bit digital-to-analog converter. The upper bit of the digital inputs is tied to one. The other bits of the digital inputs are driven by GOCT1. The overcurrent comparator threshold voltage can be calculated from equation below. $$Voct1 = (32 + GOCT1) \cdot \frac{VDDA}{64}$$

Address & Name		7	6	5	4	3	2	1	0
0x0011 FCCOB2LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0012 FCCOB3HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x0013 FCCOB3LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0014 FCCOB4HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x0015 FCCOB4LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0016 FCCOB5HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x0017 FCCOB5LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								

= Unimplemented or Reserved

Figure 20-4. FTMRZ128K512 Register Summary (continued)

1. Number of implemented DPS bits depends on EEPROM memory size.

20.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Offset Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	FDIVLD	FDIVLCK	FDIV[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-5. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bit 7 is not writable, bit 6 is write-once-hi and controls the writability of the FDIV field in normal mode. In special mode, bits 6-0 are writable any number of times but bit 7 remains unwritable.

(protection enabled). If the DPOPEN bit is set, the state of the DPS bits is irrelevant. All DPOPEN/DPS bit registers are writable without restriction in Special Single Chip Mode.

During the reset sequence, fields DPOPEN and DPS of the DFPROT register are loaded with the contents of the EEPROM protection byte in the Flash configuration field at global address 0xFF_FE0D located in P-Flash memory (see Table 20-4) as indicated by reset condition F in Table 20-25. To change the EEPROM protection that will be loaded during the reset sequence, the P-Flash sector containing the EEPROM protection byte must be unprotected, then the EEPROM protection byte must be programmed. If a double bit fault is detected while reading the P-Flash phrase containing the EEPROM protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the EEPROM memory fully protected.

Trying to alter data in any protected area in the EEPROM memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the EEPROM memory is not possible if any of the EEPROM sectors are protected.

Table 20-24. DFPROT Field Descriptions

Field	Description
7 DPOPEN	EEPROM Protection Control 0 Enables EEPROM memory protection from program and erase with protected address range defined by DPS bits 1 Disables EEPROM memory protection from program and erase
6–0 DPS[6:0]	**EEPROM Protection Size** — The DPS bits determine the size of the protected area in the EEPROM memory as shown inTable 20-25 .

Table 20-25. EEPROM Protection Address Range

DPS[6:0]	Global Address Range	Protected Size
0000000	0x10_0000 – 0x10_001F	32 bytes
0000001	0x10_0000 – 0x10_003F	64 bytes
0000010	0x10_0000 – 0x10_005F	96 bytes
0000011	0x10_0000 – 0x10_007F	128 bytes
0000100	0x10_0000 – 0x10_009F	160 bytes
The Protection Size goes on enlarging in step of 32 bytes, for each DPS value increment . .		
0001111	0x10_0000 – 0x10_01FF	512 bytes
0011111	0x10_0000 – 0x10_03FF	1K byte
0111111	0x10_0000 – 0x10_07FF	2K bytes
1111111	0x10_0000 – 0x10_0FFF	4K bytes

20.4.7.17 Protection Override Command

The Protection Override command allows the user to temporarily override the protection limits, either decreasing, increasing or disabling protection limits, on P-Flash and/or EEPROM, if the comparison key provided as a parameter loaded on FCCOB matches the value of the key previously programmed on the Flash Configuration Field (see Table 20-4). The value of the Protection Override Comparison Key must not be 16'hFFFF, that is considered invalid and if used as argument will cause the Protection Override feature to be disabled. Any valid key value that does not match the value programmed in the Flash Configuration Field will cause the Protection Override feature to be disabled. Current status of the Protection Override feature can be observed on FPSTAT FPOVRD bit (see Section 20.3.2.4, "Flash Protection Status Register (FPSTAT)).

Table 20-68. Protection Override Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x13	Protection Update Selection [1:0] See Table 20-69
FCCOB1	Comparison Key	
FCCOB2	reserved	New FPROT value
FCCOB3	reserved	New DFPROT value

Table 20-69. Protection Override selection description

Protection Update Selection code [1:0]	Protection register selection
bit 0	Update P-Flash protection 0 - keep unchanged (do not update) 1 - update P-Flash protection with new FPROT value loaded on FCCOB
bit 1	Update EEPROM protection 0 - keep unchanged (do not update) 1 - update EEPROM protection with new DFPROT value loaded on FCCOB

If the comparison key successfully matches the key programmed in the Flash Configuration Field the Protection Override command will preserve the current values of registers FPROT and DFPROT stored in an internal area and will override these registers as selected by the Protection Update Selection field with the value(s) loaded on FCCOB parameters. The new values loaded into FPROT and/or DFPROT can reconfigure protection without any restriction (by increasing, decreasing or disabling protection limits). If the command executes successfully the FPSTAT FPOVRD bit will set.

If the comparison key does not match the key programmed in the Flash Configuration Field, or if the key loaded on FCCOB is 16'hFFFF, the value of registers FPROT and DFPROT will be restored to their original contents before executing the Protection Override command and the FPSTAT FPOVRD bit will be cleared. If the contents of the Protection Override Comparison Key in the Flash Configuration Field is left in the erased state (i.e. 16'hFFFF) the Protection Override feature is permanently disabled. If the command execution is flagged as an error (ACCERR being set for incorrect command launch) the values of FPROT and DFPROT will not be modified.

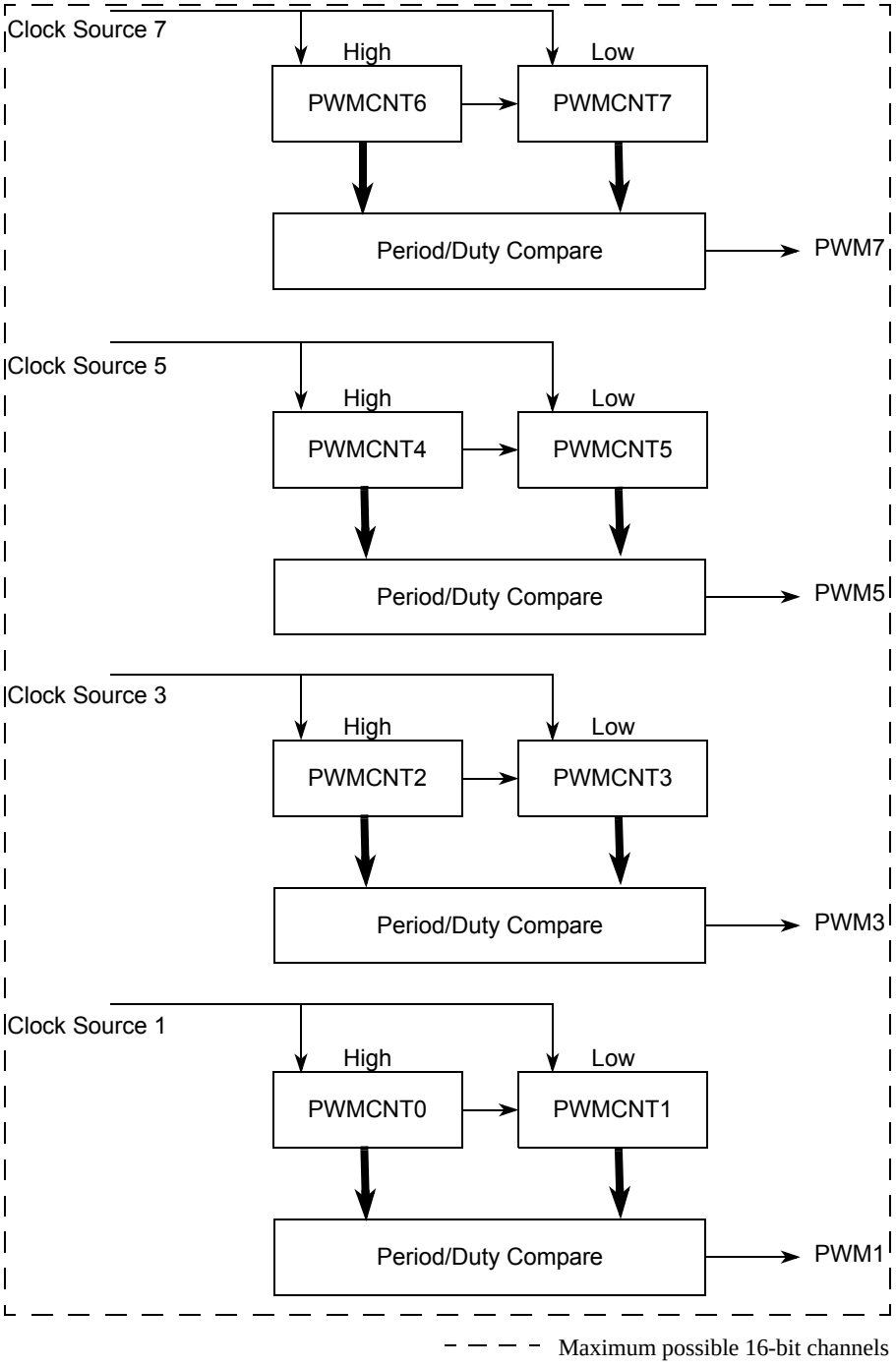

Figure 22-21. PWM 16-Bit Mode

Once concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low order PWMEx bit. In this case, the high order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

Table F-3. FTMRZ32K128 NVM Timing Characteristics (Junction Temperature From –40°C To +150°C)

Derivatives ZVML31, ZVM32, ZVM16									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	50	50	50	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	8992	t_{RD1ALL}	0.18	0.18	0.36	17.98	ms
4	Erase Verify Block (Pflash)	0	8750	t_{RD1BLK_P}	0.18	0.18	0.35	17.50	ms
5	Erase Verify Block (EEPROM)	0	631	t_{RD1BLK_D}	0.01	0.01	0.03	1.26	ms
6	Erase Verify P-Flash Section	0	511	t_{RD1SEC}	0.01	0.01	0.02	1.02	ms
7	Read Once	0	481	t_{RDONCE}	9.62	9.62	9.62	481.00	us
8	Program P-Flash (4 Word)	164	3136	t_{PGM_4}	0.22	0.23	0.41	12.75	ms
9	Program Once	164	3107	$t_{PGMONCE}$	0.22	0.23	0.23	3.31	ms
10	Erase All Blocks	100066	9455	t_{ERSALL}	95.49	100.26	100.44	143.99	ms
11	Erase Flash Block (Pflash)	100060	9119	t_{ERSBLK_P}	95.48	100.24	100.42	143.31	ms
12	Erase Flash Block (EEPROM)	100060	970	t_{ERSBLK_D}	95.31	100.08	100.10	127.02	ms
13	Erase P-Flash Sector	20015	927	t_{ERSPG}	19.08	20.03	20.05	26.87	ms
14	Unsecure Flash	100066	9533	t_{UNSECU}	95.49	100.26	100.45	144.15	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	9.86	9.86	9.86	493.00	us
16	Set User Margin Level	0	439	t_{MLOADU}	8.78	8.78	8.78	439.00	us
17	Set Factory Margin Level	0	448	t_{MLOADF}	8.96	8.96	8.96	448.00	us
18	Erase Verify EEPROM Sector	0	583	$t_{DRD1SEC}$	0.01	0.01	0.02	1.17	ms
19	Program EEPROM (1 Word)	68	1678	t_{DPGM_1}	0.10	0.10	0.20	6.80	ms
20	Program EEPROM (2 Word)	136	2702	t_{DPGM_2}	0.18	0.19	0.35	10.98	ms
21	Program EEPROM (3 Word)	204	3726	t_{DPGM_3}	0.27	0.28	0.50	15.16	ms
22	Program EEPROM (4 Word)	272	4750	t_{DPGM_4}	0.35	0.37	0.65	19.34	ms
23	Erase EEPROM Sector	5015	817	t_{DERSPG}	4.79	5.03	20.34	38.96	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	9.50	9.50	9.50	475.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging