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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP Exposed Pad
Supplier Device Package	80-TQFP-EP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc25f1mkk

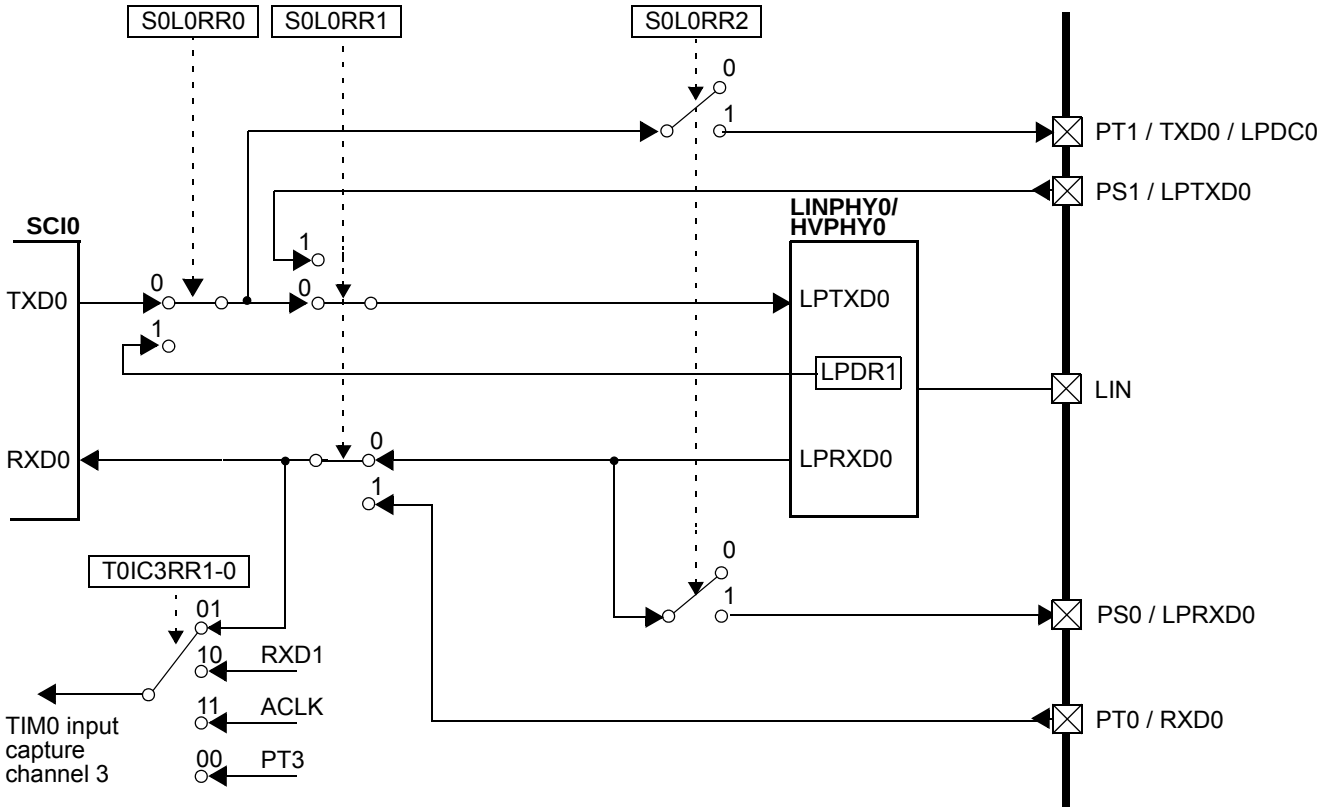

Figure 2-2. SCI0-to-LINPHY0 Routing Options Illustration

Table 2-10. Preferred Interface Configurations

S0L0RR[2:0]	Signal Routing	Description
000	TXD0 → LPTXD0 RXD0 ← LPRXD0	Default setting: SCI0 connects to LINPHY0/HVPHY0, interface internal only
001	LP0DR1 → LPTXD0 RXD0 ← LPRXD0	Direct control setting: LP0DR[LPDR1] register bit controls LPTXD0, interface internal only

3.1.1 Glossary

Table 3-2. Glossary Of Terms

Term	Definition
MCU	Microcontroller Unit
CPU	S12Z Central Processing Unit
BDC	S12Z Background Debug Controller
ADC	Analog-to-Digital Converter
PTU	Programmable Trigger Unit
unmapped address range	Address space that is not assigned to a memory
reserved address range	Address space that is reserved for future use cases
illegal access	Memory access, that is not supported or prohibited by the S12ZMMC, e.g. a data store to NVM
access violation	Either an illegal access or an uncorrectable ECC error
byte	8-bit data
word	16-bit data

3.1.2 Overview

The S12ZMMC provides access to on-chip memories and peripherals for the S12ZCPU, the S12ZBDC, the PTU, and the ADC. It arbitrates memory accesses and determines all of the MCU memory maps. Furthermore, the S12ZMMC is responsible for selecting the MCUs functional mode.

3.1.3 Features

- S12ZMMC mode operation control
- Memory mapping for S12ZCPU and S12ZBDC, PTU and ADCs
  - — Maps peripherals and memories into a 16 MByte address space for the S12ZCPU, the S12ZBDC, the PTU, and the ADCs
  - — Handles simultaneous accesses to different on-chip resources (NVM, RAM, and peripherals)
- Access violation detection and logging
  - — Triggers S12ZCPU machine exceptions upon detection of illegal memory accesses and uncorrectable ECC errors
  - — Logs the state of the S12ZCPU and the cause of the access error

Table 5-6. BDCCSRL Field Descriptions (continued)

Field	Description
0 ILLCMD	**Illegal Command Flag** — Indicates an illegal BDC command. This bit is set in the following cases: When an unimplemented BDC command opcode is received. When a DUMP_MEM{_WS}, FILL_MEM{_WS} or READ_SAME{_WS} is attempted in an illegal sequence. When an active BDM command is received whilst BDM is not active When a non Always-available command is received whilst the BDC is disabled or a flash mass erase is ongoing. When a non Always-available command is received whilst the device is secure Read commands return a value of 0xEE for each data byte Writing a “1” to this bit, clears the bit. 0 No illegal command detected. 1 Illegal BDC command detected.

5.4 Functional Description

5.4.1 Security

If the device resets with the system secured, the device clears the BDCCSR UNSEC bit. In the secure state BDC access is restricted to the BDCCSR register. A mass erase can be requested using the ERASE_FLASH command. If the mass erase is completed successfully, the device programs the security bits to the unsecure state and sets the BDC UNSEC bit. If the mass erase is unsuccessful, the device remains secure and the UNSEC bit is not set.

For more information regarding security, please refer to device specific security information.

5.4.2 Enabling BDC And Entering Active BDM

BDM can be activated only after being enabled. BDC is enabled by setting the ENBDC bit in the BDCCSR register, via the single-wire interface, using the command WRITE_BDCCSR.

After being enabled, BDM is activated by one of the following[1]:

- The BDC BACKGROUND command
- A CPU BGND instruction
- The DBG Breakpoint mechanism

Alternatively BDM can be activated directly from reset when resetting into Special Single Chip Mode.

The BDC is ready for receiving the first command 10 core clock cycles after the deassertion of the internal reset signal. This is delayed relative to the external pin reset as specified in the device reset documentation. On S12Z devices an NVM initialization phase follows reset. During this phase the BDC commands classified as always available are carried out immediately, whereas other BDC commands are subject to delayed response due to the NVM initialization phase.

NOTE

After resetting into SSC mode, the initial PC address must be supplied by the host using the WRITE_Rn command before issuing the GO command.

1. BDM active immediately out of special single-chip reset.

6.3.2.20 Debug Comparator C Data Register (DBGCD)

Address: 0x0138, 0x0139, 0x013A, 0x013B

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-22. Debug Comparator C Data Register (DBGCD)

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

This register can be accessed with a byte resolution, whereby DBGCD0, DBGCD1, DBGCD2, DBGCD3 map to DBGCD[31:0] respectively.

XGATE data accesses have a maximum width of 16-bits and are mapped to DBGCD[15:0].

Table 6-37. DBGCD Field Descriptions

Field	Description
31–16 Bits[31:16] (DBGCD0, DBGCD1)	**Comparator Data Bits** — These bits control whether the comparator compares the data bus bits to a logic one or logic zero. The comparator data bits are only used in comparison if the corresponding data mask bit is logic 1. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one
15–0 Bits[15:0] (DBGCD2, DBGCD3)	**Comparator Data Bits** — These bits control whether the comparator compares the data bus bits to a logic one or logic zero. The comparator data bits are only used in comparison if the corresponding data mask bit is logic 1. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

6.3.2.21 Debug Comparator C Data Mask Register (DBGCDM)

Address: 0x013C, 0x013D, 0x013E, 0x013F

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-23. Debug Comparator C Data Mask Register (DBGCDM)

Read: Anytime.

1. If the CDCM field selects range mode comparisons, then DBGCCTL bits configure the comparison, DBGDCTL is ignored.

Table 6-40 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 6-40. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

6.3.2.23 Debug Comparator D Address Register (DBGDAH, DBGDAM, DBGDAL)

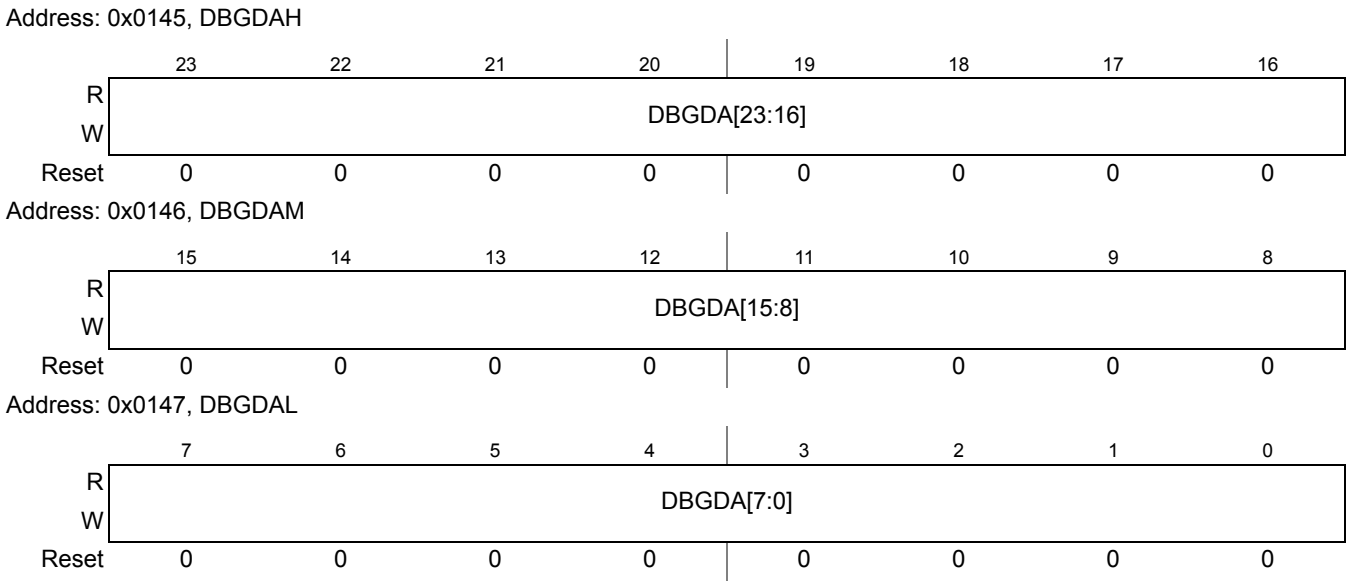

Figure 6-25. Debug Comparator D Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-41. DBGDAH, DBGDAM, DBGDAL Field Descriptions

Field	Description
23–16 DBGDA [23:16]	**Comparator Address Bits [23:16]—** These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

Table 8-23. Selectable Autonomous Periodical Interrupt Periods

APICLK	APIR[15:0]	Selected Period
0	0000	0.2 ms(1)
0	0001	0.4 ms[1]
0	0002	0.6 ms[1]
0	0003	0.8 ms[1]
0	0004	1.0 ms[1]
0	0005	1.2 ms[1]
0	.....	.....
0	FFFD	13106.8 ms[1]
0	FFFE	13107.0 ms[1]
0	FFFF	13107.2 ms[1]
1	0000	2 * Bus Clock period
1	0001	4 * Bus Clock period
1	0002	6 * Bus Clock period
1	0003	8 * Bus Clock period
1	0004	10 * Bus Clock period
1	0005	12 * Bus Clock period
1	.....	.....
1	FFFD	131068 * Bus Clock period
1	FFFE	131070 * Bus Clock period
1	FFFF	131072 * Bus Clock period

1. When f_{ACLK} is trimmed to 20KHz.

8.4.6.3 PLL Bypassed External Mode (PBE)

In this mode, the Bus Clock is based on the external oscillator clock. The reference clock for the PLL is based on the external oscillator.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock or the RC-Oscillator (ACLK).

This mode can be entered from default mode PEI by performing the following steps:

1. Make sure the PLL configuration is valid.
2. Enable the external Oscillator (OSCE bit)
3. Wait for the oscillator to start-up and the PLL being locked (LOCK = 1) and (UPOSC =1)
4. Clear all flags in the CPMUIFLG register to be able to detect any status bit change.
5. Optionally status interrupts can be enabled (CPMUINT register).
6. Select the Oscillator clock as source of the Bus clock (PLLSEL=0)

Loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status (UPOSC=0) in PBE mode is as follows:

- PLLSEL is set automatically and the Bus clock source is switched back to the PLL clock.
- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

NOTE Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

When using the oscillator clock as system clock (write PLLSEL = 0) it is highly recommended to enable the oscillator clock monitor reset feature (write OMRE = 1 in CPMUOSC2 register). If the oscillator monitor reset feature is disabled (OMRE = 0) and the oscillator clock is used as system clock, the system might stall in case of loss of oscillation.

8.5 Resets

8.5.1 General

All reset sources are listed in Table 8-35. There is only one reset vector for all these reset sources. Refer to MCU specification for reset vector address.

Table 8-35. Reset Summary

Reset Source	Local Enable
Power-On Reset (POR)	None
Low Voltage Reset (LVR)	None
External pin $\overline{\text{RESET}}$	None
PLL Clock Monitor Reset	None

9.5.2.12 ADC Conversion Interrupt Flag Register (ADCCONIF)

After being set any of these bits can be cleared by writing a value of 1’b1. All bits are cleared if bit ADC_EN is clear or via ADC soft-reset (bit ADC_SR set). Writing any flag with value 1’b0 does not clear the flag. Writing any flag with value 1’b1 does not set the flag.

Module Base + 0x000C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CON_IF[15:1]															EOL_IF
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-15. ADC Conversion Interrupt Flag Register (ADCCONIF)

Read: Anytime

Write: Anytime

Table 9-17. ADCCONIF Field Descriptions

Field	Description
15-1 CON_IF[15:1]	**Conversion Interrupt Flags** — These bits could be set by the binary coded interrupt select bits INTFLG_SEL[3:0] when the corresponding conversion command has been processed and related data has been stored to RAM. See also notes below.
0 EOL_IF	**End Of List Interrupt Flag** — This bit is set by the binary coded conversion command type select bits CMD_SEL[1:0] for “end of list” type of commands and after such a command has been processed and the related data has been stored RAM. See also second note below

NOTE

These bits can be used to indicate if a certain packet of conversion results is available. Clearing a flag indicates that conversion results have been retrieved by software and the flag can be used again (see also Section 9.9.6, “RVL swapping in RVL double buffer mode and related registers ADCIMDRI and ADCEOLRI.

NOTE

Overrun situation of a flag CON_IF[15:1] and EOL_IF are indicated by flag CONIF_OIF.

12.3.2.7 Timer Control Register 3/Timer Control Register 4 (TCTL3 and TCTL4)

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 12-12. Timer Control Register 3 (TCTL3)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 12-13. Timer Control Register 4 (TCTL4)

Read: Anytime

Write: Anytime.

Table 12-8. TCTL3/TCTL4 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
1:0 EDGnB EDGnA	**Input Capture Edge Control** — These two pairs of control bits configure the input capture edge detector circuits.

Table 12-9. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-11. MSCAN Transmitter Interrupt Enable Register (CANTIER)

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANTIER register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-13. CANTIER Register Field Descriptions

Field	Description
2-0 TXEIE[2:0]	**Transmitter Empty Interrupt Enable** 0 No interrupt request is generated from this event. 1 A transmitter empty (transmit buffer available for transmission) event causes a transmitter empty interrupt request.

13.3.2.9 MSCAN Transmitter Message Abort Request Register (CANTARQ)

The CANTARQ register allows abort request of queued messages as described below.

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-12. MSCAN Transmitter Message Abort Request Register (CANTARQ)

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANTARQ register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-23. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 13-23. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

13.3.3 Programmer’s Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 13.3.2.1, “MSCAN Control Register 0 (CANCTL0)”).

The time stamp register is written by the MSCAN. The CPU can only read these registers.

13.3.3.1.1 IDR0–IDR3 for Extended Identifier Mapping

Module Base + 0x00X0

	7	6	5	4	3	2	1	0
R W	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
Reset:	x	x	x	x	x	x	x	x

Figure 13-26. Identifier Register 0 (IDR0) — Extended Identifier Mapping

Table 13-26. IDR0 Register Field Descriptions — Extended

Field	Description
7-0 ID[28:21]	**Extended Format Identifier** — The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

Module Base + 0x00X1

	7	6	5	4	3	2	1	0
R W	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
Reset:	x	x	x	x	x	x	x	x

Figure 13-27. Identifier Register 1 (IDR1) — Extended Identifier Mapping

Table 13-27. IDR1 Register Field Descriptions — Extended

Field	Description
7-5 ID[20:18]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.
4 SRR	**Substitute Remote Request** — This fixed recessive bit is used only in extended format. It must be set to 1 by the user for transmission buffers and is stored as received on the CAN bus for receive buffers.
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)
2-0 ID[17:15]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

Table 14-12. TG1LIST Register Field Descriptions

Field	Description
0 TG1LIST	Trigger Generator 1 List — This bit shows the number of the current used list. 0 Trigger generator 1 is using list 0 1 Trigger generator 1 is using list 1

- Three complementary pairs and zero independent PWM outputs
- Zero complementary pairs and six independent PWM outputs

All PWM outputs can be generated from the same counter, or each pair can have its own counter for three independent PWM frequencies. Complementary operation permits programmable deadtime insertion, distortion correction through current sensing by software, and separate top and bottom output polarity control. Each counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width-control and full range modulation from 0 percent to 100 percent, are supported. The PMF is capable of controlling most motor types: AC induction motors (ACIM), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

15.1.1 Features

- Three complementary PWM signal pairs, or six independent PWM signals
- Edge-aligned or center-aligned mode
- Features of complementary channel operation:
  - — Deadtime insertion
  - — Separate top and bottom pulse width correction via current status inputs or software
  - — Three variants of PWM output:
    - – Asymmetric in center-aligned mode
    - – Variable edge placement in edge-aligned mode
    - – Double switching in center-aligned mode
- Three 15-bit counters based on core clock
- Separate top and bottom polarity control
- Half-cycle reload capability
- Integral reload rates from 1 to 16
- Programmable fault protection
- Link to timer output compare for 6-step BLDC commutation support with optional counter restart Reload overrun interrupt
- PWM compare output polarity control Software-controlled PWM outputs, complementary or independent

15.1.2 Modes of Operation

Care must be exercised when using this module in the modes listed in Table 15-4. Some applications require regular software updates for proper operation. Failure to do so could result in destroying the hardware setup. Because of this, PWM outputs are placed in their inactive states in STOP mode, and optionally under WAIT and FREEZE modes. PWM outputs will be reactivated (assuming they were active to begin with) when these modes are exited.

the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. Mode fault error doesn't occur in slave mode.

If a mode fault error occurs, the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So SCK, MISO, and MOSI pins are forced to be high impedance inputs to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for a SPI system configured in master mode, output enable of the MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to SPI control register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

NOTE

If a mode fault error occurs and a received data byte is pending in the receive shift register, this data byte will be lost.

17.4.7 Low Power Mode Options

17.4.7.1 SPI in Run Mode

In run mode with the SPI system enable (SPE) bit in the SPI control register clear, the SPI system is in a low-power, disabled state. SPI registers remain accessible, but clocks to the core of this module are disabled.

17.4.7.2 SPI in Wait Mode

SPI operation in wait mode depends upon the state of the SPISWAI bit in SPI control register 2.

- If SPISWAI is clear, the SPI operates normally when the CPU is in wait mode
- If SPISWAI is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
  - If SPISWAI is set and the SPI is configured for master, any transmission and reception in progress stops at wait mode entry. The transmission and reception resumes when the SPI exits wait mode.
  - If SPISWAI is set and the SPI is configured as a slave, any transmission and reception in progress continues if the SCK continues to be driven from the master. This keeps the slave synchronized to the master and the SCK.

    If the master transmits several bytes while the slave is in wait mode, the slave will continue to send out bytes consistent with the operation mode at the start of wait mode (i.e., if the slave is currently sending its SPIDR to the master, it will continue to send the same byte. Else if the slave is currently sending the last received byte from the master, it will continue to send each previous master byte).

18.3.2.3 GDU Interrupt Enable Register (GDUIE)

Module Base + 0x0002 — Access: User read write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	GOCIE[1:0]		GDSEIE	GHHDIE	GLVLSIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-5. GDU Interrupt Enable Register (GDUIE)

1. Read: Anytime
   Write: Anytime

Table 18-5. GDUIE Register Field Descriptions

Field	Description
4-3 GOCIE[1:0]	GDU Overcurrent Interrupt Enable — Enables overcurrent interrupt. 0 No interrupt will be requested if any of the flags GOCIF[1:0] in the GDUF register is set 1 Interrupt will be requested if any of the flags GOCIF[1:0] in the GDUF register is set
2 GDSEIE	GDU Desaturation Error Interrupt Enable — Enables desaturation error interrupt on low-side or high-side drivers 0 No interrupt will be requested if any of the flags in the GDUDSE register is set 1 Interrupt will be requested if any of the flags in the GDUDSE register is set
1 GHHDIE	GDU High HD Interrupt Enable — Enables the high HD interrupt. 0 No interrupt will be requested whenever GHHDIF flag is set 1 Interrupt will be requested whenever GHHDIF flag is set
0 GLVLSIE	GDU Low VLS Interrupt Enable — Enables the interrupt which indicates low VLS supply 0 No interrupt will be requested whenever GLVLSIF flag is set 1 Interrupt will be requested whenever GLVLSIF flag is set

18.3.2.4 GDU Desaturation Error Flag Register (GDUDSE)

Module Base + 0x0003 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	GDHSIF[2:0]			0	GDLSIF[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-6. GDU Desaturation Error Flag Register (GDUDSE)

1. Read: Anytime
   Write: Anytime, write 1 to clear

18.4 Functional Description

18.4.1 General

The PMF module provides the values to be driven onto the outputs of the low-side and high-side FET pre-drivers. If the FET pre-drivers are enabled, the PMF channels drive their corresponding high-side or low-side FET pre-drivers according Table 18-22.

Table 18-22. PMF Channel Assignment

PMF Channel	PMF Channel Assignment
0	High-Side Gate and Source Pins HG[0], HS[0]
1	Low-Side Gate and Source Pins LG[0], LS[0]
2	High-Side Gate and Source Pins HG[1], HS[1]
3	Low-Side Gate and Source Pins LG[1], LS[1]
4	High-Side Gate and Source Pins HG[2], HS[2]
5	Low-Side Gate and Source Pins LG[2], LS[2]

18.4.2 Low-Side FET Pre-Drivers

The three low-side FET pre-drivers turn on and off the external low-side power FETs. The energy required to charge the gate capacitance of the power FET C_G is drawn from the output of the voltage regulator VLS. See Figure 18-20. The register bits GSRCLS[2:0] in the GDUSRC Register (see Figure 18-8) control the slew rate of the low-side FET pre-drivers in order to control fast voltage changes dv/dt (see also Section 18.5.1, “FET Pre-Driver Details).

18.4.3 High-Side FET Pre-Driver

The three high-side FET pre-drivers turn on and off the external high-side power FETs. The required charge for the gate capacitance of the external power FET is delivered by the bootstrap capacitor. After the supply voltage is applied to the microcontroller or after exit from stop mode, the low-side FET pre-drivers should be activated for a short time in order to charge the bootstrap capacitor C_{BS}. Care must be taken after a long period of inactivity of the low-side FET pre-drivers to verify that the bootstrap capacitor C_{BS} is not discharged.

The register bits GSRCHS[2:0] in the GDUSRC Register (see Figure 18-8) control the slew rate of the high-side FET pre-driver in order to control fast voltage changes dv/dt (see also Section 18.5.1, “FET Pre-Driver Details).

NOTE

The minimum PWM pulse on & off time must be $t_{minpulse}$.

Table 20-32. Allowed P-Flash and EEPROM Simultaneous Operations on a single hardblock

	EEPROM				
Program Flash	**Read**	**Margin Read[2]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read	OK[(1)]	OK	OK	OK	
Margin Read[(2)]					
Program					
Sector Erase					
Mass Erase[(3)]					OK

1. Strictly speaking, only one read of either the P-Flash or EEPROM can occur at any given instant, but the memory controller will transparently arbitrate P-Flash and EEPROM accesses giving uninterrupted read access whenever possible.

2. A 'Margin Read' is any read after executing the margin setting commands 'Set User Margin Level' or 'Set Field Margin Level' with anything but the 'normal' level specified. See the Note on margin settings in Section 20.4.7.12 and Section 20.4.7.13.

3. The 'Mass Erase' operations are commands 'Erase All Blocks' and 'Erase Flash Block'

20.4.7 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation may return invalid data resulting in an illegal access (as described on Section 20.4.6).

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 20.3.2.7).

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

Table A-4. ESD Protection and Latch-up Characteristics

5		Latch-up Current of 5V GPIOs at T=125°C positive negative	I_{LAT}	 +100 -100	-	mA
6		Latch-up Current (VCP, BST, LIN, HD, HS, HG, LG, LS, LD) T=125°C positive negative	I_{LAT}	 +100 -100	-	mA
7		Latch-up Current of 5V GPIOs at 27°C positive negative	I_{LAT}	 +200 -200	-	mA
8		Latch-up Current (VCP, BST, LIN, HD, HS, HG, LG, LS, LD) T= 27°C positive negative	I_{LAT}	 +200 -200	-	mA

A.1.6 Recommended Capacitor Values

Table A-5. Recommended Capacitor Values (nominal component values)

Num	Characteristic	Symbol	Typical	Unit
1	VDDX decoupling capacitor (1) (2)	$C_{VDDX1,2}$	100-220	nF
2	VDDA decoupling capacitor (1)	C_{VDDA}	100-220	nF
3	VDDX stability capacitor (3) (4)	C_{VDD5}	4.7-10	uF
4	VDDC stability capacitor	C_{VDDC}	4.7-10	uF
5	VDDS[2:1] stability capacitor	C_{VDDS}	4.7-10	uF
6	VLS decoupling capacitor (1) (5)	$C_{VLS0,1,2}$	100-220	nF
7	VLS stability capacitor (3) (6)	C_{VLS}	4.7-10	uF
8	VDD decoupling capacitor (1)	C_{VDD}	100-220	nF
9	VDDF decoupling capacitor (1)	C_{VDDF}	100-220	nF
10	LIN decoupling capacitor (1)	C_{LIN}	220	pF

1. X7R ceramic
2. One capacitor per VDDX pin
3. 4.7μF ceramic or 10μF tantalum
4. Can be placed anywhere on the 5V supply node (VDDA, VDDX)
5. One capacitor per each VLS[2:0] pin
6. Can be placed anywhere on the VLS node

A.1.7 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted these conditions apply to the following electrical parameters.

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MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP–OUT ZONE FOR PCB ROUTING.

TITLE: LQFP, 12 X 12 X 1.4 PKG, 0.5 PITCH, 80LD, 5.6 X 5.6 EXPOSED PAD	DOCUMENT NO: 98ASA00505D	REV: X2
	STANDARD: NON–JEDEC	
	SHEET: 4	