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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP Exposed Pad
Supplier Device Package	80-TQFP-EP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc25f1wkkr

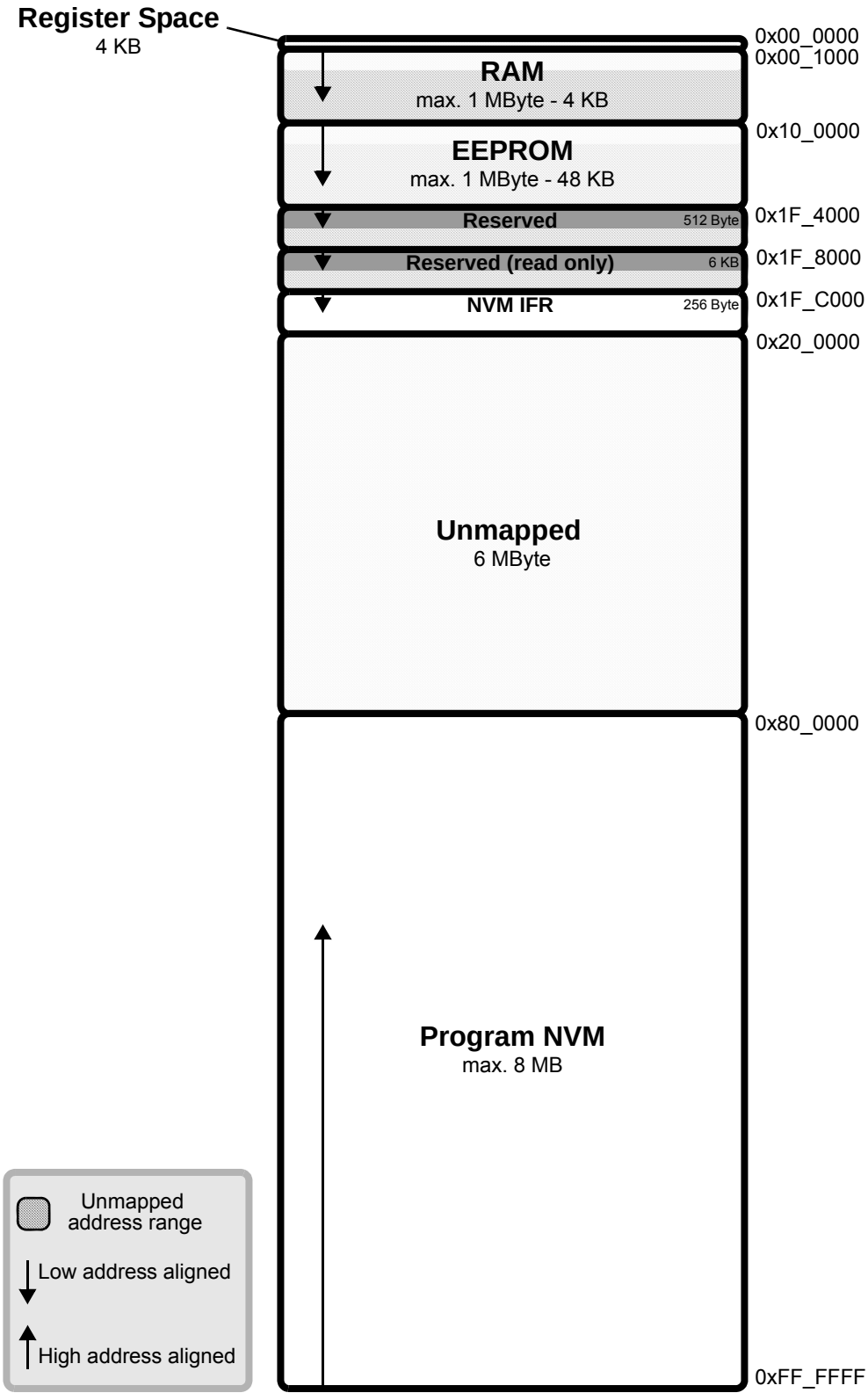


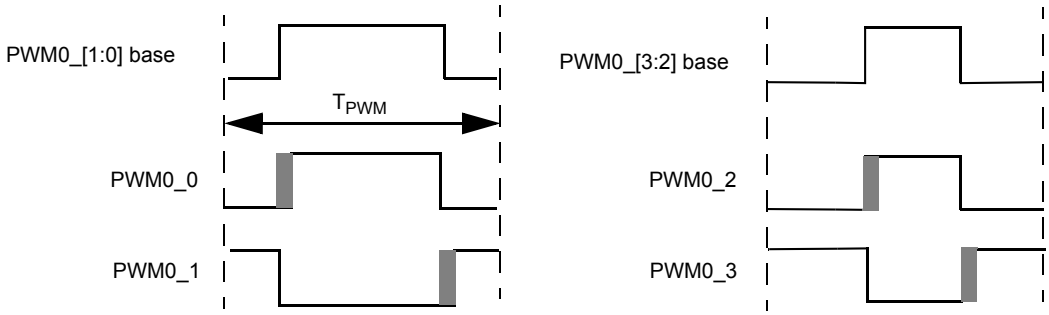
Figure 1-2. MC9S12ZVM-Family Global Memory Map. (See Table 1-3 for individual device details)

1.7.4.1 Pin Summary And Signal Mapping

Table 1-8. Pin Summary For 64-Pin and 48-Pin Package Options (Sheet 1 of 4)

LQFP Option				Function (Priority and device dependencies specified in PIM chapter)					Power Supply	Internal Pull Resistor	
64 M/ ML	64 MC	48	Pin	1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
1	—	1	LIN0	—	—	—	—	—	—	—	Up (weak)
—	1	—	BCTLC	—	—	—	—	—	—	—	—
2	2	2	BKGD	MODC	—	—	—	—	V_{DDX}	—	Up
3	3	3	PS0 (1)	KWS0	RXD1	RXCAN0	LP0RXD	PTUT0 / IOC0_1	V_{DDX}	PERS/ PPSS	Up
4	4	4	PS1 (1)	KWS1	TXD1	TXCAN0	LP0TXD	PTUT1 / IOC0_2	V_{DDX}	PERS/ PPSS	Up
5	5	—	PS2	KWS2	RXD1	MISO0	—	—	V_{DDX}	PERS/ PPSS	Up
6	6	—	PS3	KWS3	DBGEEV	TXD1	MOSI0	—	V_{DDX}	PERS/ PPSS	Up
7	7	—	PS4	KWS4	SCK0	PDOCLK	—	—	V_{DDX}	PERS/ PPSS	Up
8	8	—	PS5	KWS5	SS0	PDO	—	—	V_{DDX}	PERS/ PPSS	Up
9	9	5	BCTL	—	—	—	—	—	—	—	—
10	10	6	HD	—	—	—	—	—	—	—	—
11	11	7	VCP	—	—	—	—	—	—	—	—
12	12	8	BST	—	—	—	—	—	—	—	—
13	13	9	VSSB	—	—	—	—	—	—	—	—
14	14	10	CP	—	—	—	—	—	—	—	—
15	15	11	VLS_OUT	—	—	—	—	—	—	—	—
16	16	12	VSUP	—	—	—	—	—	V_{SUP}	—	—
17	17	13	VDDX2	—	—	—	—	—	V_{DDX}	—	—
18	18	14	TEST	—	—	—	—	—	—	RESET	Down
19	19	15	VSS2	—	—	—	—	—	—	—	—

Figure 1-13. BDCM Complementary Mode Waveform



Assuming first quadrant operation, forward accelerating operation, the applied voltage at node A must exceed the applied voltage at node B (Figure 1-11). Thus the PWM0_0 duty cycle must exceed the PWM0_2 duty cycle.

The duty cycle of PWM0_0 defines the voltage at the first power stage branch.

The duty cycle of PWM0_2 defines the voltage at the second power stage branch.

Modulating the duty cycle every period using the function F_{PWM} then the duty cycle is expressed as:

PWM0_0 duty-cycle = 0.5 + (0.5 * F_{PWM}); For -1<=F_{PWM} <= 1;

PWM0_2 duty-cycle = 0.5 - (0.5 * F_{PWM})

by the CPU monitoring flags or responding to interrupts. The TIM then generates the commutation_event under CPU control, based on the zero crossing time.

1. Enable TIM OC0 and select toggle action on output compare event: TCTL2[OM0:OL0]=0b01.
2. Enable PMF commutation event input: PMFCFG1[ENCE]=0b1.
3. Enable internal ADC channel for measuring the phase voltages from the muxed GDU outputs.
4. Align rotor to stator field. Initialize phase MUX using register GDUPHMUX.
5. Startup motor by applying PWM to an arbitrary motor phase.
6. Take samples of the phase voltages periodically based on PWM cycle to detect zero crossing.
7. Calculate the delay to next commutation and store value to output compare register. Update registers with next values of mask and swap.
8. On next output compare event the buffered mask and swap information are transferred to the active PMF register to execute the commutation.

1.13.6 PMSM Control

PMSM control drives all 3 phases simultaneously with sinusoidal waveforms. Both sensorless and Sine-Cosine position sensor control loop operation are supported.

1.13.6.1 PMSM Sensorless Operation

In this configuration the PMSM stator winding currents are driven sinusoidally and the back EMF waveform is also sinusoidal. Thus all 3 phases are active simultaneously. The rotor position and speed are determined by the current and calculated voltages respectively. The back EMF voltage is calculated based on the currents.

1. Configure PMF for complementary mode operation.
2. Configure PMF for center aligned or phase shifted operation.
3. Select correct PMF deadtime insertion based on external FET switches.
4. Enable GDU current sense opamps for measuring the phase currents from 2 external shunts.
5. Map the output pin of each current sense opamp to the ADC input.
6. Optionally use GDU phase comparators for zero crossing detection to correct deadtime distortion.
7. Fetch targeted motor speed parameter from external source (e.g. SCI)
8. Configure PMF period and duty cycle.
9. Startup motor by applying FOC startup algorithm.
10. Take samples of the phase currents periodically based on PWM cycle to determine motor speed.
11. Calculate FOC algorithm to determine back EMF and motor position.

2.3 Memory Map and Register Definition

This section provides a detailed description of all port integration module registers.

Subsection 2.3.1 shows all registers and bits at their related addresses within the global SoC register map. A detailed description of every register bit is given in subsection 2.3.2 to 2.3.4.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F8–0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	RDRP	R	0	0	0	0	0	0	0	RDRP0
		W								
0x02FE–0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL[2]	R	0	0	0	0	0	0	0	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL[2]	R	0	0	0	0	0	0	0	PTPSL0
		W								
0x0334	PPSL[2]	R	0	0	0	0	0	0	0	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL[2]	R	0	0	0	0	0	0	0	PIEL0
		W								
0x0337	PIFL[2]	R	0	0	0	0	0	0	0	PIFL0
		W								

5.3.2.2 BDC Control Status Register Low (BDCCSRL)

Register Address: This register is not in the device memory map. It is accessible using BDC inherent addressing commands

	7	6	5	4	3	2	1	0
R W	WAIT	STOP	RAMWF	OVRUN	NORESP	RDINV	ILLACC	ILLCMD
Reset	0	0	0	0	0	0	0	0

Figure 5-4. BDC Control Status Register Low (BDCCSRL)

Read: BDC access only.

Write: Bits [7:5], [3:0] BDC access only, restricted to flag clearing by writing a “1” to the bit position.
Write: Bit 4 never. It can only be cleared by a SYNC pulse.

If ACK handshaking is enabled then BDC commands with ACK causing a BDCCSRL[3:1] flag setting condition also generate a long ACK pulse. Subsequent commands that are executed correctly generate a normal ACK pulse. Subsequent commands that are not correctly executed generate a long ACK pulse. The first ACK pulse after WAIT or STOP have been set also generates a long ACK. Subsequent ACK pulses are normal, whilst STOP and WAIT remain set.

Long ACK pulses are not immediately generated if an overrun condition is caused by the host driving the BKGD pin low whilst a target ACK is pending, because this would conflict with an attempted host transmission following the BKGD edge. When a whole byte has been received following the offending BKGD edge, the OVRUN bit is still set, forcing subsequent ACK pulses to be long.

Unimplemented BDC opcodes causing the ILLCMD bit to be set do not generate a long ACK because this could conflict with further transmission from the host. If the ILLCMD is set for another reason, then a long ACK is generated for the current command if it is a BDC command with ACK.

Table 5-6. BDCCSRL Field Descriptions

Field	Description
7 WAIT	**WAIT Indicator Flag** — Indicates that the device entered wait mode. Writing a “1” to this bit whilst in wait mode has no effect. Writing a “1” after exiting wait mode, clears the bit. 0 Device did not enter wait mode 1 Device entered wait mode.
6 STOP	**STOP Indicator Flag** — Indicates that the CPU requested stop mode following a STOP instruction. Writing a “1” to this bit whilst not in stop mode clears the bit. Writing a “1” to this bit whilst in stop mode has no effect. This bit can only be set when the BDC is enabled. 0 Device did not enter stop mode 1 Device entered stop mode.
5 RAMWF	**RAM Write Fault** — Indicates an ECC double fault during a BDC write access to RAM. Writing a “1” to this bit, clears the bit. 0 No RAM write double fault detected. 1 RAM write double fault detected.

Table 7-9. Memory access cycles

Access type	ECC error	access cycle	Internal operation	Memory content	Error indication
1 or 3 byte write, non-aligned 2 byte write	no	2	read data from the memory write old + new data to the memory	old + new data	—
	single bit	2	read data from the memory write corrected + new data to the memory	corrected + new data	SBEEIF
	double bit	2	read data from the memory ignore write data[1]	unchanged[1]	initiator module is informed
read access	no	1	read from memory	unchanged	-
	single bit	1	read data from the memory write corrected data back to memory	corrected data	SBEEIF
	double bit	1	read from memory	unchanged	data mark as invalid

The single bit ECC error generates an interrupt when enabled. The double bit ECC errors are reported by the SRAM_ECC module, but handled at MCU level. For more information, see the MMC description.

7.3.1 Non-aligned Memory Write Access

Non-aligned write accesses are separated into a read-modify-write operation. During the first cycle, the logic reads the data from the memory and performs an ECC check. If no ECC errors were detected then the logic generates the new ECC value based on the read and write data and writes the new data word together with the new ECC value into the memory. If required both 2 byte data words are updated.

If the module detects a single bit ECC error during the read cycle, then the logic generates the new ECC value based on the corrected read and new write read. In the next cycle, the new data word and the new ECC value are written into the memory. If required both 2 byte data words are updated. The SBEEIF bit is set. Hence, the single bit ECC error was corrected by the write access. Figure 7-9 shows an example of a 2 byte non-aligned memory write access.

If the module detects a double bit ECC error during the read cycle, then the write access to the memory is blocked and the initiator module is informed about the error[1].

1. On S12ZVMC256 device only, the data are written into the memory even if a double bit ECC error was detected. The data word written to the memory is undefined due to the correction based on a double bit ECC error signature. The written data word is ECC clean.

8.3.2.29 VDDS Status Register (CPMUVDDS)

This register is only available in V10.

The CPMUVDDS register contains the status and flag bits for VDDS1 and VDDS2 to indicate integrity fails. Monitoring of VDDS1 and VDDS2 domain is only active in full performance mode (FPM) and if the respective supply is enabled in CPMUVREGCTL register. It is disabled in reduced performance mode (RPM).

Module Base + 0x001F

	7	6	5	4	3	2	1	0
R	SCS2	SCS1	LVDS2	LVDS1	SCS2IF	SCS1IF	LVS2IF	LVS1IF
W								
Reset	0	0	U	U	0	0	U	U

The Reset state of LVDS and LVIF depends on the external supplied VDDA level
"U" = Unknown, either 0 or 1

= Unimplemented or Reserved

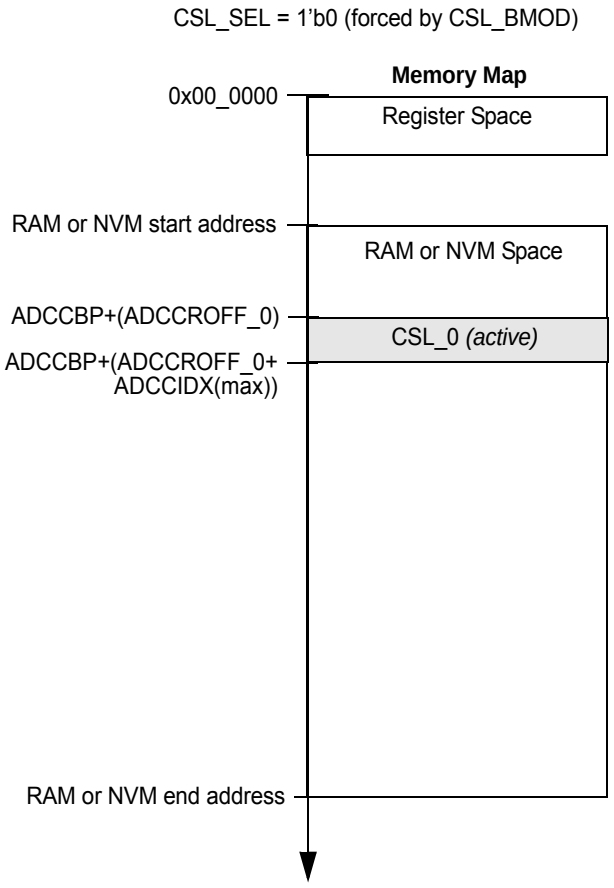
Figure 8-40. VDDS Status Register (CPMUVDDS)

Read: Anytime

Write: SCS2IF, SCS1IF, LVS2IF and LVS1IF are write anytime,
SCS2, SCS, LVS2 and LVS1 are read only

Table 8-33. CPMUVDDS Field Descriptions

Field	Description
7 SCS2	Short circuit on VDDS2 Status Bit —This read-only status bit reflects short circuit status on VDDS2 supply. This feature only makes sense if the VDDS2 supply is enabled (EXT2SON=1). 0 VRH2EN=0 or RPM or VDDS2 voltage level is less than or equal to VDDA supply. 1 VRH2EN=1and FPM and the voltage level on VDDS2 is greater than on VDDA supply.
6 SCS1	Short circuit on VDDS1 Status Bit —This read-only status bit reflects short circuit status on VDDS1 supply. This feature only makes sense if the VDDS1 supply is enabled (EXT1SON=1). 0 VRH1EN=0 or RPM or VDDS1 voltage level is less than or equal to VDDA supply. 1 VRH1EN=1and FPM and the voltage level on VDDS1 is greater than on VDDA supply.
5 LVDS2	Low Voltage on VDDS2 Status Bit —This read-only status bit reflects the voltage level on VDDS2 supply. If VDDS2 is enabled (EXTS2ON=1 in CPMUVREGCTL register), it is monitored that VDDS2 does not drop below a voltage threshold V_{DDSM}. 0 VDDS2 voltage is above V_{DDSM} threshold or VDDS2 is disabled or RPM. 1 EXTS2ON =1 and VDDS2 voltage is below V_{DDSM} threshold and FPM.
4 LVDS1	Low Voltage on VDDS1 Status Bit —This read-only status bit reflects the voltage level on VDDS1 supply. If VDDS1 is enabled (EXTS1ON=1 in CPMUVREGCTL register), it is monitored that VDDS1 does not drop below a voltage threshold V_{DDSM}. 0 VDDS1 voltage is above V_{DDSM} threshold or VDDS1 is disabled or RPM. 1 EXTS1ON =1 and VDDS1 voltage is below V_{DDSM} threshold and FPM.



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 9-32. Command Sequence List Schema in Single Buffer Mode

While the ADC is enabled, one CSL is active (indicated by bit CSL_SEL) and the corresponding list should not be modified anymore. At the same time the alternative CSL can be modified to prepare the ADC for new conversion sequences in CSL double buffered mode. When the ADC is enabled, the command address registers (ADCCBP, ADCCROFF_0/2, ADCCIDX) are read only and register ADCCIDX is under control of the ADC.

14.3.2.15 Trigger Generator 0 List 0 Index (TG0L0IDX)

Module Base + 0x0014 Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	TG0L0IDX[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-17. Trigger Generator 0 List 0 Index (TG0L0IDX)

1. Read: Anytime
   Write: Never

Table 14-17. TG0L0IDX Register Field Descriptions

Field	Description
6:0 TG0L0IDX [6:0]	Trigger Generator 0 List 0 Index Register — This register defines offset of the start point for the trigger event list 0 used by trigger generator 0. This register is read only, so the list 0 for trigger generator 0 will start at the PTUPTR address. For more information see Section 14.4.2, “Memory based trigger event list”.

14.3.2.16 Trigger Generator 0 List 1 Index (TG0L1IDX)

Module Base + 0x0015 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	TG0L1IDX[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-18. Trigger Generator 0 List 1 Index (TG0L1IDX)

1. Read: Anytime
   Write: Anytime, if TG0EN bit is cleared

Table 14-18. TG0L1IDX Register Field Descriptions

Field	Description
6:0 TG0L1IDX [6:0]	Trigger Generator 0 List 1 Index Register — This register cannot be modified after the TG0EN bit is set. This register defines offset of the start point for the trigger event list 1 used by trigger generator 0. For more information see Section 14.4.2, “Memory based trigger event list”.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKB bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODB returns the value in the buffer. It is not necessarily the value the PWM generator B is currently using.

15.3.2.28 PMF Deadtime B Register (PMFDTMB)

Address: Module Base + 0x002E — Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PMFDTMB											
W																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Figure 15-33. PMF Deadtime B Register (PMFDTMB)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to the maximum value of 0x0FFF, selecting a deadtime of 4095 PWM clock cycles. Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows:

$$T_{DEAD\_B} = PMFDTMB / f_{PWM\_B} = PMFDTMB \times P_B \times T_{core} \qquad \textit{Eqn. 15-2}$$

15.3.2.29 PMF Enable Control C Register (PMFENCC)

Address: Module Base + 0x0030 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-34. PMF Enable Control C Register (PMFENCC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. GLDOKC and RSTRTC cannot be modified after the WP bit is set.

16.3.2.5 SCI Alternative Control Register 2 (SCIACR2)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-8. SCI Alternative Control Register 2 (SCIACR2)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 16-7. SCIACR2 Field Descriptions

Field	Description
7 IREN	**Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	**Transmitter Narrow Pulse Bits** — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 16-8.
2:1 BERRM[1:0]	**Bit Error Mode** — Those two bits determines the functionality of the bit error detect feature. See Table 16-9.
0 BKDFE	**Break Detect Feature Enable** — BKDFE enables the break detect circuitry. 0 Break detect circuit disabled 1 Break detect circuit enabled

Table 16-8. IRSCI Transmit Pulse Width

TNP[1:0]	Narrow Pulse Width
11	1/4
10	1/32
01	1/16
00	3/16

Table 16-9. Bit Error Mode Coding

BERRM1	BERRM0	Function
0	0	Bit error detect circuit is disabled
0	1	Receive input sampling occurs during the 9th time tick of a transmitted bit (refer to Figure 16-19)
1	0	Receive input sampling occurs during the 13th time tick of a transmitted bit (refer to Figure 16-19)
1	1	Reserved

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0007 Reserved	R								
	W								

= Unimplemented or Reserved

Figure 17-2. SPI Register Summary

17.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

17.3.2.1 SPI Control Register 1 (SPICR1)

Module Base +0x0000

	7	6	5	4	3	2	1	0
R W	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

Figure 17-3. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

Table 17-2. SPICR1 Field Descriptions

Field	Description
7 SPIE	**SPI Interrupt Enable Bit** — This bit enables SPI interrupt requests, if SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	**SPI System Enable Bit** — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	**SPI Transmit Interrupt Enable** — This bit enables SPI interrupt requests, if SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	**SPI Master/Slave Mode Select Bit** — This bit selects whether the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode. 1 SPI is in master mode.

To re-enable the transmitter then, the LPDTIF flag must be cleared (by writing a 1).

NOTE

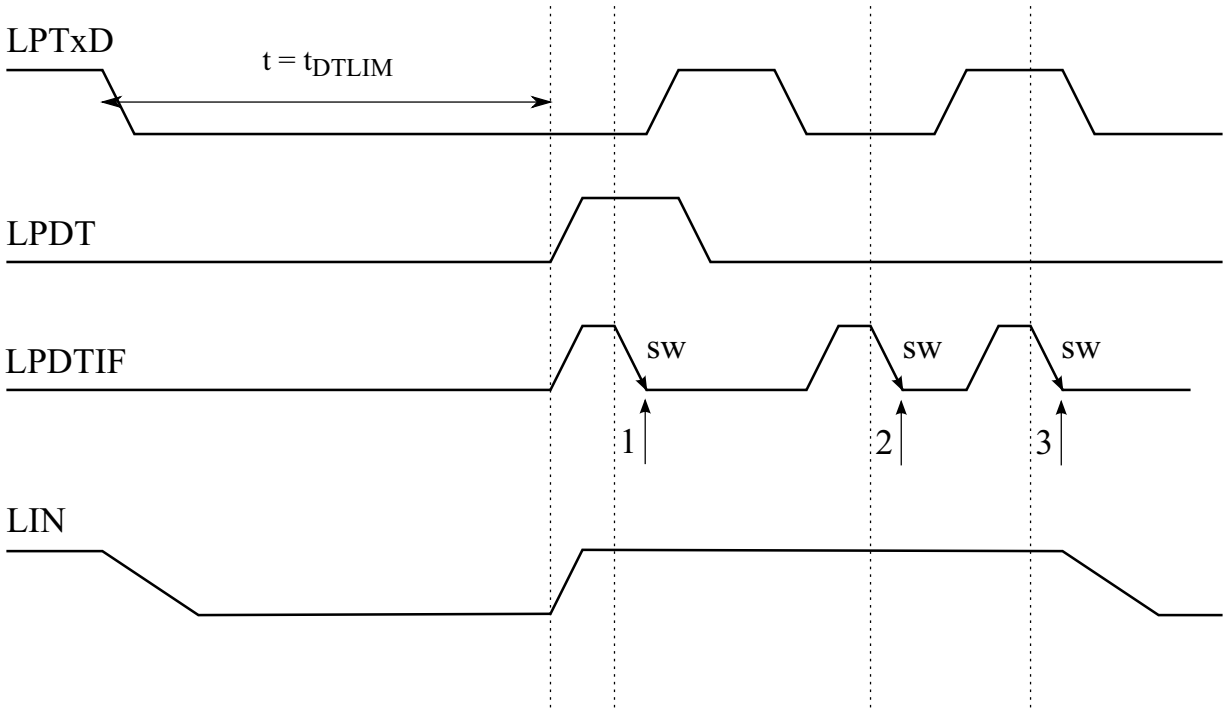
Please make sure that LPDTIF=1 before trying to clear it. It is not allowed to try to clear LPDTIF if LPDTIF=0 already.

After clearing LPDTIF, if the TxD-dominant timeout condition is still present or the LPTxD pin is dominant while being in normal mode, the transmitter remains disabled and the LPDTIF flag is set after a time again to indicate that the attempt to re-enable has failed. This time is equal to:

- minimum 1 IRC period (1 us) + 2 bus periods
- maximum 2 IRC periods (2 us) + 3 bus periods

If the bit LPDTIE is set in the LPIE register, an interrupt is requested.

Figure 19-13 shows the different scenarios of TxD-dominant timeout interrupt handling.



1: Flag cleared, transmitter re-enable not successful because TxD-dominant timeout condition is still present
2: Flag cleared, transmitter re-enable not successful because LPTxD is dominant
3: Flag cleared, transmitter re-enable successful

Figure 19-13. TxD-dominant timeout interrupt handling

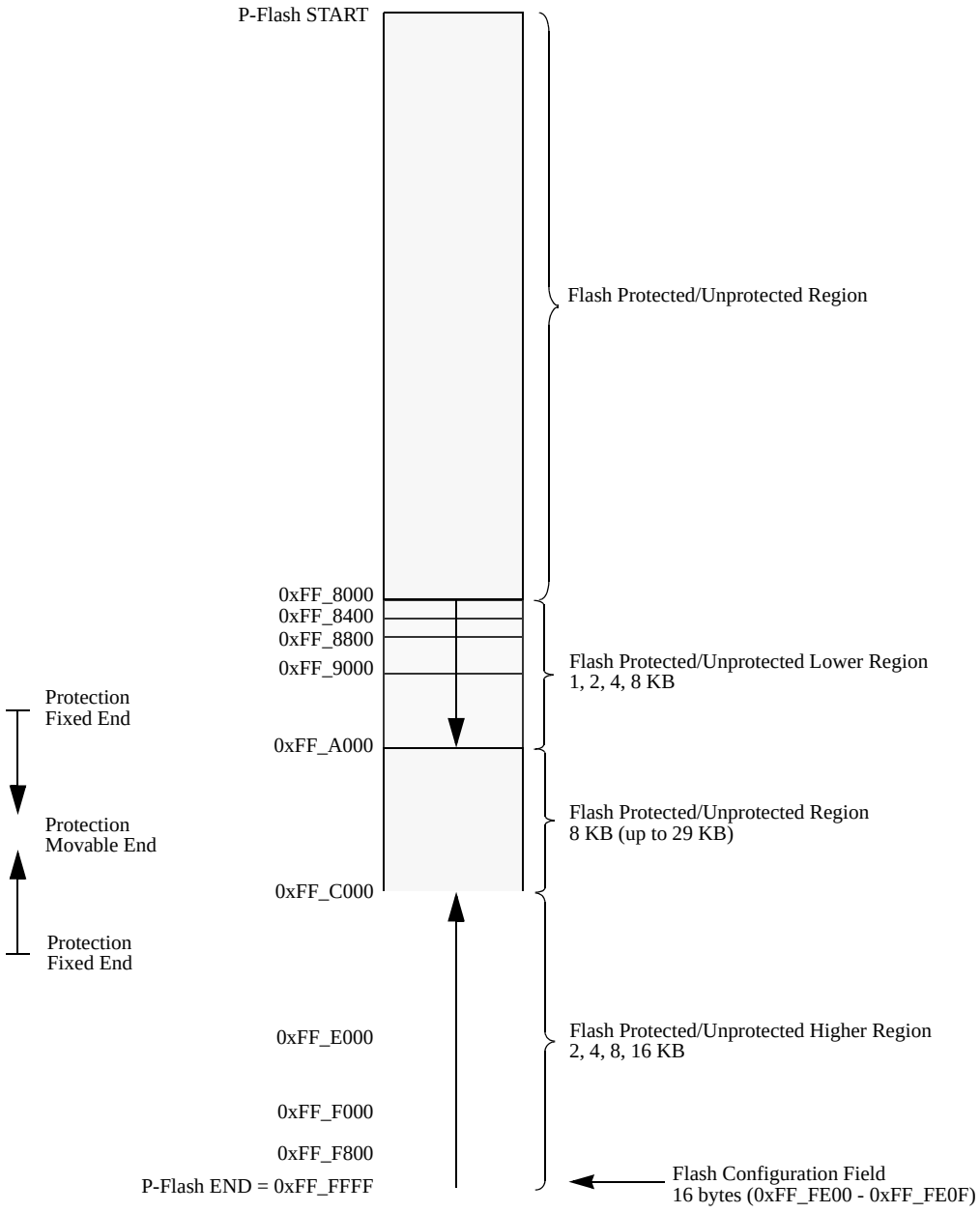


Figure 20-2. P-Flash Memory Map With Protection Alignment

Table C-2. ADC Electrical Characteristics (Junction Temperature From –40°C To +175°C)

Supply voltage 3.13 V < V_{DDA} < 5.5 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Max input source resistance	R_S	—	—	1	KΩ
2		Total input capacitance Non sampling Total input capacitance Sampling	C_{INN} C_{INS}	— —	— —	10 16	pF
3a		Input internal Resistance Junction temperature from –40×°C to +150°C	R_{INA}	—	5	9.9	kΩ
3b		Input internal Resistance Junction temperature from 150°C to +175°C	R_{INA}	—	—	12	kΩ
4		Disruptive analog input current	I_{NA}	-2.5	—	2.5	mA
5		Coupling ratio positive current injection	K_p	—	—	1E-4	A/A
6		Coupling ratio negative current injection	K_n	—	—	5E-3	A/A

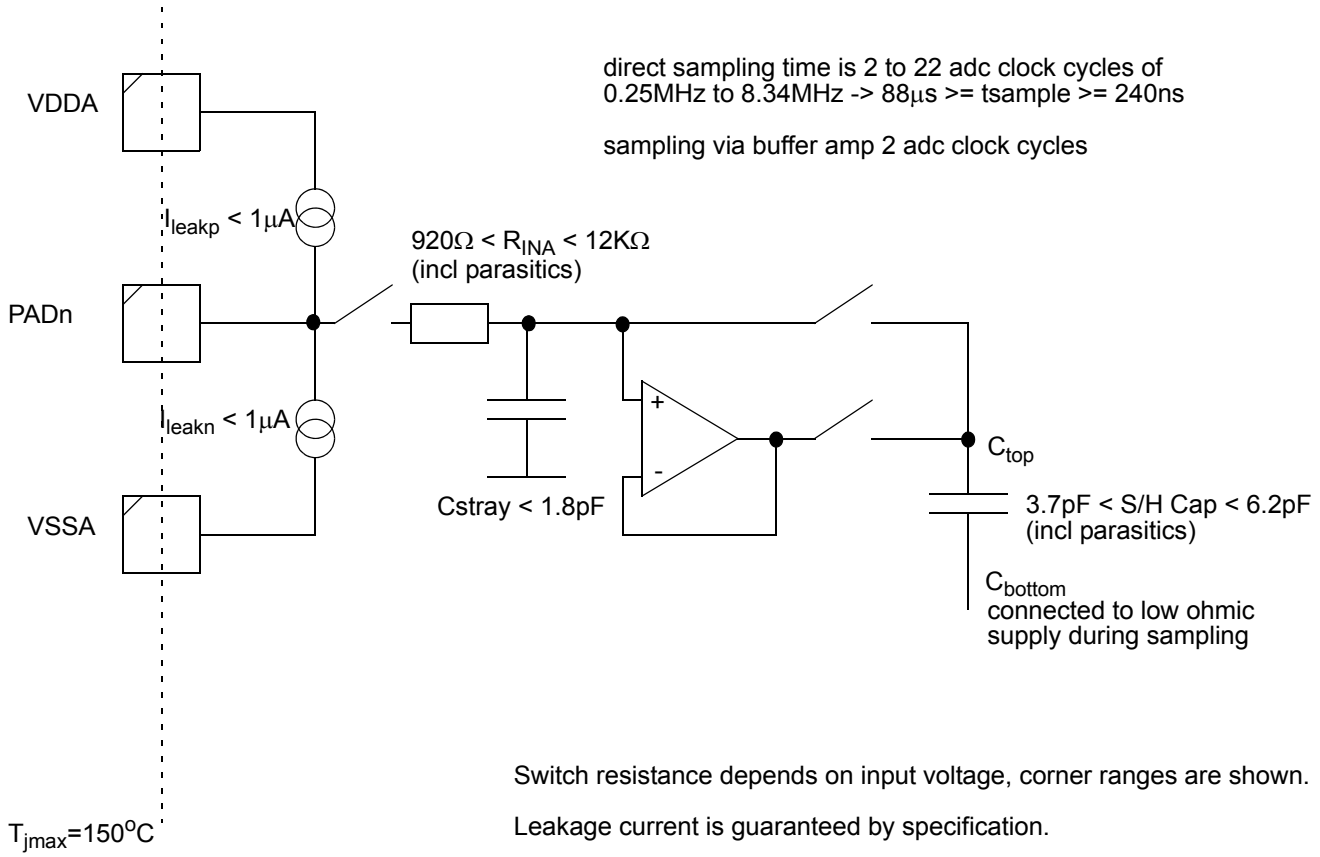


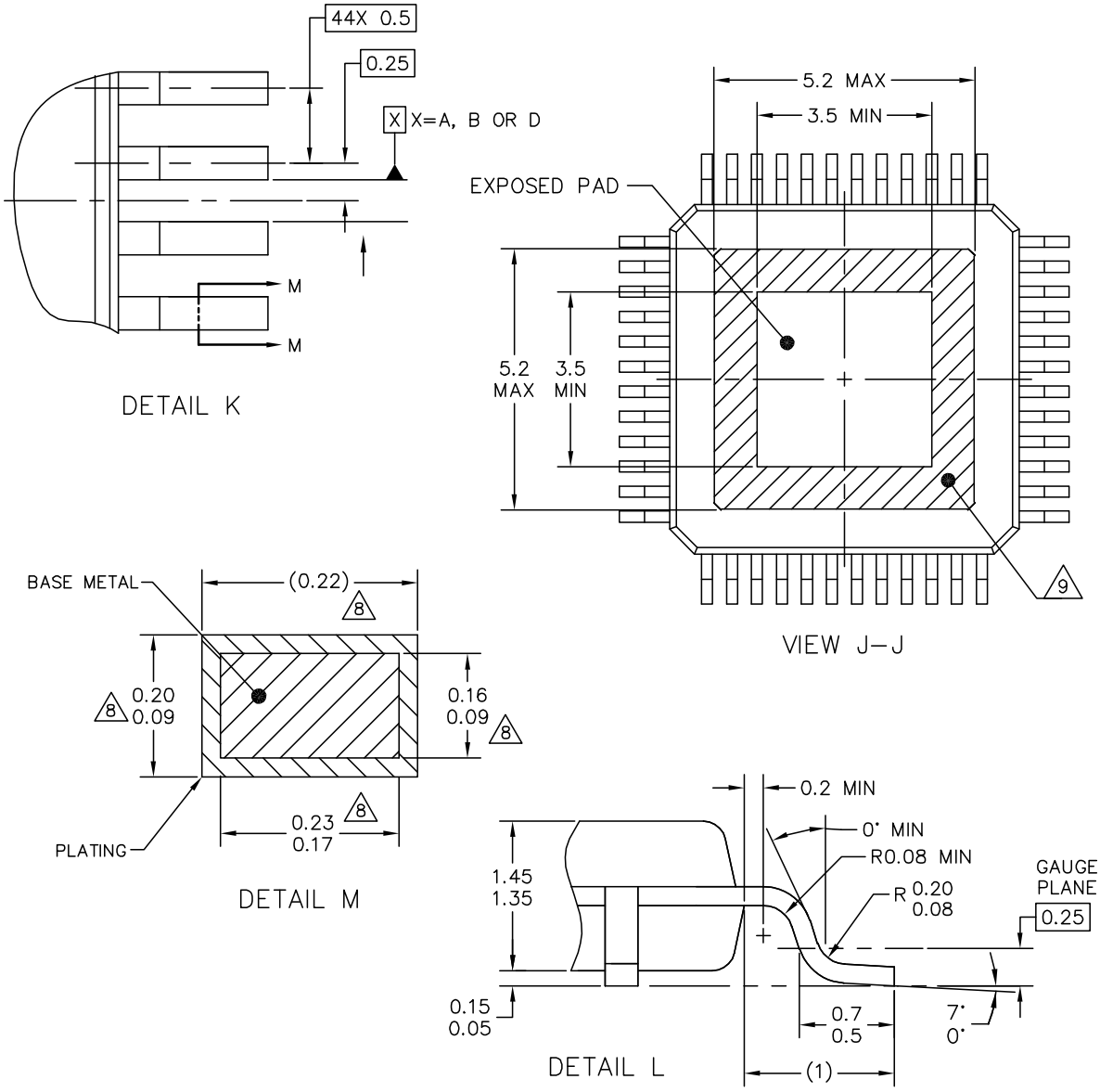
Figure C-1.

3. For high side, the performance of external diodes may influence this parameter.
4. If VSUP is lower than 11.2V, external FET gate drive will diminish and roughly follow VSUP - 2* Vbe
5. Total gate charge spec is only a recommendation. FETs with higher gate charge can be used when resulting slew rates are tolerable by the application and resulting power dissipation does not lead to thermal overload.
6. Blanking time for assert (see device level mask set dependencies)
7. (VBSx - HSx) = 10V respectively VLSx=10V, measured from 1V to 9V HGx/LGx vs HSx/LSx
8. (VBSx - HSx) = 10V respectively VLSx=10V, measured from 9V to 1V HGx/LGx vs HSx/LSx
9. The delay is dependent on slew rate configuration. The variation on a given device for a given slew setting is much less than the specified range.
10. V(VBSx) - V(VLSx) > 9V, resp VLSx > 9V
11. V(VBSx) - V(VLSx) > 9V, resp VLSx > 9V, nmos branch only
12. V(VBSx) - V(VLSx) > 9V, resp VLSx > 9V, pmos branch only
13. Not tested on the mask set 2N95G, which does not feature the BST pin function
14. VLS > 6V
15. Output current range for which the effective output resistance specification applies
16. Input resistance can be calculated from the pin input leakage because the sense amp has high impedance MOS inputs
17. Av=10, no frequency compensation in feedback network, 90% output swing
18. Low side desaturation comparator range extends to LSx <= 2.35V - $V_{desatls}$

E.2 Preliminary GDU specifications for devices featuring GDU V5

Table E-2. GDUV5 Electrical Characteristics (Junction Temperature From –40°C To +175°C)

4.85V<=VDDX,VDDA<=5.15V						
Num	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	VSUP Supply range	V_{VSUP}	-0.3	—	40	V
2a	VSUP, HD Supply range FETs can be turned on(1) (normal range)	V_{VSUP}/V_{HD}	7	14	20	V
2b	VSUP, HD Supply range FETs can be turned on(2) (extended range)	V_{VSUP}/V_{HD}	7	14	26.6	V
3	External FET Vgs drive with boost(3) (7V < V_{RBATP} < 20V)	V_{VGS}	9	9.6	12	V
4	External FET Vgs drive without boost(4)	V_{VGS}	5	9.6	12	V
5	External FET total gate charge @ 10V(5)	QG	—	50	—	nC
6	Pull resistance between HGx and HSx	R_{HSpul}	60	80	120	KΩ
7	Pull resistance between LGx and LSx	R_{LSpul}	60	80	120	KΩ
8a	VLS output voltage for Vsup >=12.5V, Iout=30mA -40°C < T_j < 150°C	V_{VLS_OUT}	10.5	11	11.5	V
8b	VLS output voltage for Vsup >=12.5V, Iout=30mA 150°C < T_j < 175°C	V_{VLS_OUT}	10.0	10.6	11.5	V
9	VLS current limit threshold	I_{LIMVLS}	60	77	112	mA
10a	VLS low voltage monitor trippoint assert (GVLSLVL=1)	V_{LVLSHA}	6.2	6.5	7	V
10b	VLS low voltage monitor trippoint deassert (GVLSLVL=1)	V_{LVLSHD}	6.2	6.58	7	V
10c	VLS low voltage monitor trippoint assert (GVLSLVL=0)	V_{LVLSLA}	5.2	5.5	6	V
10d	VLS low voltage monitor trippoint deassert (GVLSLVL=0)	V_{LVLSLD}	5.2	5.55	6	V
11a	HD high voltage monitor assert trippoint low	V_{HVHDLA}	20	21	22	V
11b	HD high voltage monitor deassert trippoint low	V_{HVHDLD}	19.5	20.5	21.6	V
12a	HD high voltage monitor assert trippoint high	V_{HVHDHA}	26.6	28.3	29.4	V
12b	HD high voltage monitor deassert trippoint high	V_{HVHDHD}	26.2	27.9	29	V



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TITLE: LQFP, 7 X 7 X 1.4 PKG, 0.5 PITCH, 48LD 4.4 X 4.4 EXPOSED PAD	DOCUMENT NO: 98ASA00945D	REV: X0
	STANDARD: NON-JEDEC	
	02 NOV 2015	

M.11 0x0580-0x059F PTU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0589	TG0TVL	R	TG0TV[7:0]							
		W								
0x058A	TG1LIST	R	0	0	0	0	0	0	0	TG1LIST
		W								
0x058B	TG1TNUM	R	0	0	0	TG1TNUM4:0]				
		W								
0x058C	TG1TVH	R	TG1TV[15:8]							
		W								
0x058D	TG1TVL	R	TG1TV[7:0]							
		W								
0x058E	PTUCNTH	R	PTUCNT[15:8]							
		W								
0x058F	PTUCNTL	R	PTUCNT[7:0]							
		W								
0x0590	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0591	PTUPTRH	R	PTUPTR[23:16]							
		W								
0x0592	PTUPTRM	R	PTUPTR[15:8]							
		W								
0x0593	PTUPTRL	R	PTUPTR[7:1]							0
		W								
0x0594	TG0L0IDX	R	0	0	0	0	0	0	0	0
		W								
0x0595	TG0L1IDX	R	0	TG0L1IDX[6:0]						
		W								
0x0596	TG1L0IDX	R	0	TG1L0IDX[6:0]						
		W								
0x0597	TG1L1IDX	R	0	TG1L1IDX[6:0]						
		W								
0x0598 - 0x059E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x059F	PTUDEBUG	R	0	PTUREPE	PTUT1PE	PTUT0PE	0	0	0	0
		W						PTUFRE	TG1FTE	TG0FTE