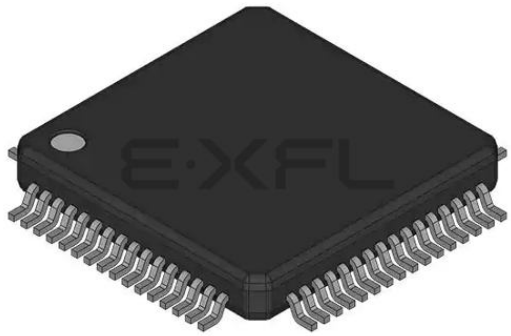

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Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f1mkh

1.6 Device Memory Map

Table 1-5 shows the device register memory map. All modules that can be instantiated more than once on S12 devices are listed with an index number, even if they are only instantiated once on this device family.

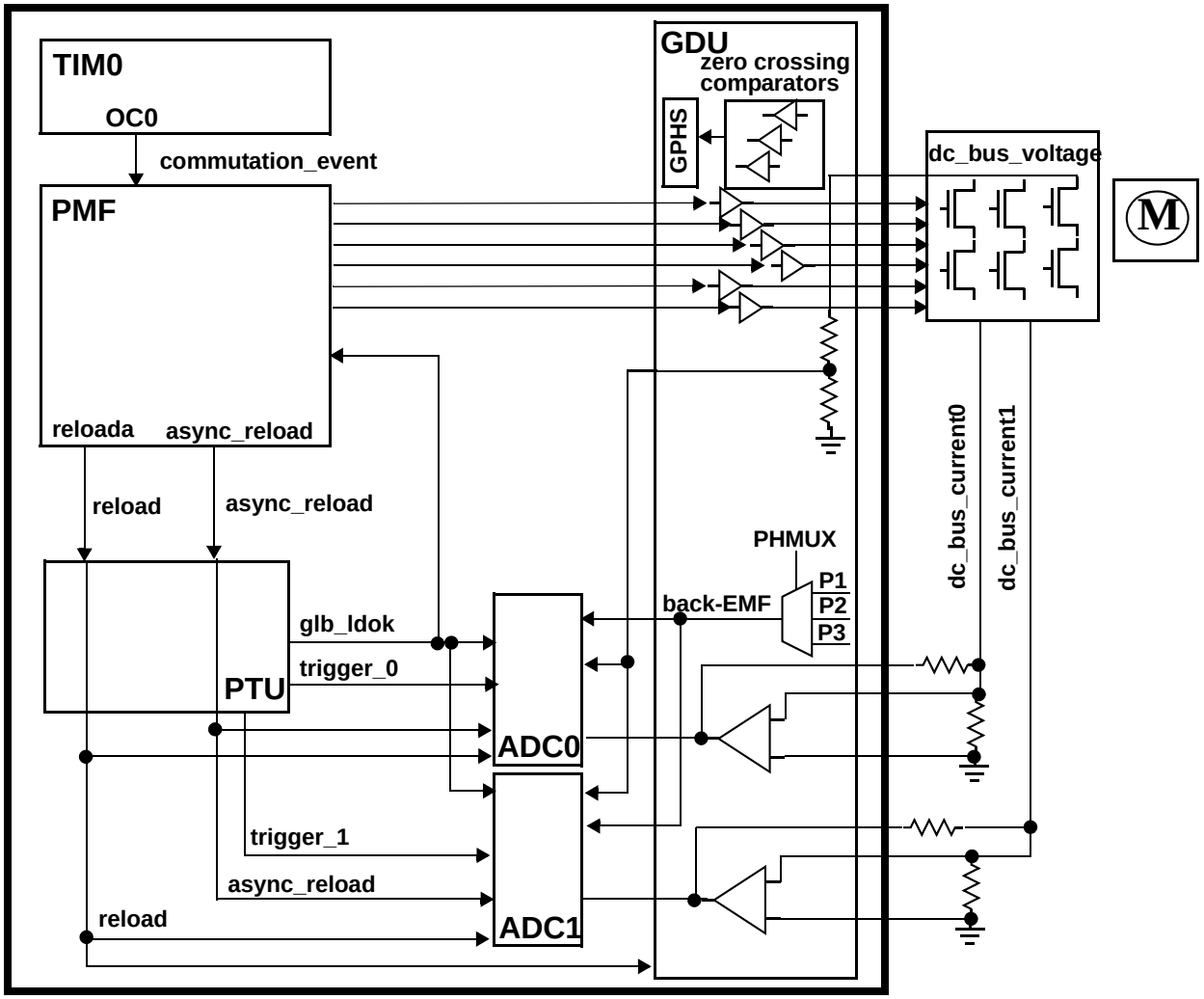
Table 1-5. Module Register Address Ranges

Address	Module	Size (Bytes)
0x0000–0x0003	Part ID Register Section 1.6.2	4
0x0004–0x000F	Reserved	12
0x0010–0x001F	INT	16
0x0020–0x006F	Reserved	80
0x0070–0x008F	MMC	32
0x0090–0x00FF	MMC Reserved	112
0x0100–0x017F	DBG	128
0x0180–0x01FF	Reserved	128
0x0200–0x033F	PIM	320
0x0340–0x037F	Reserved	64
0x0380–0x039F	FTMRZ	32
0x03A0–0x03BF	Reserved	32
0x03C0–0x03CF	RAM ECC	16
0x03D0–0x03FF	Reserved	48
0x0400–0x043F	TIM1 (ZVMC256 only)	64
0x0440–0x047F	Reserved	64
0x0480–0x04AF	PWM0 (ZVMC256 only)	48
0x04B0–0x04FF	Reserved[1]	80
0x0500–0x053F	PMF	64
0x0540–0x057F	Reserved	64
0x0580–0x059F	PTU	32
0x05A0–0x05BF	Reserved	32
0x05C0–0x05EF	TIM0	48
0x05F0–0x05FF	Reserved	16
0x0600–0x063F	ADC0	64
0x0640–0x067F	ADC1	64
0x0680–0x069F	Reserved	32
[2]0x06A0–0x06BF	GDU	32
0x06C0–0x06DF	CPMU	32

7. Read port register PTIT[3:1] to determine starting sector.
8. Startup motor by applying PWM to the related motor phase.
9. In IC1 interrupt ISR calculate the delay to next commutation and store value to output compare register. Update registers with next values of mask and swap.
10. On next output compare event the buffered mask and swap information is transferred to the active PMF registers to execute the commutation.

1.13.5.2 Sensorless Commutation

Figure 1-15. Sensorless BLDC Configuration



To calculate the commutation time in a sensorless motor system the back-EMF zero crossing event of the currently non-fed phase within an electrical rotation cycle must be determined. For fast motor rotation, the ADC is used to measure the back-EMF voltage and the DC bus voltage to determine the zero crossing time. For slow motor rotation the GPHS register can be polled. In either case the zero crossing event is handled

to start the bit up to one target clock cycle earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 5-6 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD pin. Internal glitch detect logic requires the pin be driven high no later than eight target clock cycles after the falling edge for a logic 1 transmission.

Since the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.

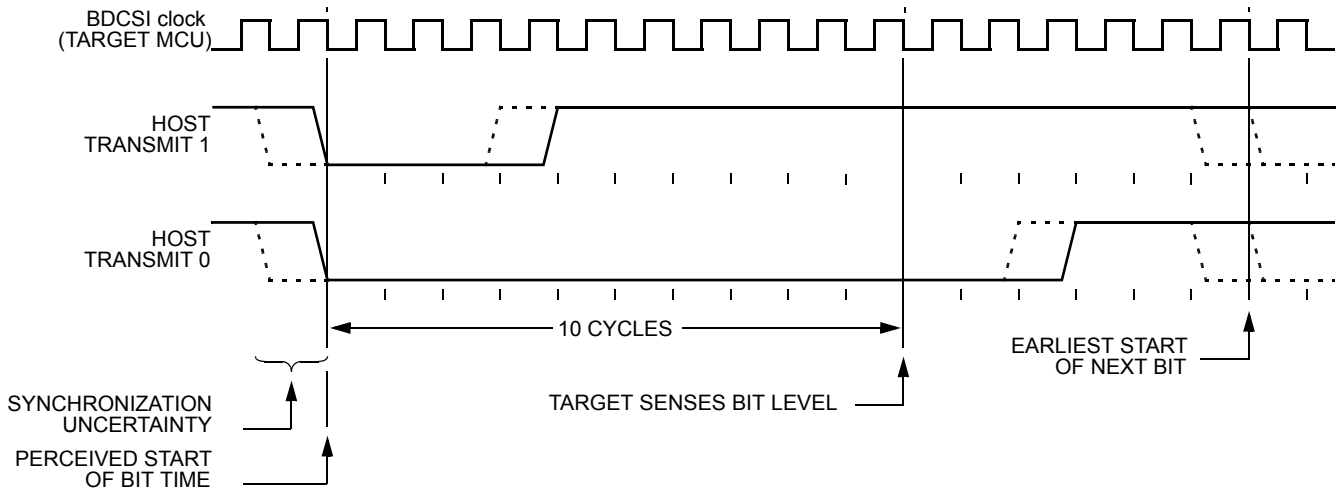


Figure 5-6. BDC Host-to-Target Serial Bit Timing

Figure 5-7 shows the host receiving a logic 1 from the target system. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive at the latest after 6 clock cycles, before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

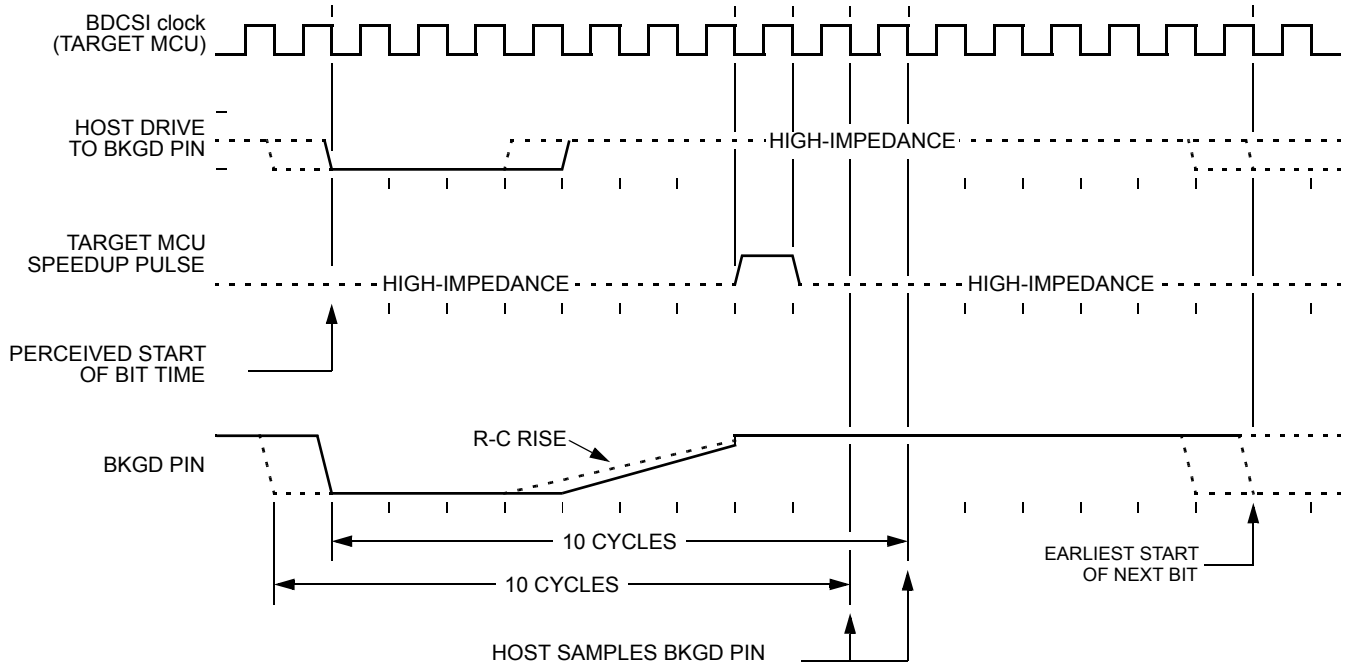


Figure 5-7. BDC Target-to-Host Serial Bit Timing (Logic 1)

Figure 5-8 shows the host receiving a logic 0 from the target. The host initiates the bit time but the target finishes it. Since the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

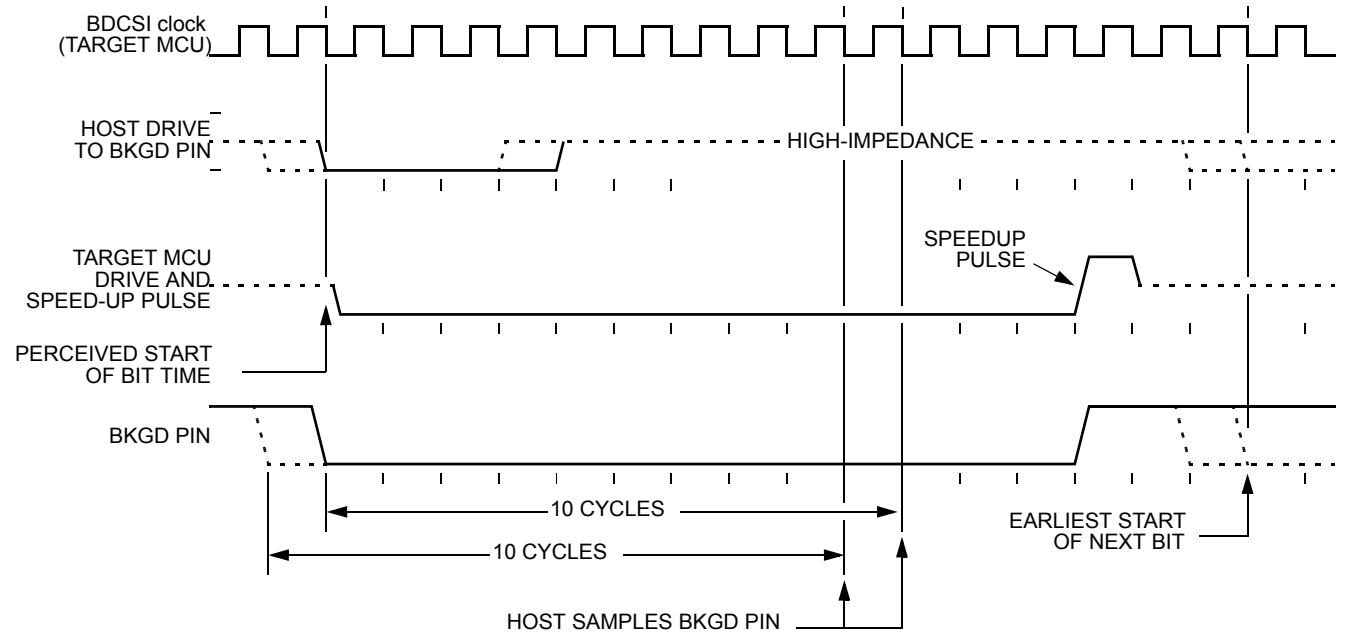


Figure 5-8. BDC Target-to-Host Serial Bit Timing (Logic 0)

6.4.3.1.2 Data Access Comparator Match

Data access matches are generated when an access occurs at the address contained in the comparator address register. The match can be qualified by the access data and by the access type (read/write). The breakpoint occurs a maximum of 2 instructions after the access in the CPU flow. Note, if a COF occurs between access and breakpoint, the opcode address of the breakpoint can be elsewhere in the memory map.

Opcode fetches are not classed as data accesses. Thus data access matches are not possible on opcode fetches.

6.4.3.2 External Event

The DBGEEV input signal can force a state sequencer transition, independent of internal comparator matches. The DBGEEV is an input signal mapped directly to a device pin and configured by the EEVE field in DBGC1. The external events can change the state sequencer state, or force a trace buffer entry, or gate trace buffer entries.

If configured to change the state sequencer state, then the external match is mapped to DBGSCRx bits C3SC[1:0]. In this configuration, internal comparator channel3 is de-coupled from the state sequencer but can still be used for timestamps. The DBGEFR bit EEVF is set when an external event occurs.

6.4.3.3 Setting The TRIG Bit

Independent of comparator matches it is possible to initiate a tracing session and/or breakpoint by writing the TRIG bit in DBGC1 to a logic “1”. This forces the state sequencer into the Final State. If configured for End aligned tracing or for no tracing, the transition to Final State is followed immediately by a transition to State0. If configured for Begin- or Mid Aligned tracing, the state sequencer remains in Final State until tracing is complete, then it transitions to State0.

Breakpoints, if enabled, are issued on the transition to State0.

6.4.3.4 Profiling Trace Buffer Overflow Event

During code profiling a trace buffer overflow forces the state sequencer into the disarmed State0 and, if breakpoints are enabled, issues a breakpoint request to the CPU.

6.4.3.5 Event Priorities

If simultaneous events occur, the priority is resolved according to Table 6-46. Lower priority events are suppressed. It is thus possible to miss a lower priority event if it occurs simultaneously with an event of a higher priority. The event priorities dictate that in the case of simultaneous matches, the match on the higher comparator channel number (3,2,1,0) has priority.

If a write access to DBGC1 with the ARM bit position set occurs simultaneously to a hardware disarm from an internal event, then the ARM bit is cleared due to the hardware disarm.

Table 6-46. Event Priorities

Priority	Source	Action
Highest	TB Overflow	Immediate force to state 0, generate breakpoint and terminate tracing

6.4.5 Trace Buffer Operation

The trace buffer is a 64 lines deep by 64-bits wide RAM array. If the TSOURCE bit is set the DBG module can store trace information in the RAM array in a circular buffer format. Data is stored in mode dependent formats, as described in the following sections. After each trace buffer entry, the counter register DBGCNT is incremented. Trace buffer rollover is possible when configured for End- or Mid-Aligned tracing, such that older entries are replaced by newer entries. Tracing of CPU activity is disabled when the BDC is active.

The RAM array can be accessed through the register DBGTB using 16-bit wide word accesses. After each read, the internal RAM pointer is incremented so that the next read will receive fresh information. Reading the trace buffer whilst the DBG is armed returns invalid data and the trace buffer pointer is not incremented.

In Detail mode the address range for CPU access tracing can be limited to a range specified by the TRANGE bits in DBGTCRH. This function uses comparators C and D to define an address range inside which accesses should be traced. Thus traced accesses can be restricted, for example, to particular register or RAM range accesses.

The external event pin can be configured to force trace buffer entries in Normal or Loop1 trace modes. All tracing modes support trace buffer gating. In Pure PC and Detail modes external events do not force trace buffer entries.

If the external event pin is configured to gate trace buffer entries then any trace mode is valid.

6.4.5.1 Trace Trigger Alignment

Using the TALIGN bits (see Section 6.3.2.3”) it is possible to align the trigger with the end, the middle, or the beginning of a tracing session.

If End or Mid-Alignment is selected, tracing begins when the ARM bit in DBGC1 is set and State1 is entered. The transition to Final State if End-Alignment is selected, ends the tracing session. The transition to Final State if Mid-Alignment is selected signals that another 32 lines are traced before ending the tracing session. Tracing with Begin-Alignment starts at the trigger and ends when the trace buffer is full.

Table 6-47. Tracing Alignment

TALIGN	Tracing Begin	Tracing End
00	On arming	At trigger
01	At trigger	When trace buffer is full
10	On arming	When 32 trace buffer lines have been filled after trigger
11	Reserved	

6.4.5.1.1 Storing with Begin-Alignment

Storing with Begin-Alignment, data is not stored in the trace buffer until the Final State is entered. Once the trigger condition is met the DBG module remains armed until 64 lines are stored in the trace buffer.

When the DBG module is disarmed but profiling transmission is ongoing, register write accesses are suppressed and reading from the DBGTB returns the code 0xEEEE.

6.4.6.3 Code Profiling Internal Data Storage Format

When profiling starts, the first trace buffer entry is made to provide the start address. This uses a 4 byte format (PTS), including the INFO byte and a 3-byte PC start address. In order to avoid trace buffer overflow a fully compressed format is used for direct (conditional branch) COF information.

Table 6-59. Profiling Trace buffer line format

Format	8-Byte Wide Trace Buffer Line							
	7	6	5	4	3	2	1	0
PTS					PC Start Address			INFO
PTIB	Indirect	Indirect	Indirect	Direct	Direct	Direct	Direct	INFO
PTHF			0	Direct	Direct	Direct	Direct	INFO
PTVB	Timestamp	Timestamp	Vector	Direct	Direct	Direct	Direct	INFO
PTW	Timestamp	Timestamp	0	Direct	Direct	Direct	Direct	INFO

The INFO byte indicates the line format used. Up to 4 bytes of each line are dedicated to branch COFs. Further bytes are used for storing indirect COF information (indexed jumps and interrupt vectors). Indexed jumps force a full line entry with the PTIB format and require 3-bytes for the full 24-bit destination address. Interrupts force a full line entry with the PTVB format, whereby vectors are stored as a single byte and a 16-bit timestamp value is stored simultaneously to indicate the number of core clock cycles relative to the previous COF. At each trace buffer entry the 16-bit timestamp counter is cleared. The device vectors use address[8:0] whereby address[1:0] are constant zero for vectors. Thus the value stored to the PTVB vector byte is equivalent to (Vector Address[8:1]).

After the PTS entry, the pointer increments and the DBG begins to fill the next line with direct COF information. This continues until the direct COF field is full or an indirect COF occurs, then the INFO byte and, if needed, indirect COF information are entered on that line and the pointer increments to the next line.

If a timestamp overflow occurs, indicating a 65536 bus clock cycles without COF, then an entry is made with the TSOVF bit set, INFO[6] (Table 6-60) and profiling continues.

If a trace buffer overflow occurs, a final entry is made with the TBOVF bit set, profiling is terminated and the DBG is disarmed. Trace buffer overflow occurs when the trace buffer contains 64 lines pending transmission.

Whenever the DBG is disarmed during profiling, a final entry is made with the TERM bit set to indicate the final entry.

When a final entry is made then by default the PTW line format is used, except if a COF occurs in the same cycle in which case the corresponding PTIB/PTVB/PTHF format is used. Since the development tool receives the INFO byte first, it can determine in advance the format of data it is about to receive. The

Chapter 8
S12 Clock, Reset and Power Management Unit (V10 and V6)

Table 8-1. Revision History

Rev. No. (Item No)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V10.01	3 Dec. 2014		• Signal Description: added Figures to illustrate application of BCTL and BCTLS1 • VDDS1, VDDS2, SNPS1, SNPS2, BCTLS1, BCTLS2: added pins to Block Diagram and Signal Description
V10.02	22 Jan. 2015		• correct typo in CPMUVREGTRIM0 register bits
V10.03	23 Jan. 2015		• added section: differences between V10 and V6 • changed Framemaker variables to have V10_V6 instead of V10
V10.04	27 Jan. 2015		• Diagram “BCTLS1 application example”: added VRH switch • Added bits VRH2EN and VRH1EN to CPMUVREGCTL register
V10.05	10 Feb. 2015		• Signal description of VDDS1/2: removed statement “monitored by LVR” • Formal cleanup of header 1.2.6
V10.06	20 Feb. 2015		• CPMUVREGCTL register: added footnote for bits only available in version V10
V10.07	3 Mar. 2015		• CPMULVCTL register: added VDDSIE interrupt enable bit for VDDS1 and VDDS2 fail events • Added CPMUVDDS register with 4 status bits and 4 interrupt flags
V10.08	11 Mar. 2015		• CPMUVDDS register: added detailed register description • Interrupt chapter: Added VDDS Integrity Interrupt • Updated Differences V10 versus V6
V10.09	27 Mar. 2015		• Syntax cleanup
V10.10	22 April 2015		• Removed blank page • Corrected typo in Application section
V10.11	24 April 2015		• Signal Description: Added more details to the description of the VDDS1, VDDS2, SNPS1, SNPS2 signals
V10.12	15 Sept. 2015		• CPMUVDDS register: corrected reset values
V10.13	6 Oct. 2015		• Section: Differences V10 versus V6: changed “VDD Integrity” to “VDDS Integrity” • Improved EXTCON Bit description regarding presence of CANPHY • CPMUVDDS register: Improved description of SCS1 and SCS2 Bits.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0009 TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
	W								
0x000A TCTL3	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								
0x000B TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
	W								
0x000C TIE	R	RESERVED	RESERVED	RESERVED	RESERVED	C3I	C2I	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	RESERVED	PR2	PR1	PR0
	W								
0x000E TFLG1	R	RESERVED	RESERVED	RESERVED	RESERVED	C3F	C2F	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x001F TCxH–TCxL[1]	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 11-3. TIM16B4CV3 Register Summary (Sheet 2 of 2)

1. The register is available only if corresponding channel exists.

11.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	IOS3	IOS2	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 11-4. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

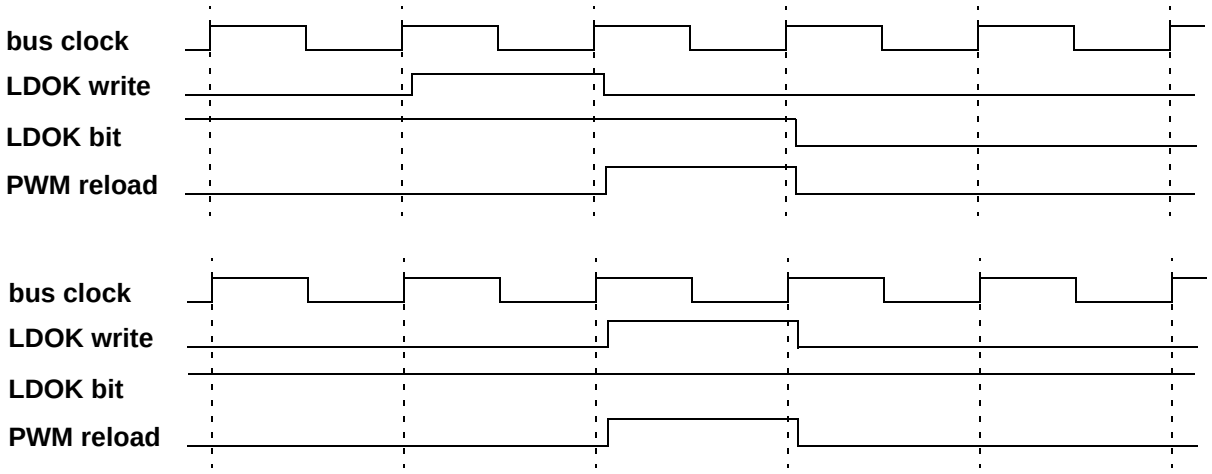


Figure 15-72. Setting asserted LDOK bit at PWM reload event

15.4.12.2 Global Load Enable

If a global load enable bit GLDOKA, B, or C is set, the global load OK bit defined on device level as input to the PMF replaces the function of the related local LDOKA, B, or C bits. The global load OK signal is typically shared between multiple IP blocks with the same double buffer scheme. Software handling must be transferred to the global load OK bit at the chip level.

15.4.12.3 Load Frequency

The LDFQ3, LDFQ2, LDFQ1, and LDFQ0 bits in the PWM control register (PMFFQCx) select an integral loading frequency of 1 to 16-PWM reload opportunities. The LDFQ bits take effect at every PWM reload opportunity, regardless the state of the related load okay bit or global load OK. The *half* bit in the PMFFQC register controls half-cycle reloads for center-aligned PWMs. If the *half* bit is set, a reload opportunity occurs at the beginning of every PWM cycle and half cycle when the count equals the modulus. If the half bit is not set, a reload opportunity occurs only at the beginning of every cycle. Reload opportunities can only occur at the beginning of a PWM cycle in edge-aligned mode.

NOTE

Setting the half bit takes effect immediately. Depending on whether the counter is incrementing or decrementing at this point in time, reloads at even-numbered reload frequencies (every 2, 4, 6,... reload opportunities) will occur only when the counter matches the modulus or only when the counter equals zero, respectively (refer to example of reloading at every two opportunities in Figure 15-74).

NOTE

Loading a new modulus on a half cycle will force the count to the new modulus value minus one on the next clock cycle. Half cycle reloads are possible only in center-aligned mode. Enabling or disabling half-cycle reloads in edge-aligned mode will have no effect on the reload rate.

16.3.2.2 SCI Control Register 1 (SCICR1)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
Reset	0	0	0	0	0	0	0	0

Figure 16-5. SCI Control Register 1 (SCICR1)

Read: Anytime, if AMAP = 0.

Write: Anytime, if AMAP = 0.

NOTE

This register is only visible in the memory map if AMAP = 0 (reset condition).

Table 16-3. SCICR1 Field Descriptions

Field	Description
7 LOOPS	**Loop Select Bit** — LOOPS enables loop operation. In loop operation, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function. 0 Normal operation enabled 1 Loop operation enabled The receiver input is determined by the RSRC bit.
6 SCISWAI	**SCI Stop in Wait Mode Bit** — SCISWAI disables the SCI in wait mode. 0 SCI enabled in wait mode 1 SCI disabled in wait mode
5 RSRC	**Receiver Source Bit** — When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. See Table 16-4. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter
4 M	**Data Format Mode Bit** — MODE determines whether data characters are eight or nine bits long. 0 One start bit, eight data bits, one stop bit 1 One start bit, nine data bits, one stop bit
3 WAKE	**Wakeup Condition Bit** — WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD pin. 0 Idle line wakeup 1 Address mark wakeup
2 ILT	**Idle Line Type Bit** — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

16.4.6.3 Data Sampling

The RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 16-21) is re-synchronized immediatelly at bus clock edge:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

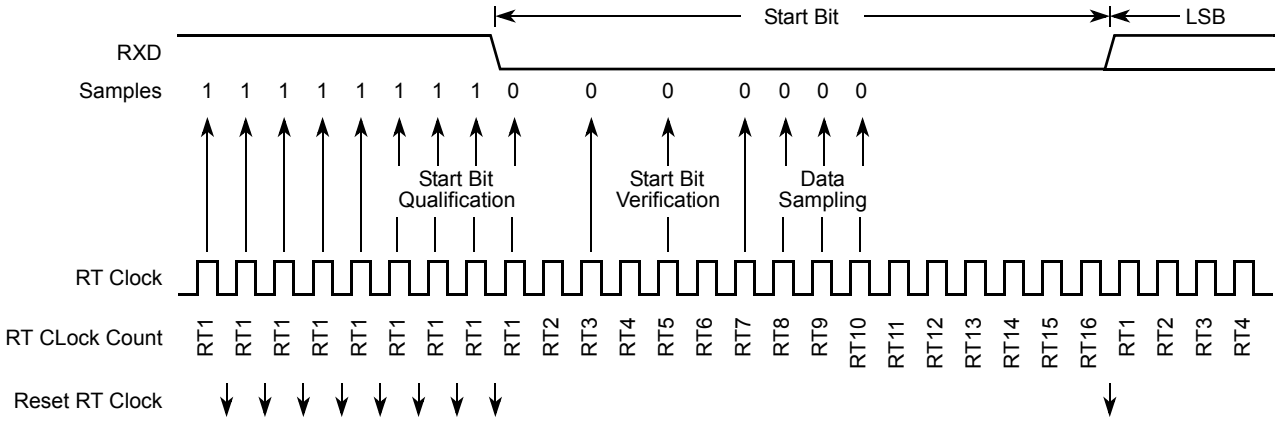


Figure 16-21. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Figure 16-17 summarizes the results of the start bit verification samples.

Table 16-17. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

Table 18-2. GDUV4/V5/V6 Differences(1)

Feature	GDU V4	GDU V5	GDU V6
On chip bootstrap diode	not available, off chip bootstrap diode required	available	not available, off chip bootstrap diode required
Desaturation filter bits GDSFLS/GDSFHS	not available	available	available
Fault[3] output to PMF	driven by GLVLSIF	driven by GLVLSF	driven by GLVLSF
Fault[4] output to PMF	driven by GHHDIF	driven by GHHDF	driven by GHHDF
Low-side drivers on or off out of reset dependent on NVM option	available[1.]	available[1.]	available
additional drain connections LD[2:0] to external low-side power FETs	not available	not available	available
Control bits GSRMOD1/0 for SR motor drive	not available	not available	available

1. Refer to device overview for mask set / GDU version info.

The GDU module is a Field Effect Transistor (FET) pre-driver designed for three phase motor control applications.

18.1.1 Features

The GDU module includes these distinctive features:

- 11V voltage regulator for FET pre-drivers
- Boost converter option for low supply voltage condition
- 3-phase bridge FET pre-drivers
- Bootstrap circuit for high-side FET pre-drivers with external bootstrap capacitor
- Charge pump for static high-side driver operation
- Phase voltage measurement with internal ADC
- Two low-side current measurement amplifiers for DC phase current measurement
- Phase comparators for BEMF zero crossing detection in sensorless BLDC applications
- Voltage measurement on HD pin (DC-Link voltage) with internal ADC
- Desaturation comparator for high-side drivers and low-side drivers protection
- Undervoltage detection on FET pre-driver supply pin VLS
- Two overcurrent comparators with programmable voltage threshold
- Overvoltage detection on 3-phase bridge supply HD pin

18.3.2.11 GDU Current Sense Offset Register (GDUCSO)

Module Base + 0x000A — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	GCSO1[2:0]			0	GCSO0[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-13. GDU Current Sense Offset (GDUCSO)

1. Read: Anytime
   Write: Anytime

Table 18-14. GDUCSO Register Field Descriptions

Field	Description (See also Section 18.4.8, “Current Sense Amplifier and Overcurrent Comparator)
6:4 GCSO1[2:0]	GDU Current Sense Amplifier 1 Offset — These bits adjust the offset of the current sense amplifier 000 No offset 001 Offset is +3mV (GDUV5 and V6). Offset is +5mV (GDUV4). 010 Offset is +6mV (GDUV5 and V6). Offset is +10mV (GDUV4) 011 Offset is +9mV (GDUV5 and V6). Offset is +15mV (GDUV4) 100 No offset 101 Offset is -9mV (GDUV5 and V6). Offset is -15mV (GDUV4) 110 Offset is -6mV (GDUV5 and V6). Offset is -10mV (GDUV4). 111 Offset is -3mV (GDUV5 and V6). Offset is -5mV (GDUV4).
2:0 GCSO0[2:0]	GDU Current Sense Amplifier 0 Offset — These bits adjust the offset of the current sense amplifier. 000 No offset 001 Offset is +3mV (GDUV5 and V6). Offset is +5mV (GDUV4). 010 Offset is +6mV (GDUV5 and V6). Offset is +10mV (GDUV4) 011 Offset is +9mV (GDUV5 and V6). Offset is +15mV (GDUV4) 100 No offset 101 Offset is -9mV (GDUV5 and V6). Offset is -15mV (GDUV4) 110 Offset is -6mV (GDUV5 and V6). Offset is -10mV (GDUV4). 111 Offset is -3mV (GDUV5 and V6). Offset is -5mV (GDUV4).

18.3.2.12 GDU Desaturation Level Register (GDUDSLVL)

Module Base + 0x000B — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GDSFHS	GDSLHS[2:0]			GDSFLS	GDSLLS[2:0]		
W								
Reset	0	0	0	0	0	1	1	1

= Unimplemented

Figure 18-14. GDU Desaturation Level Register (GDUDSLVL)

1. Read: Anytime
   Write: Only if GWP=0

Table 20-12. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	**Common Command Register Index**— The CCOBIX bits are used to indicate how many words of the FCCOB register array are being read or written to. See Section 20.3.2.13, “Flash Common Command Object Registers (FCCOB)“,” for more details.

20.3.2.4 Flash Protection Status Register (FPSTAT)

This Flash register holds the status of the Protection Override feature.

Offset Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	FPOVRD	0	0	0	0	0	0	WSTATACK
W								
Reset	0	0	0	0	0	0	0	1

= Unimplemented or Reserved

Figure 20-8. Flash Protection Status Register (FPSTAT)

All bits in the FPSTAT register are readable but are not writable.

Table 20-13. FPSTAT Field Descriptions

Field	Description
7 FPOVRD	**Flash Protection Override Status** — The FPOVRD bit indicates if the Protection Override feature is currently enabled. See Section 20.4.7.17, “Protection Override Command” for more details. 0 Protection is not overridden 1 Protection is overridden, contents of registers FPROT and/or DFPROT (and effective protection limits determined by their current contents) were determined during execution of command Protection Override
0 WSTATACK	**Wait-State Switch Acknowledge** — The WSTATACK bit indicates that the wait-state configuration is effectively set according to the value configured on bits FCNFG[WSTAT] (see Section 20.3.2.5, “Flash Configuration Register (FCNFG)”). WSTATACK bit is cleared when a change in FCNFG[WSTAT] is requested by writing to those bits, and is set when the Flash has effectively switched to the new wait-state configuration. The application must check the status of WSTATACK bit to make sure it reads as 1 before changing the frequency setup (see Section 20.4.3, “Flash Block Read Access”). 0 Wait-State switch is pending, Flash reads are still happening according to the previous value of FCNFG[WSTAT] 1 Wait-State switch is complete, Flash reads are already working according to the value set on FCNFG[WSTAT]

20.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt, control generation of wait-states and forces ECC faults on Flash array read access from the CPU.

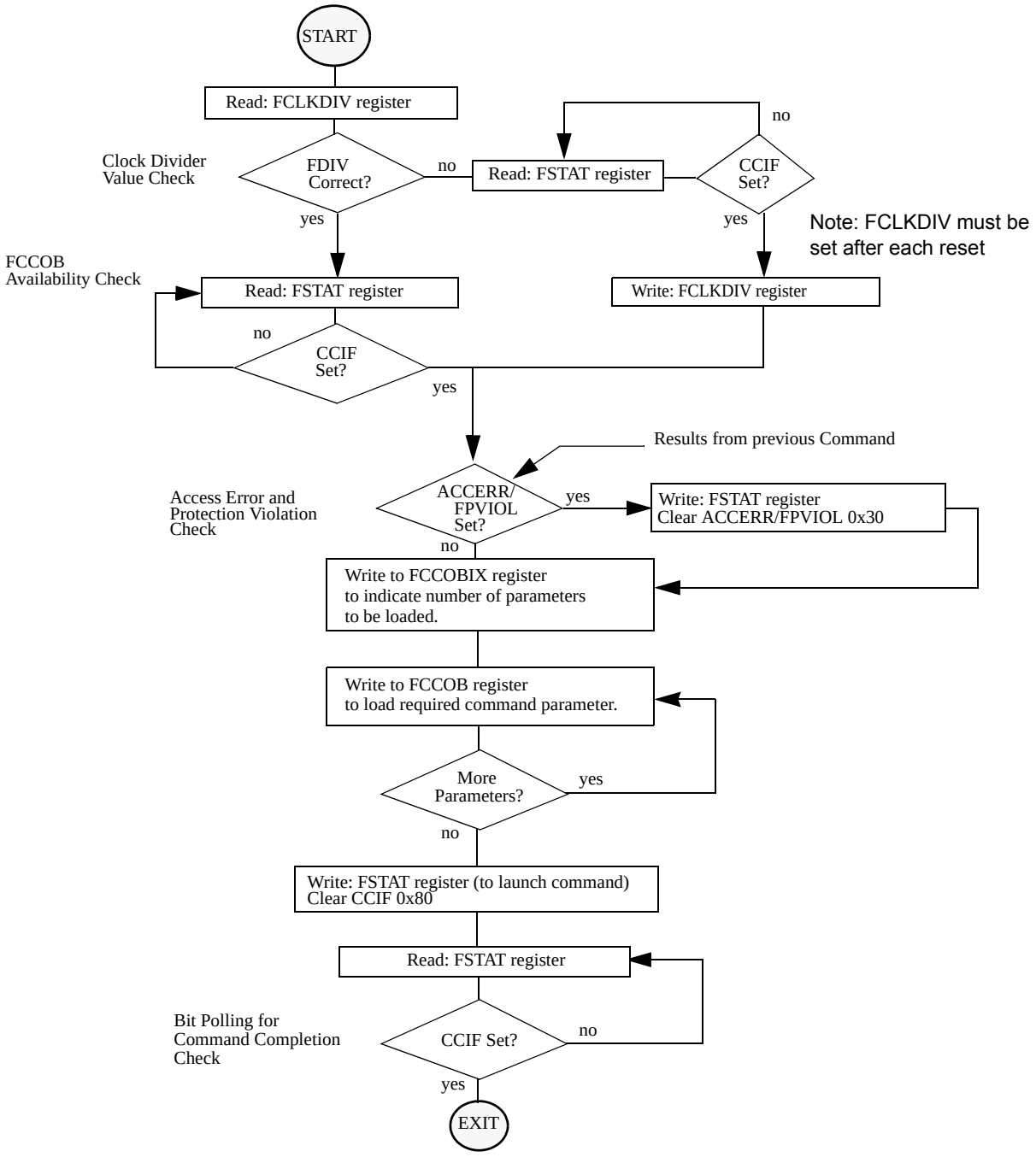


Figure 20-30. Generic Flash Command Write Sequence Flowchart

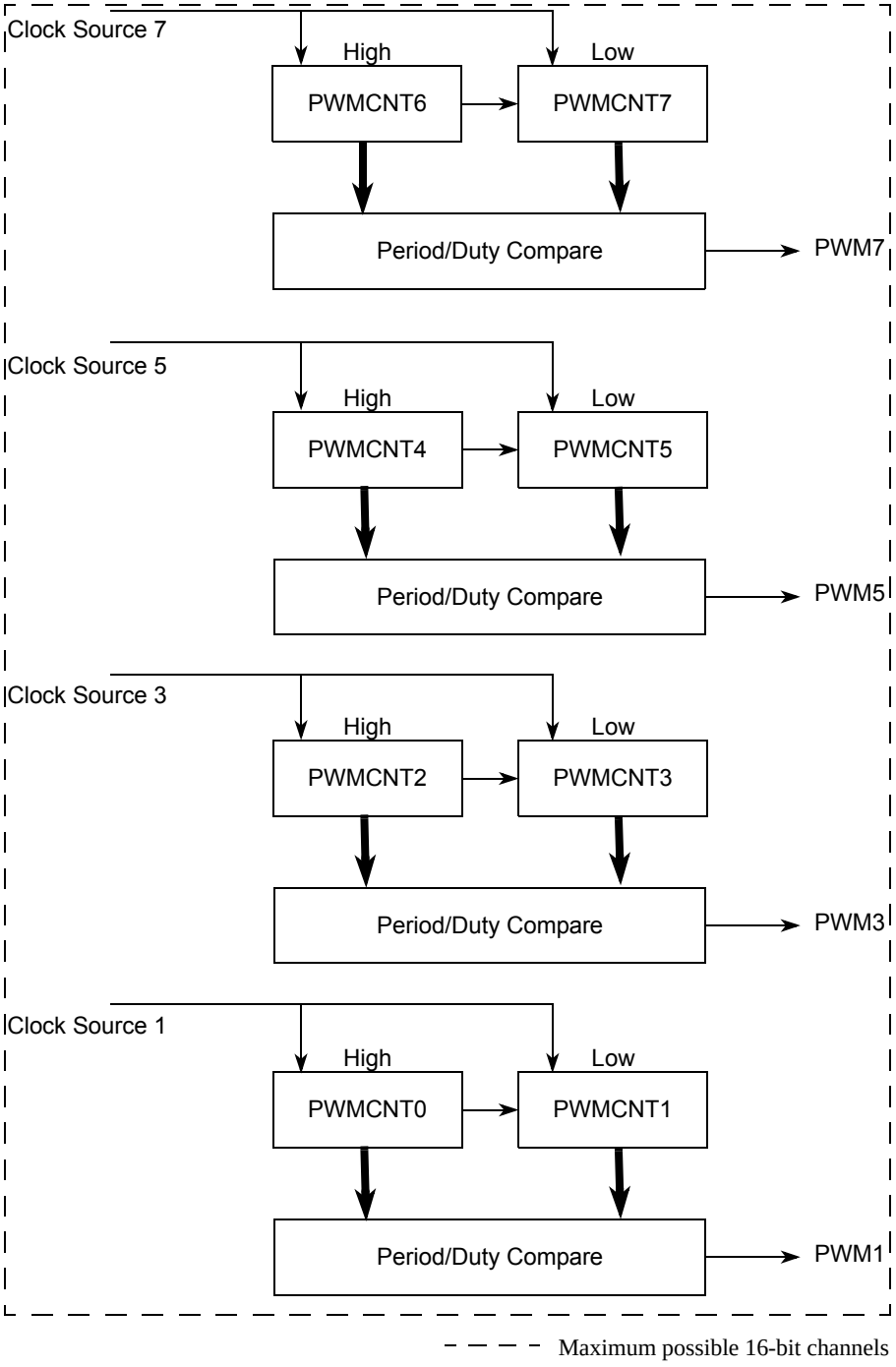


Figure 22-21. PWM 16-Bit Mode

Once concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low order PWMEx bit. In this case, the high order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

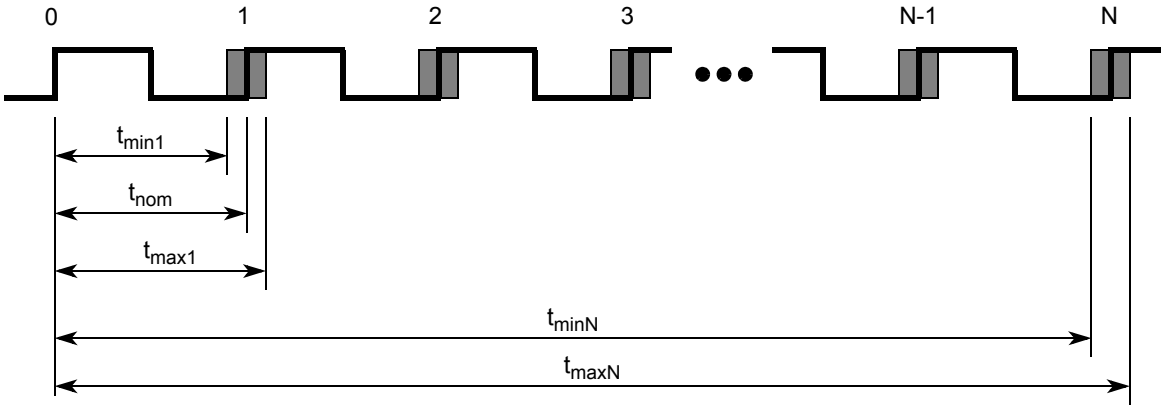


Figure B-1. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

The following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N(POSTDIV + 1)}}$$

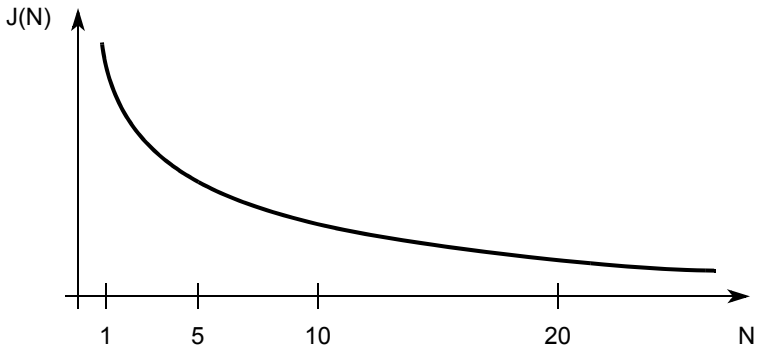


Figure B-2. Maximum Bus Clock Jitter Approximation (N = number of bus cycles)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0412	TIM1TC1H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0413	TIM1TC1L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0414– 0x042B	Reserved	R W								
0x042C	TIM1OCPD	R W							OCPD1	OCPD0
0x042D	Reserved	R W								
0x042E	TIM1PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x042F	Reserved	R W								

M.9 0x0480-0x04AF PWM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0480	PWME	R W	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
0x0481	PWMPOL	R W	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
0x0482	PWMCLK	R W	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
0x0483	PWMPRCLK	R W	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
0x0484	PWMCAE	R W	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
0x0485	PWMCTL	R W	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
0x0486	PWMCLKAB	R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
0x0487	RESERVED	R W	0	0	0	0	0	0	0	0
0x0488	PWMSCLA	R W	Bit 7	6	5	4	3	2	1	Bit 0

M.15 0x06A0-0x06BF GDU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x06A0	GDUE	R	GWP	0	0	GCS1E	GBOE	GCS0E	GCPE	GFDE
		W								
0x06A1	GDUCTR	R	GHHDLVL	GVLSLVL (1)	GBKTIM2[3:0]				GBKTIM1[1:0]	
		W								
0x06A2	GDUIE	R	0	0	0	GOCIE[1:0]		GDSEIE	GHHDIE	GLVLSIE
		W								
0x06A3	GDUDSE	R	0	GDHSIF[2:0]			0	GDLSIF[2:0]		
		W								
0x06A4	GDUSTAT	R	GPHS[2:0]			GOCS[1:0]			GHHDS	GLVLSS
		W								
0x06A5	GDUSRC	R	0	GSRCHS[2:0]			0	GSRCLS[2:0]		
		W								
0x06A6	GDUF	R	GSUF	GHHDF	GLVLSF	GOCIF[1:0]		0	GHHDIF	GLVLSIF
		W								
0x06A7	GDUCLK1	R	0	GBOCD[4:0]					GBODC[1:0]	
		W								
0x06A8	GDUBCL	R	0	0	0	0	GBCL[3:0]			
		W								
0x06A9	GDUPHMUX	R	0	0	0	0	0	0	GPHMX[1:0]	
		W								
0x06AA	GDUCSO	R	0	GCSO1[2:0]			0	GCSO0[2:0]		
		W								
0x06AB	GDUDSLVL	R	GDSFHS[1]	GDSLHS[2:0]			GDSFLS[1]	GDSLLS[2:0]		
		W								
0x06AC	GDUPHL	R	0	0	0	0	0	GPHL[2:0]		
		W								
0x06AD	GDUCLK2	R	0	0	0	0	GCPCD[3:0]			
		W								
0x06AE	GDUOC0	R	GOCA0	GOCE0	0	GOCT0[4:0](2)				
		W								
0x06AF	GDUOC1	R	GOCA1	GOCE1	0	GOCT1[4:0](3)				
		W								
0x06B0	GDUCTR1(4)	R	GSRMOD[1:0]		0	0	0	0	0	TDEL
		W								