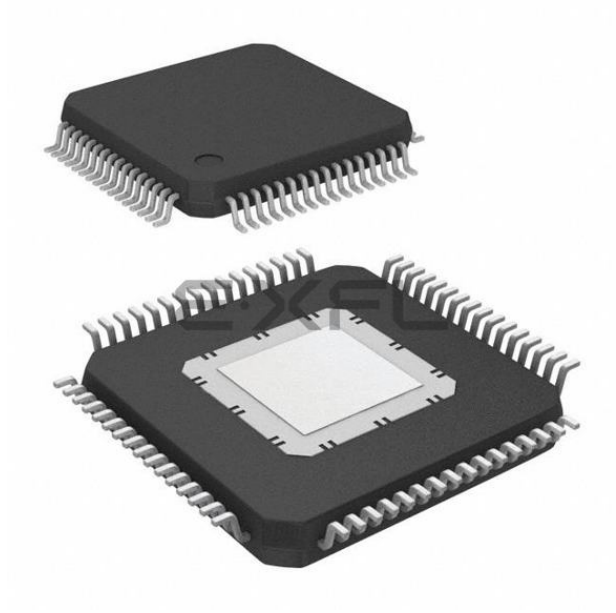


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f1mkhr

Chapter 2
Port Integration Module (S12ZVMPIMV3)

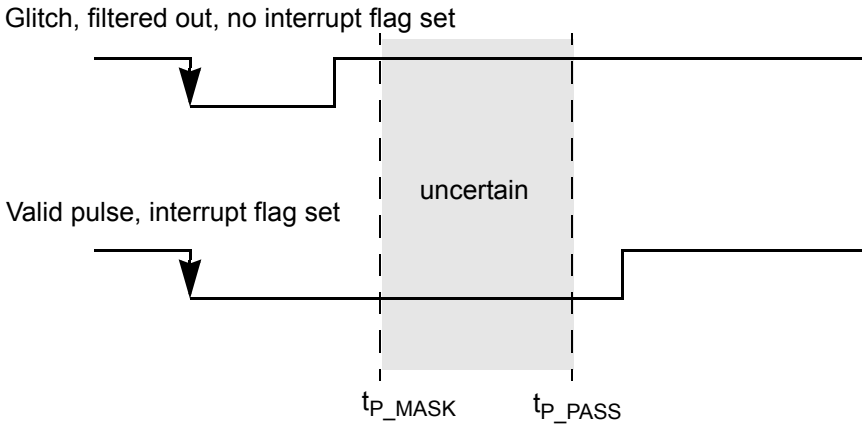


Figure 2-36. Interrupt Glitch Filter (here: active low level selected)

2.4.5 Over-Current Interrupt

In case of an over-current condition on PP0 (see Section 2.5.2, “Open Input Detection on HVI”) the over-current interrupt flag PIFP[OCIF1] asserts. This flag generates an interrupt if the enable bit PIEP[OCIE1] is set.

An asserted flag immediately forces the output pin low to protect the device. The flag must be cleared to re-enable the driver.

2.4.6 High-Voltage Input

A high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to V_{HVI}
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wakeup from stop (pin interrupts in run mode not available). Open input detection.

Figure 2-37 shows a block diagram of the HVI.

NOTE

The term stop mode (STOP) is limited to voltage regulator operating in reduced performance mode (RPM). Refer to “Low Power Modes” section in device overview.

input or the voltage divider can be bypassed (PTADIRL=1). Additionally in latter case the impedance converter in the ADC signal path can be used or bypassed in direct input mode (PTABYPL).

Out of reset the digital input buffer of the selected pin is disabled to avoid shoot-through current. Thus pin interrupts can only be generated if DIENL=1.

In stop mode (RPM) the digital input buffer is enabled only if DIENL=1 to support wakeup functionality.

Table 2-42 shows the HVI input configuration depending on register bits and operation mode.

Table 2-42. HVI Input Configurations

Mode	DIENL	PTAENL	Digital Input	Analog Input	Resulting Function
Run	0	0	off	off	Input disabled (Reset)
	0	1	off[1]	enabled	Analog input, interrupt not supported
	1	0	enabled	off	Digital input, interrupt supported
	1	1	off[1]	enabled	Analog input, interrupt not supported
Stop[2]	0	X	off	off	Input disabled, wakeup from stop not supported
	1	X	enabled	off	Digital input, wakeup from stop supported

1. Enabled if PTTEL=1 & PTADIRL=0)
2. The term “stop mode” is limited to voltage regulator operating in reduced performance mode (RPM; refer to “Low Power Modes” section in device overview). In any other case the HVI input configuration defaults to “run mode”. Therefore set PTAENL=0 before entering stop mode in order to generally support wakeup from stop.

NOTE

An external resistor R_{EXT_HVI} must always be connected to the high-voltage input to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

2.5 Initialization and Application Information

2.5.1 Port Data and Data Direction Register writes

It is not recommended to write PORTx/PTx and DDRx in a word access. When changing the register pins from inputs to outputs, the data may have extra transitions during the write access. Initialize the port data register before enabling the outputs.

2.5.2 Open Input Detection on HVI

The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type an external pull-down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull-down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

5.1.2 Features

The BDC includes these distinctive features:

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

5.1.3 Modes of Operation

S12 devices feature power modes (run, wait, and stop) and operating modes (normal single chip, special single chip). Furthermore, the operation of the BDC is dependent on the device security status.

5.1.3.1 BDC Modes

The BDC features module specific modes, namely disabled, enabled and active. These modes are dependent on the device security and operating mode. In active BDM the CPU ceases execution, to allow BDC system access to all internal resources including CPU internal registers.

5.1.3.2 Security and Operating mode Dependency

In device run mode the BDC dependency is as follows

- Normal modes, unsecure device
  General BDC operation available. The BDC is disabled out of reset.
- Normal modes, secure device
  BDC disabled. No BDC access possible.
- Special single chip mode, unsecure
  BDM active out of reset. All BDC commands are available.
- Special single chip mode, secure
  BDM active out of reset. Restricted command set available.

When operating in secure mode, BDC operation is restricted to allow checking and clearing security by mass erasing the on-chip flash memory. Secure operation prevents BDC access to on-chip memory other than mass erase. The BDC command set is restricted to those commands classified as Always-available.

Table 6-32 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, as matches based on instructions reaching the execution stage are data independent.

Table 6-32. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

6.3.2.17 Debug Comparator B Address Register (DBGBAH, DBGBAM, DBGBAL)

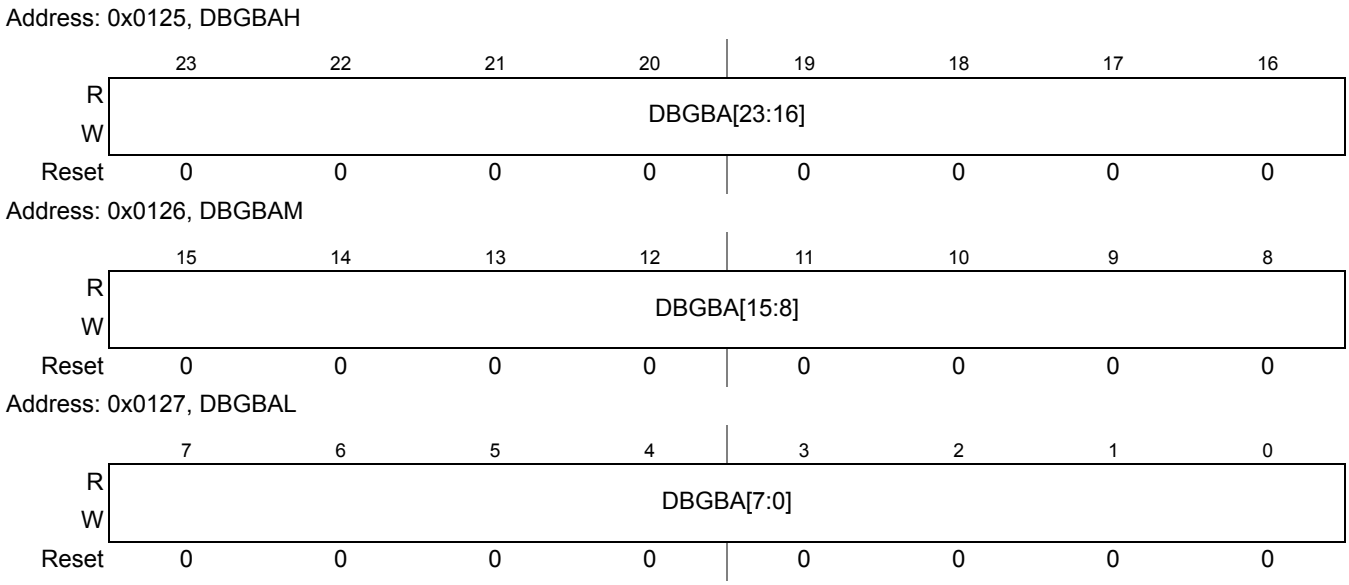


Figure 6-19. Debug Comparator B Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-33. DBGBAH, DBGBAM, DBGBAL Field Descriptions

Field	Description
23–16 DBGBA [23:16]	**Comparator Address Bits [23:16]**— These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one
15–0 DBGBA [15:0]	**Comparator Address Bits**[15:0]— These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

8.3.2.26 Reserved Register CPMUTEST2

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

Module Base + 0x001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

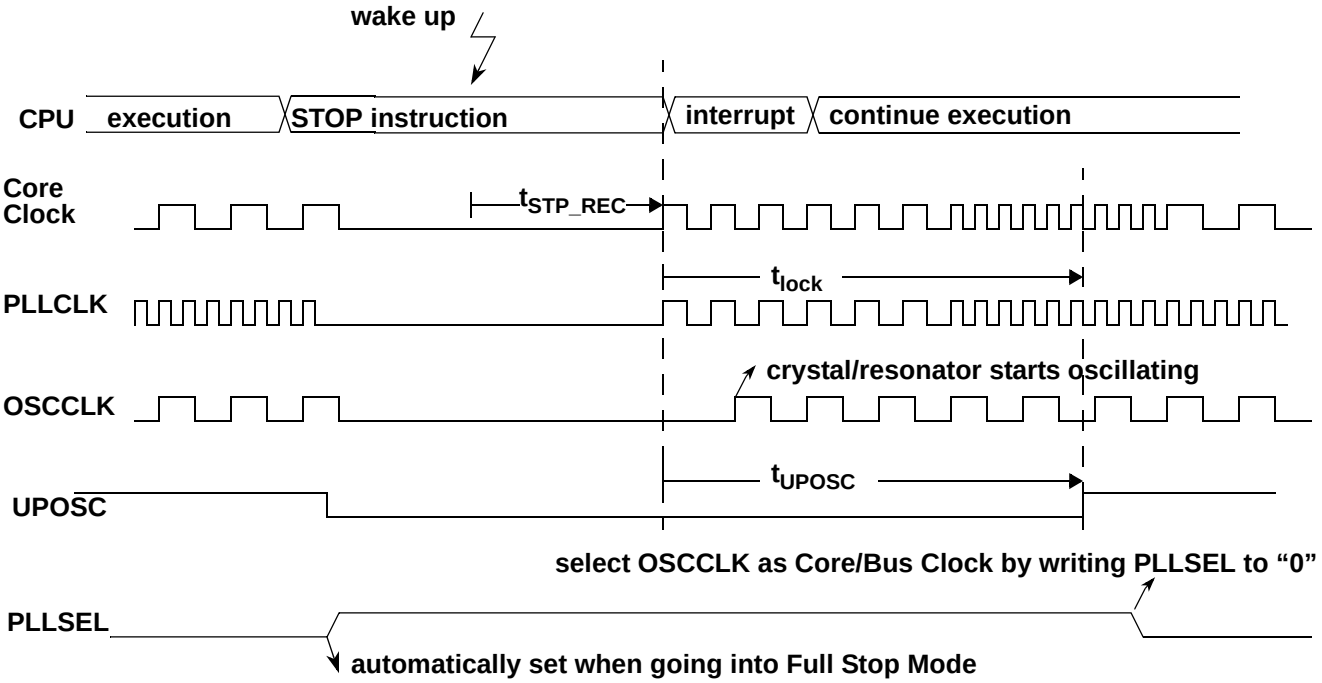
= Unimplemented or Reserved

Figure 8-37. Reserved Register CPMUTEST2

Read: Anytime

Write: Only in Special Mode

Figure 8-43. Full Stop Mode using Oscillator Clock as source of the Bus Clock



Depending on the COP configuration there might be a significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

9.5 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B_LBA.

9.5.1 Module Memory Map

Figure 9-3 gives an overview of all ADC12B_LBA registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ADCCTL_0	R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
		W								
0x0001	ADCCTL_1	R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
		W								
0x0002	ADCSTS	R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
		W								
0x0003	ADCTIM	R	0	PRS[6:0]						
		W								
0x0004	ADCFMT	R	DJM	0	0	0	0	SRES[2:0]		
		W								
0x0005	ADCFLWCTL	R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
		W								
0x0006	ADCEIE	R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
		W								
0x0007	ADCIE	R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
		W								
0x0008	ADCEiF	R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
		W								
0x0009	ADCIF	R	SEQAD_IF	CONIF_OIF	Reserved	0	0	0	0	0
		W								
0x000A	ADCCONIE_0	R	CON_IE[15:8]							
		W								
0x000B	ADCCONIE_1	R	CON_IE[7:1]							EOL_IE
		W								
0x000C	ADCCONIF_0	R	CON_IF[15:8]							
		W								
0x000D	ADCCONIF_1	R	CON_IF[7:1]							EOL_IF
		W								
0x000E	ADCIMDRI_0	R	CSL_IMD	RVL_IMD	0	0	0	0	0	0
		W								
0x000F	ADCIMDRI_1	R	0	0	RIDX_IMD[5:0]					
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 1 of 3)

Table 13-23. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 13-23. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

13.3.3 Programmer’s Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 13.3.2.1, “MSCAN Control Register 0 (CANCTL0)”).

The time stamp register is written by the MSCAN. The CPU can only read these registers.

mechanism” above. The only difference is, that during an async reload event the error interrupt flags PTUROIF and TGxREIF are not generated.

14.4.5 Interrupts and error handling

This section describes the interrupts generated by the PTU module and their individual sources, Vector addresses and interrupt priority are defined by MCU level.

Table 14-22. PTU Interrupt Sources

Module Interrupt Sources	Local Enable
PTU Reload Overrun Error	PTUIEH[PTUROIE]
TG0 Error	PTUIEL[TG0AEIE,TG0REIE,TG0TEIE]
TG1 Error	PTUIEL[TG1AEIE,TG1REIE,TG1TEIE]
TG0 Done	PTUIEL[TG0DIE]
TG1 Done	PTUIEL[TG1DIE]

14.4.5.1 PTU Double Bit ECC Error

If one trigger generator reads trigger values from the memory which contains double bit ECC errors then the PTUDEEF is set. These read data are ignored and the execution of both trigger generators is stopped until the PTUDEEF flag was cleared. To make sure the trigger generator starts in a define state it is required to execute follow sequence:

1. disable both trigger generators
2. configure the PTU if required
3. clear the PTUDEEF
4. enable the desired trigger generators

14.4.5.2 PTU Reload Overrun Error

If the PTULDOK bit is not set during the reload event then the PTUROIF bit is set. If enabled (PTUROIE is set) an interrupt is generated. For more information see Section 14.4.3, “Reload mechanism”. During an async reload event the PTUROIF interrupt flag is not set.

14.4.5.3 Trigger Generator Memory Access Error

The trigger generator memory access error flag (TGxAEIF) is set if the used read address is outside the accessible memory address area; see the MMC section for the supported memory area. The loaded trigger values are ignored and the execution of this trigger list is stopped until the next reload event. If enabled (TGxAEIE is set) an interrupt will be generated.

14.4.5.4 Trigger Generator Reload Error

The trigger generator reload error flag (TGxREIF) is set if a new reload event occurs before the trigger generator reaches the EOL symbol or the maximum number of generated triggers. Independent of this

Table 15-2. Glossary of Terms

Term	Definition
PWM active state Normal output Positive polarity	PWM logic level high causing external power device to conduct
PWM inactive or disabled state Inverted output Negative polarity	PWM logic level low causing external power device not to conduct
PWM clock	Clock supplied to PWM and deadtime generators. Based on core clock. Rate depends on prescaler setting.
PWM cycle	PWM period determined by modulus register and PWM clock rate. Note the differences in edge- or center-aligned mode.
PWM reload cycle	A.k.a. control cycle. Determined by load frequency which is 1 to n-times the PWM cycle. PWM reload cycle triggered double-buffered registers take effect at the next PWM reload event.
Commutation cycle	For 6-step motor control only. Started by an event external to the PMF module (async_event). This may be a delayed Hall effect or back-EMF zero crossing event determining the rotor position. Commutation cycle triggered double-buffered registers take effect at the next commutation event and optionally the PWM counters are restarted.
Index *x*	Related to time bases. *x* = A, B or C
Index *n*	Related to PWM channels. *n* = 0, 1, 2, 3, 4, or 5
Index *m*	Related to fault inputs. *m* = 0, 1, 2, 3, 4, or 5

15.1 Introduction

NOTE

Device reference manuals specify which module version is integrated on the device. Some reference manuals support families of devices, with device dependent module versions. This chapter describes the superset. The feature differences are listed in Table 15-3.

Table 15-3. Comparison of PMF15B6C Module Versions

Feature	V3	V4
Write protection (WP) on REV1-0 bits	not available	available
Ability to read the PWM output value through PMFOUTB register	not available	available

The Pulse width Modulator with Fault protection (PMF) module can be configured for one, two, or three complementary pairs. For example:

- One complementary pair and four independent PWM outputs
- Two complementary pairs and two independent PWM outputs

NOTE

Because of the equals-comparator architecture of this PMF, the modulus equals zero case is considered illegal in center-aligned mode. Therefore, the modulus register does not return to zero, and a modulus value of zero will result in waveforms inconsistent with the other modulus waveforms. If a modulus of zero is loaded, the counter will continually count down from 0x7FFF. This operation will not be tested or guaranteed. Consider it illegal. However, the deadtime constraints and fault conditions will still be guaranteed.

In edge-aligned mode, the PWM counter is an up counter. The PWM output resolution is one core clock cycle.

PWM period = PWM modulus × PWM clock period ***Eqn. 15-5***

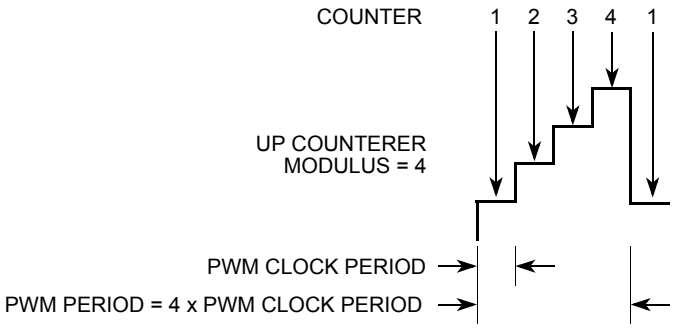


Figure 15-45. Edge-Aligned PWM Period

NOTE

In edge-aligned mode the modulus equals zero and one cases are considered illegal.

15.4.3.3 Duty Cycle

The signed 16-bit number written to the PMF value registers (PMFVAL*n*) is the pulse width in PWM clock periods of the PWM generator output (or period minus the pulse width if CINV*n*=1).

$$\text{Duty cycle} = \frac{\text{PMFVAL}}{\text{PMFMOD}} \times 100$$

NOTE

A PWM value less than or equal to zero deactivates the PWM output for the entire PWM period. A PWM value greater than or equal to the modulus activates the PWM output for the entire PWM period when CINV*n*=0, and vice versa if CINV*n*=1.

16.4.6 Receiver

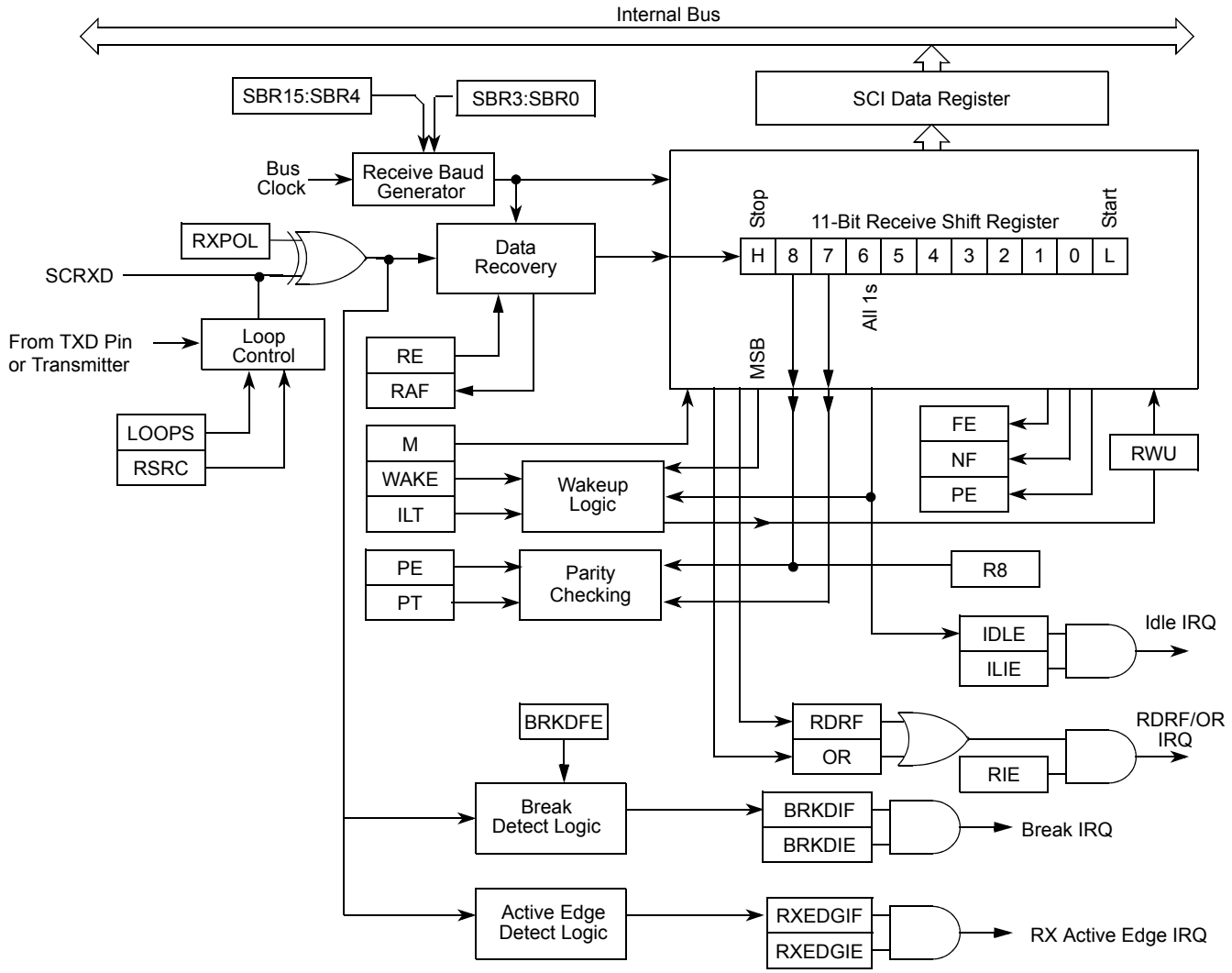


Figure 16-20. SCI Receiver Block Diagram

16.4.6.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

16.4.6.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

The CPOL clock polarity control bit specifies an active high or low clock and has no significant effect on the transmission format.

The CPHA clock phase control bit selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

17.4.3.2 CPHA = 0 Transfer Format

The first edge on the SCK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. In some peripherals, the first bit of the slave's data is available at the slave's data out pin as soon as the slave is selected. In this format, the first SCK edge is issued a half cycle after $\overline{SS}$ has become low.

A half SCK cycle later, the second edge appears on the SCK line. When this second edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the shift register, depending on LSBFE bit.

After this second edge, the next bit of the SPI master data is transmitted out of the serial data output pin of the master to the serial input pin on the slave. This process continues for a total of 16 edges on the SCK line, with data being latched on odd numbered edges and shifted on even numbered edges.

Data reception is double buffered. Data is shifted serially into the SPI shift register during the transfer and is transferred to the parallel SPI data register after the last bit is shifted in.

After $2n^1$ (last) SCK edges:

- Data that was previously in the master SPI data register should now be in the slave data register and the data that was in the slave data register should be in the master.
- The SPIF flag in the SPI status register is set, indicating that the transfer is complete.

Figure 17-12 is a timing diagram of an SPI transfer where CPHA = 0. SCK waveforms are shown for CPOL = 0 and CPOL = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave and the MOSI signal is the output from the master. The $\overline{SS}$ pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

1. n depends on the selected transfer width, please refer to Section 17.3.2.2, "SPI Control Register 2 (SPICR2)

Table 18-9. GDUF Register Field Descriptions

Field	Description
1 GHHDIF	GDU High V_{HD} Supply Interrupt Flag— The interrupt flag is set by hardware if GHHDF is set or if GHHDS is cleared. If the GHHDIE bit is set an interrupt is requested. Writing a logic “1” to the bit field clears the flag.
0 GLVLSIF	GDU Low VLS Supply Interrupt Flag— The interrupt flag is set by hardware if GLVLSF is set or GLVLSS is cleared. If the GLVLSIE bit is set an interrupt is requested.Writing a logic “1” to the bit field clears the flag.

NOTE

The purpose of the GSUF flag is to allow dissipation of the energy in the motor coils through the low side FETs in case of short reset pulses whilst the motor is spinning.

18.3.2.8 GDU Clock Control Register 1 (GDUCLK1)

Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	GBOCD[4:0]					GBODC[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-10. GDU Clock Control Register 1 (GDUCLK1)

1. Read: Anytime
   Write: Anytime if GWP=0

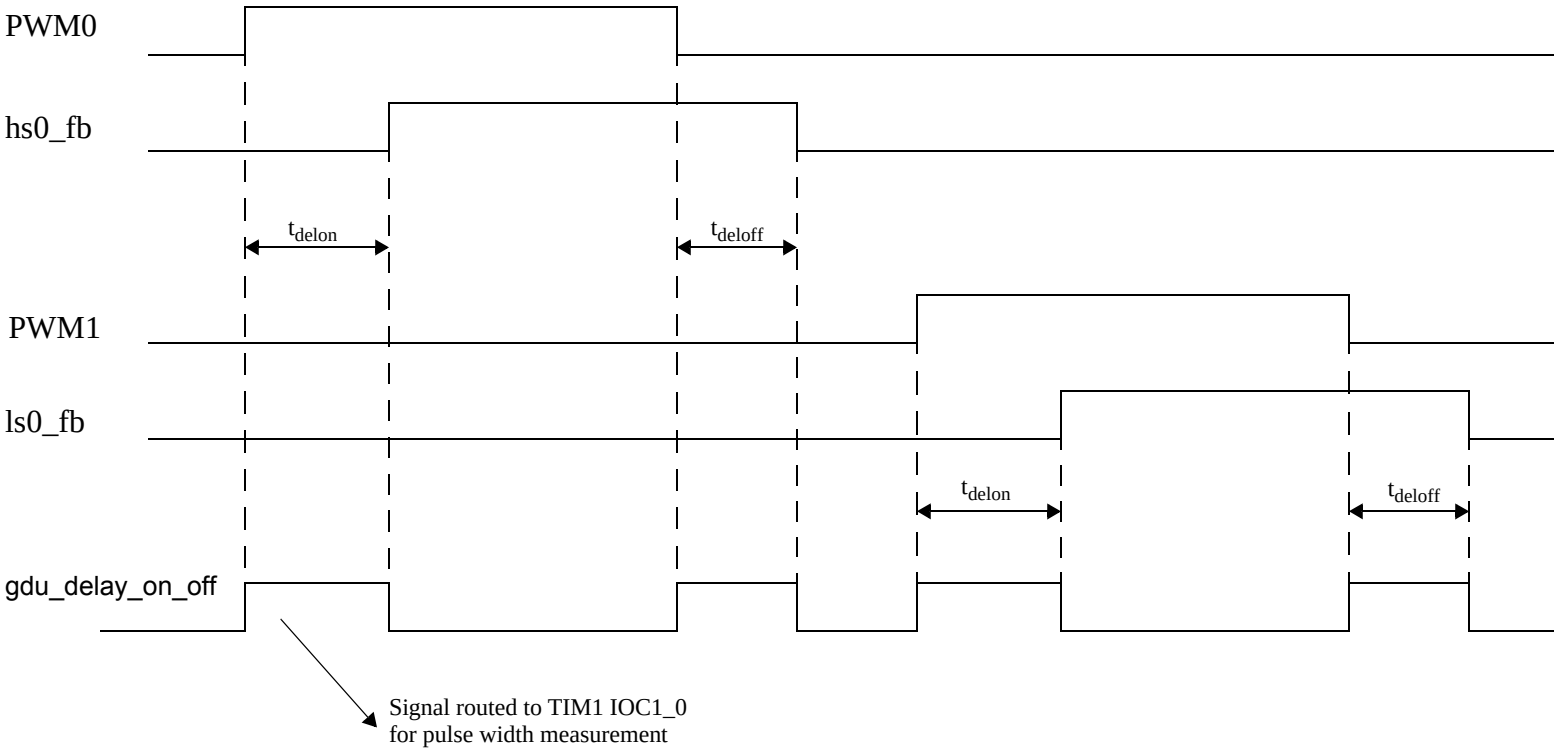
Table 18-10. GDUCLK1 Register Field Descriptions

Field	Description
6-2 GBOCD[4:0]	GDU Boost Option Clock Divider — These bits select the clock divider factor which is used to divide down the bus clock frequency f_{BUS} for the boost converter clock f_{BOOST}. These bits cannot be modified after GWP bit is set. See Table 18-11 for divider factors. See also Section 18.4.10, “Boost Converter
1-0 GBODC[1:0]	GDU Boost Option Clock Duty Cycle— These bits select the duty cycle of the boost option clock f_{boost}. For GBOCD[4]= 0 the duty cycle of the boost option clock is always 50%. These bits cannot be modified after GWP bit is set. 00 Duty Cycle = 50% 01 Duty Cycle = 25% 10 Duty Cycle = 50% 11 Duty Cycle = 75%

NOTE

The GBODC & GBOCD register bits must be set to the required value before GBOE bit is set. If a different boost clock frequency and duty cycle is required GBOE has to be cleared before new values to GBODC & GBOCD are written.

Figure 18-32. Measurement of GDU t_{delon} and t_{deloff}



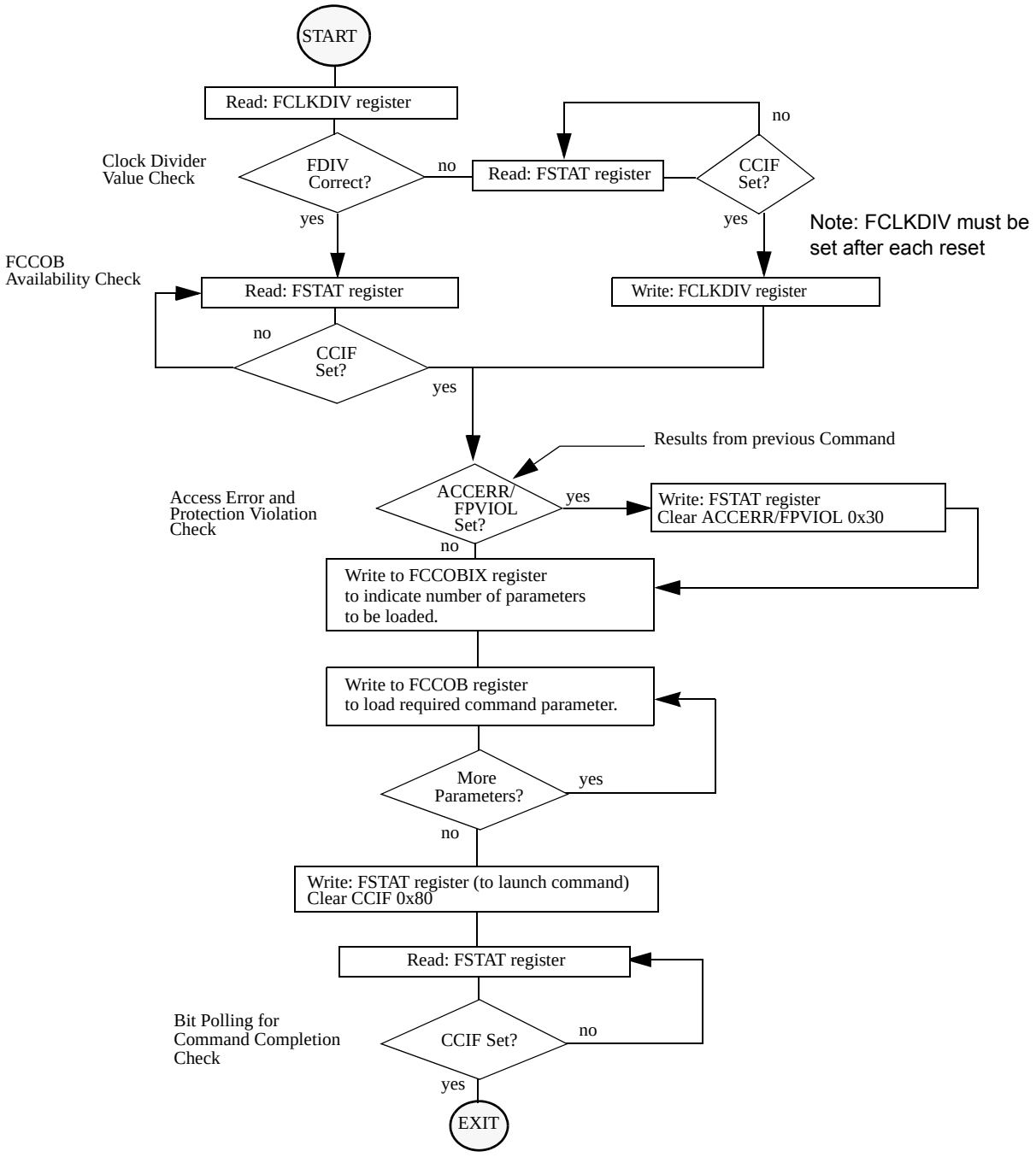


Figure 20-30. Generic Flash Command Write Sequence Flowchart

Module Base + 0x00006

	7	6	5	4	3	2	1	0
R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
Reset	0	0	0	0	0	0	0	0

Figure 22-9. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLKAB0 to PCLKAB7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 22-11. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PCLKAB7	Pulse Width Channel 7 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 7, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 7, as shown in Table 22-6.
6 PCLKAB6	Pulse Width Channel 6 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 6, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 6, as shown in Table 22-6.
5 PCLKAB5	Pulse Width Channel 5 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 5, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 5, as shown in Table 22-5.
4 PCLKAB4	Pulse Width Channel 4 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 4, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 4, as shown in Table 22-5.
3 PCLKAB3	Pulse Width Channel 3 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 3, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 3, as shown in Table 22-6.
2 PCLKAB2	Pulse Width Channel 2 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 2, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 2, as shown in Table 22-6.
1 PCLKAB1	Pulse Width Channel 1 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 1, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 1, as shown in Table 22-5.
0 PCLKAB0	Pulse Width Channel 0 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 0, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 0, as shown in Table 22-5.

4. At temperatures above 25°C the current may be naturally limited by the driver, in this case the limitation circuit is not engaged and the flag is not set.

D.2 Dynamic Electrical Characteristics

Table D-2. Dynamic electrical characteristics of the LIN/HV PHY

Characteristics noted under conditions 5.5V ≤ V_{LINSUP} ≤ 18 V unless otherwise noted(1) (2) (3). Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.							
Num	**C**	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Minimum duration of wake-up pulse generating a wake-up interrupt	t_{WUFR}	56	72	120	µs
2		TxD-dominant timeout (in IRC clock periods) (4)	t_{DTLIM}	16388	—	16389	t_{IRC}
3		Propagation delay of receiver	t_{rx_pd}	—	—	6	µs
4		Symmetry of receiver propagation delay rising edge w.r.t. falling edge	t_{rx_sym}	-2	—	2	µs
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NOMINAL SLEW RATE - 20.0KBIT/S							
5		Rising/falling edge time (min to max / max to min)	t_{rise}	—	6.5	—	µs
6		Over-current masking window (IRC trimmed at 1MHz)	t_{OCLIM}	15	—	16	µs
7	M	Duty cycle 1 $T_{HRec(max)} = 0.744 \times V_{LINSUP}$ $T_{HDom(max)} = 0.581 \times V_{LINSUP}$ V_{LINSUP} = 5.5V...18V t_{Bit} = 50us $D1 = t_{Bus\_rec(min)} / (2 \times t_{Bit})$	D1	0.396 (5)	—	—	
8	M	Duty cycle 2 $T_{HRec(min)} = 0.422 \times V_{LINSUP}$ $T_{HDom(min)} = 0.284 \times V_{LINSUP}$ V_{LINSUP} = 5.5V...18V t_{Bit} = 50us $D2 = t_{Bus\_rec(max)} / (2 \times t_{Bit})$	D2	—	—	0.581[5]	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4KBIT/S							
9		Rising/falling edge time (min to max / max to min)	t_{rise}	—	13	—	µs
10		Over-current masking window (IRC trimmed at 1MHz)	t_{OCLIM}	31	—	32	µs
11	M	Duty cycle 3 $T_{HRec(max)} = 0.778 \times V_{LINSUP}$ $T_{HDom(max)} = 0.616 \times V_{LINSUP}$ V_{LINSUP} = 5.5V...18V t_{Bit} = 96us $D3 = t_{Bus\_rec(min)} / (2 \times t_{Bit})$	D3	0.417[5]	—	—	

M.20 0x0780-0x0787 SPI0

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0780	SPI0CR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x0781	SPI0CR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x0782	SPI0BR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x0783	SPI0SR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x0784	SPI0DRH	R	R15	R14	R13	R12	R11	R10	R9	R8
		W	T15	T14	T13	T12	T11	T10	T9	T8
0x0785	SPI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0
0x0786	Reserved	R								
		W								
0x0787	Reserved	R								
		W								

M.21 0x0800–0x083F CAN0

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0800	CAN0CTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0801	CAN0CTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		W								
0x0802	CAN0BTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0803	CAN0BTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0804	CAN0RFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x0805	CAN0RIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x0806	CAN0TFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x0807	CAN0TIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								
0x0808	CAN0TARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		W								
0x0809	CAN0TAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		W								