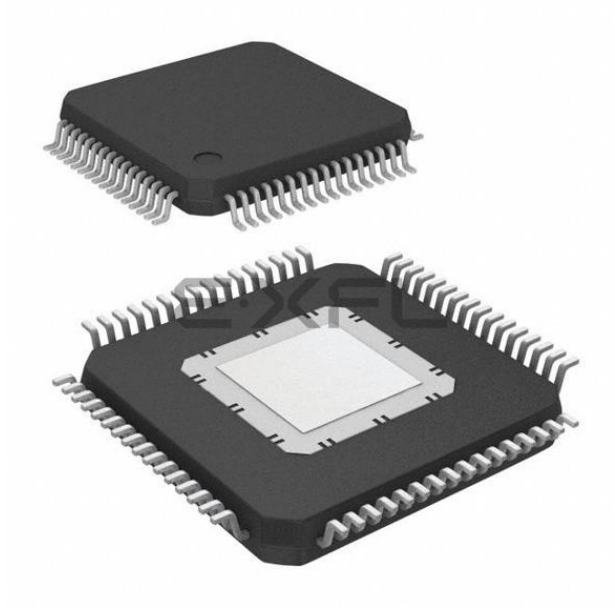


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f1vkh

1.7.3.7 VDDS1 — 5V Supply Pin For External Devices (ZVMC256 Only)

This provides a regulated, short circuit protected, 5V supply for external devices. This is the output voltage of the external bipolar, whose base current is supplied by BCTLS1. It is fed back to the MCU for regulation.

1.7.3.8 BCTLS1 (ZVMC256 Only)

BCTLS1 provides the base current of an external bipolar that supplies VDDS1. If not used BCTLS1 should be left unconnected.

1.7.3.9 SNPS1 (ZVMC256 Only)

SNPS1 is the sense input associated with the VDDS1 regulator. The voltage regulator uses it to detect a short circuit or over current condition.

1.7.3.10 VDDS2 — 5V Supply Pin For External Devices (ZVMC256 Only)

This provides a regulated, short circuit protected, 5V supply for external devices. This is the output voltage of the external bipolar, whose base current is supplied by BCTLS2. It is fed back to the MCU for regulation.

1.7.3.11 BCTLS2 (ZVMC256 Only)

BCTLS2 provides the base current of an external bipolar that supplies VDDS2. If not used BCTLS2 should be left unconnected.

1.7.3.12 SNPS2 (ZVMC256 Only)

SNPS2 is the sense input associated with the VDDS2 regulator. The voltage regulator uses it to detect a short circuit or over current condition.

1.7.4 Package and Pinouts

The following package options are offered.

- 80LQFP-EP (exposed pad) with internal CANPHY and CAN VREG.
- 64LQFP-EP (exposed pad) with internal LINPHY or HV physical interface.
- 64LQFP-EP (exposed pad) with CAN VREG to support a low cost external CANPHY.
- 48LQFP-EP (exposed pad) with internal LINPHY or HV physical interface

The exposed pad must be connected to a grounded contact pad on the PCB.

The exposed pad has an electrical connection within the package to VSSFLAG (VSSX die connection).

The pin out details are shown in the following diagrams. Signals in brackets denote routing options.

6. Map the sine/cosine input signals to ADC input channels.
7. Configure the EVDD1 pin as output.
8. Optionally use GDU phase comparators for zero crossing detection to correct dead time distortion.
9. Fetch targeted motor speed parameter from external source (e.g. SCI)
10. Configure PMF period and duty cycle.
11. Start motor by applying startup algorithm.
12. Sample the sine/cosine voltages periodically based on PWM cycle to determine motor position.
13. Use FOC algorithm to determine back EMF and motor speed.

Figure 1-17. PMSM Sine/Cosine Control Loop Configuration

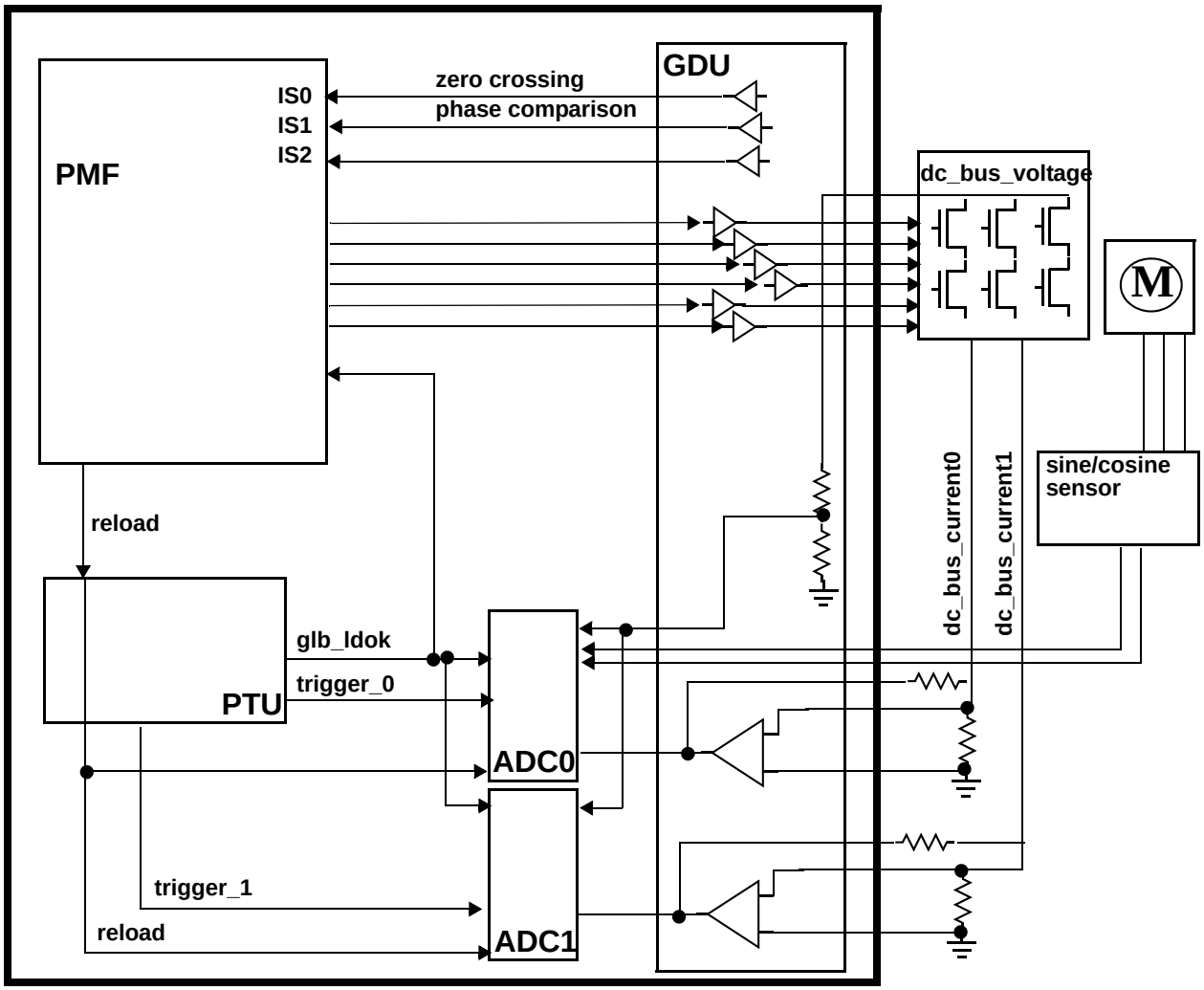


Table 2-15. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select edge sensitive only** — 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin are detected anytime when IRQE=1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ configured for low level recognition
6 IRQEN	**IRQ enable** — 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

2.3.2.6 PIM Miscellaneous Register (PIMMISC)

Address 0x020A Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	OCPE1	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-8. PIM Miscellaneous Register (PIMMISC)

1. Read: Anytime
   Write:Anytime

Table 2-16. PIM Miscellaneous Register Field Descriptions

Field	Description
1 OCPE1	Over-Current Protection Enable — Activate over-current detector on PP0 Refer to Section 2.5.3, “Over-Current Protection on EVDD1” 1 PP0 over-current detector enabled 0 PP0 over-current detector disabled

2.3.2.7 Reserved Register

Address 0x020D Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
W								
Reset	x	x	x	x	x	x	x	x

Figure 2-9. Reserved Register

Chapter 3
Memory Mapping Control (S12ZMMCV1)

Table 3-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	27 Jul 2012		Corrected Table 3-9
V01.04	27 Jul 2012		Added feature tags
V01.05	6 Aug 2012		Fixed wording
V01.06	12 Feb 2013	Figure 3-8 3.3.2.2/3-162	• Changed “KByte:to “KB” • Corrected the description of the MMCECH/L register

3.1 Introduction

The S12ZMMC module controls the access to all internal memories and peripherals for the S12ZCPU, and the S12ZBDC module. It also provides access to the RAM for ADCs and the PTU module. The S12ZMMC determines the address mapping of the on-chip resources, regulates access priorities and enforces memory protection. Figure 3-1 shows a block diagram of the S12ZMMC module.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0147	DBGDAL	R W	DBGDA[7:0]							
0x0148- 0x017F	Reserved	R	0	0	0	0	0	0	0	0
		W								

Figure 6-2. Quick Reference to DBG Registers

6.3.2 Register Descriptions

This section consists of the DBG register descriptions in address order. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, and TRIG

6.3.2.1 Debug Control Register 1 (DBGC1)

Address: 0x0100

	7	6	5	4	3	2	1	0
0x0100	ARM	0 TRIG	reserved	BDMBP	BRKCPU	reserved	EEVE	
Reset	0	0	0	0	0	0	0	0

Figure 6-3. Debug Control Register (DBGC1)

Read: Anytime

Write: Bit 7 Anytime with the exception that it cannot be set if PTACT is set. An ongoing profiling session must be finished before DBG can be armed again.
Bit 6 can be written anytime but always reads back as 0.
Bits 5:0 anytime DBG is not armed and PTACT is clear.

NOTE

On a write access to DBGC1 and simultaneous hardware disarm from an internal event, the hardware disarm has highest priority, clearing the ARM bit and generating a breakpoint, if enabled.

NOTE

When disarming the DBG by clearing ARM with software, the contents of bits[5:0] are not affected by the write, since up until the write operation, ARM = 1 preventing these bits from being written. These bits must be cleared using a second write if required.

transmission of the INFO byte starts when a line is complete. Whole bytes are always transmitted. The grey shaded bytes of Table 6-59 are not transmitted.

Figure 6-32. INFO byte encoding

Table 6-60. Profiling Format Encoding

INFO[3:0]	Line Format	Source	Description
0000	PTS	CPU	Initial CPU entry
0001	PTIB	CPU	Indexed jump with up to 31 direct COFs
0010	PTHF	CPU	31 direct COFs without indirect COF
0011	PTVB	CPU	Vector with up to 31 direct COFs
0111	PTW	CPU	Error (Error codes in INFO[7:4])
Others	Reserved	CPU	Reserved
INFO[7:4]	**Bit Name**		**Description**
INFO[7]	Reserved	CPU	Reserved
INFO[6]	TSOVF	CPU	Timestamp Overflow
INFO[5]	TBOVF	CPU	Trace Buffer Overflow
INFO[4]	TERM	CPU	Profiling terminated by disarming
Vector[7:0]	Vector[7:0]	CPU	Device Interrupt Vector Address [8:1]

6.4.6.4 Direct COF Compression

Each branch COF is stored to the trace buffer as a single bit (0=branch not taken, 1=branch taken) until an indirect COF (indexed jump, return, or interrupt) occurs. The branch COF entries are stored in the byte fields labelled “Direct” in Table 6-59. These entries start at byte1[0] and continue through to byte4[7], or until an indirect COF occurs, whichever occurs sooner. The entries use a format whereby the left most asserted bit is always the stop bit, which indicates that the bit to its right is the first direct COF and byte1[0] is the last COF that occurred before the indirect COF. This is shown in Table 6-61, whereby the Bytes 4 to 1 of the trace buffer are shown for 3 different cases. The stop bit field for each line is shaded.

In line0, the left most asserted bit is Byte4[7]. This indicates that all remaining 31 bits in the 4-byte field contain valid direct COF information, whereby each 1 represents branch taken and each 0 represents branch not taken. The stop bit of line1 indicates that all 30 bits to it’s right are valid, after the 30th direct COF entry, an indirect COF occurred, that is stored in bytes 7 to 5. In this case the bit to the left of the stop bit is redundant. Line2 indicates that an indirect COF occurred after 8 direct COF entries. The indirect COF address is stored in bytes 7 to 5. All bits to the left of the stop bit are redundant.

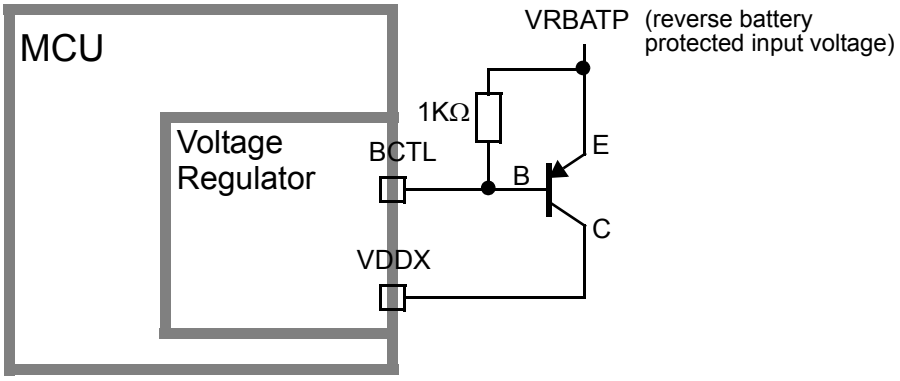


Figure 8-3. BCTL application example

8.2.10 BCTLC — Base Control Pin for external PNP for VDDC power domain

BCTLC is the ballast connection for the on chip voltage regulator for the VDDC power domain. It provides the base current of an external BJT (PNP) of the VDDC supply. An additional 1KΩ resistor between emitter and base of the BJT is required.

8.2.11 BCTLS1 — Base Control Pin for external PNP for VDDS1 power domain

BCTLS1 is the ballast connection for the on chip voltage regulator for the VDDS1 power domain. It provides the base current of an external BJT (PNP) of the VDDS1 supply. An additional 1KΩ resistor between emitter and base of the BJT is required.

Figure 8-4 shows an application example for the external BCTLS1 pin.

8.3.2.15 S12CPMU_UHV_V10_V6 COP Timer Arm/Reset Register (CPMUARMCOP)

This register is used to restart the COP time-out period.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	ARMCOP-Bit 7	ARMCOP-Bit 6	ARMCOP-Bit 5	ARMCOP-Bit 4	ARMCOP-Bit 3	ARMCOP-Bit 2	ARMCOP-Bit 1	ARMCOP-Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 8-20. S12CPMU_UHV_V10_V6 CPMUARMCOP Register

Read: Always reads $00

Write: Anytime

When the COP is disabled (CR[2:0] = “000”) writing to this register has no effect.

When the COP is enabled by setting CR[2:0] nonzero, the following applies:

Writing any value other than $55 or $AA causes a COP reset. To restart the COP time-out period write $55 followed by a write of $AA. These writes do not need to occur back-to-back, but the sequence ($55, $AA) must be completed prior to COP end of time-out period to avoid a COP reset. Sequences of $55 writes are allowed. When the WCOP bit is set, $55 and $AA writes must be done in the last 25% of the selected time-out period; writing any value in the first 75% of the selected period will cause a COP reset.

8.3.2.16 High Temperature Control Register (CPMUHTCTL)

The CPMUHTCTL register configures the temperature sense features.

Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	Reserved	0	VSEL	0	HTE	HTDS	HTIE	HTIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-21. High Temperature Control Register (CPMUHTCTL)

Read: Anytime

Write: VSEL, HTE, HTIE and HTIF are write anytime, HTDS is read only

8.3.2.26 Reserved Register CPMUTEST2

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

Module Base + 0x001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-37. Reserved Register CPMUTEST2

Read: Anytime

Write: Only in Special Mode

Table 8-33. CPMUVDDS Field Descriptions (continued)

Field	Description
3 SCS2IF	**Short circuit VDDS2 Interrupt Flag** — SCS2IF is set to 1 when SCS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS2IF causes an interrupt request. 0 No change in SCS2 bit. 1 SCS2 bit has changed.
2 SCS1IF	**Short circuit VDDS1 Interrupt Flag** — SCS1IF is set to 1 when SCS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS1IF causes an interrupt request. 0 No change in SCS1 bit. 1 SCS1 bit has changed.
1 LVS2IF	**Low-Voltage VDDS2 Interrupt Flag** — LVS2IF is set to 1 when LVDS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS2IF causes an interrupt request. 0 No change in LVDS2 bit. 1 LVDS2 bit has changed.
0 LVS1IF	**Low-Voltage VDDS1 Interrupt Flag** — LVS1IF is set to 1 when LVDS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS1IF causes an interrupt request. 0 No change in LVDS1 bit. 1 LVDS1 bit has changed.

Table 8-35. Reset Summary

Reset Source	Local Enable
Oscillator Clock Monitor Reset	OSCE Bit in CPMUOSC register and OMRE Bit in CPMUOSC2 register
COP Reset	CR[2:0] in CPMUCOP register

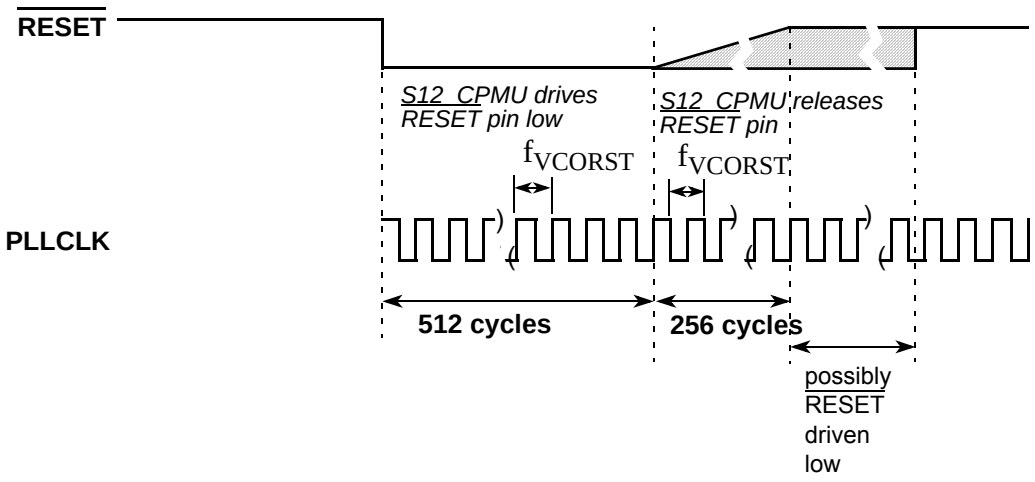
8.5.2 Description of Reset Operation

Upon detection of any reset of Table 8-35, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the $\overline{\text{RESET}}$ pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence.In case the $\overline{\text{RESET}}$ pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

NOTE

While System Reset is asserted the PLLCLK runs with the frequency f_{VCORST}.

Figure 8-45. RESET Timing



8.5.3 Oscillator Clock Monitor Reset

If the external oscillator is enabled (OSCE=1)and the oscillator clock monitor reset is enabled (OMRE=1), then in case of loss of oscillation or the oscillator frequency drops below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V10_V6 generates an Oscillator Clock Monitor Reset. In Full Stop Mode the external oscillator and the oscillator clock monitor are disabled.

8.5.4 PLL Clock Monitor Reset

In case of loss of PLL clock oscillation or the PLL clock frequency is below the failure assert frequency f_{PMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V10_V6 generates a PLL Clock Monitor Reset. In Full Stop Mode the PLL and the PLL clock monitor are disabled.

8.5.5 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus COP reset is generated.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit.

Depending on the COP configuration there might be a significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

Table 8-36 gives an overview of the COP condition (run, static) in Stop Mode depending on legal configuration and status bit settings:

Table 8-36. COP condition (run, static) in Stop Mode

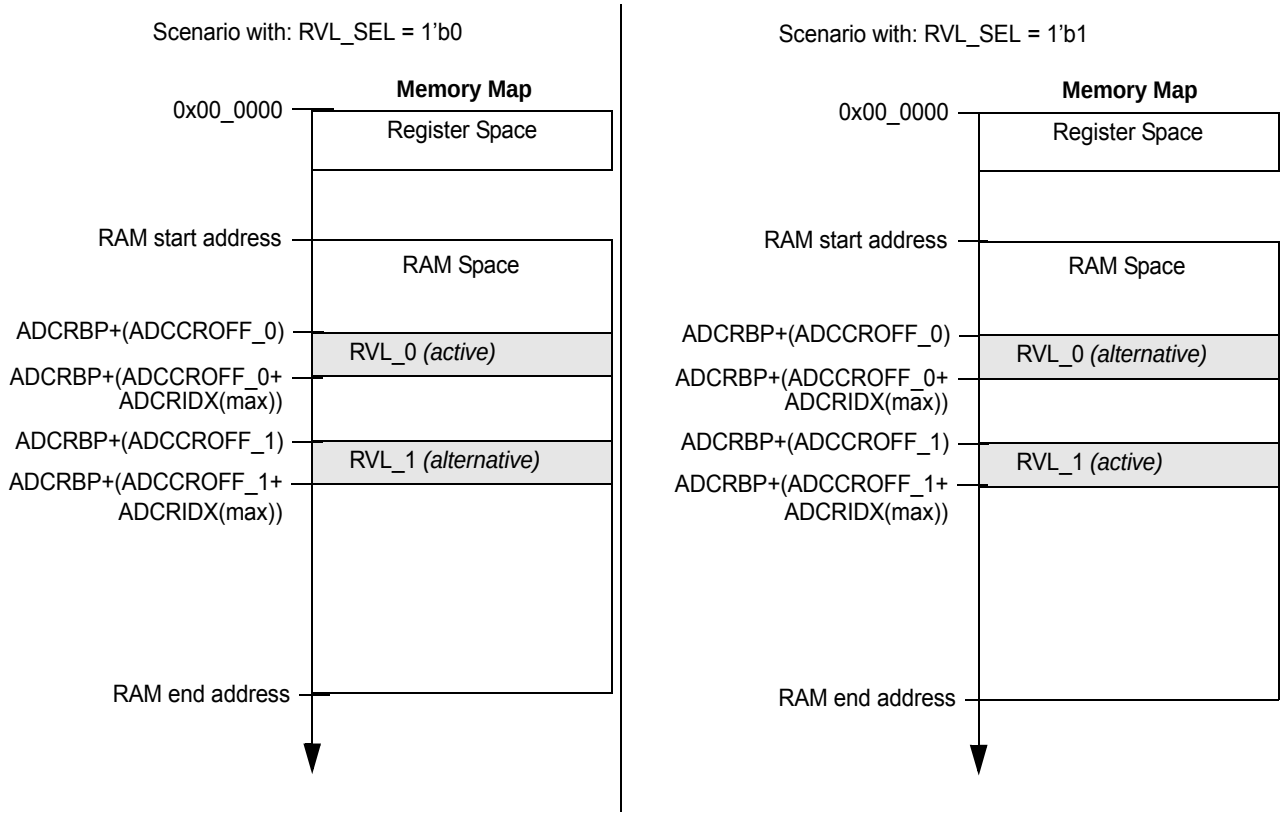
COPOSCSEL1	CSAD	PSTP	PCE	COPOSCSEL0	OSCE	UPOSC	COP counter behavior in Stop Mode (clock source)
1	0	x	x	x	x	x	Run (ACLK)
1	1	x	x	x	x	x	Static (ACLK)
0	x	1	1	1	1	1	Run (OSCCLK)
0	x	1	1	0	0	x	Static (IRCCLK)
0	x	1	1	0	1	x	Static (IRCCLK)
0	x	1	0	0	x	x	Static (IRCCLK)
0	x	1	0	1	1	1	Static (OSCCLK)
0	x	0	1	1	1	1	Static (OSCCLK)
0	x	0	1	0	1	x	Static (IRCCLK)
0	x	0	1	0	0	0	Static (IRCCLK)
0	x	0	0	1	1	1	Satic (OSCCLK)
0	x	0	0	0	1	1	Static (IRCCLK)
0	x	0	0	0	1	0	Static (IRCCLK)
0	x	0	0	0	0	0	Static (IRCCLK)

9.6.3.2.3 Introduction of the two Result Value Lists (RVLs)

The same list-based architecture as described above for the CSL has been implemented for the Result Value List (RVL) with corresponding address registers (ADCRBP, ADCCROFF_0/1, ADCRIDX).
The final address for conversion result storage is calculated by the sum of these registers (e.g.: ADCRBP+ADCCROFF_0+ADCRIDX or ADCRBP+ADCCROFF_1+ADCRIDX).
The RVL_BMOD bit selects if the RVL is used in double buffer or single buffer mode. In double buffer mode the RVL is swapped:

- Each time an “End Of List” command type got executed followed by the first conversion from top of the next CSL and related (first) result is about to be stored
- A CSL got aborted (bit SEQA=1’b1) and ADC enters idle state (becomes ready for new flow control events)

Using the RVL in double buffer mode the RVL is not swapped after exit from Stop Mode or Wait Mode with bit SWAI set. Hence the RVL used before entry of Stop or Wait Mode with bit SWAI set is overwritten after exit from the MCU Operating Mode (see also Section 9.3.1.2, “MCU Operating Modes).
Which list is actively used for the ADC conversion result storage is indicated by bit RVL_SEL. The register to define the RVL start addresses (ADCRBP) can be set to any even location of the system RAM area. It is the user’s responsibility to make sure that the different ADC lists do not overlap or exceed the system RAM area. The error flag IA_EIF will be set for accesses to ranges outside system RAM area and cause an error interrupt if enabled.



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 9-33. Result Value List Schema in Double Buffer Mode

13.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the MSCAN.

13.3.1 Module Memory Map

Figure 13-3 gives an overview on all registers and their individual bits in the MSCAN memory map. The *register address* results from the addition of *base address* and *address offset*. The *base address* is determined at the MCU level and can be found in the MCU memory map description. The *address offset* is defined at the module level.

The MSCAN occupies 64 bytes in the memory space. The base address of the MSCAN module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset.

The detailed register descriptions follow in the order they appear in the register map.

13.5 Initialization/Application Information

13.5.1 MSCAN initialization

The procedure to initially start up the MSCAN module out of reset is as follows:

1. Assert CANE
2. Write to the configuration registers in initialization mode
3. Clear INITRQ to leave initialization mode

If the configuration of registers which are only writable in initialization mode shall be changed:

1. Bring the module into sleep mode by setting SLPRQ and awaiting SLPAK to assert after the CAN bus becomes idle.
2. Enter initialization mode: assert INITRQ and await INITAK
3. Write to the configuration registers in initialization mode
4. Clear INITRQ to leave initialization mode and continue

13.5.2 Bus-Off Recovery

The bus-off recovery is user configurable. The bus-off state can either be left automatically or on user request.

For reasons of backwards compatibility, the MSCAN defaults to automatic recovery after reset. In this case, the MSCAN will become error active again after counting 128 occurrences of 11 consecutive recessive bits on the CAN bus (see the Bosch CAN 2.0 A/B specification for details).

If the MSCAN is configured for user request (BORM set in MSCAN Control Register 1 (CANCTL1)), the recovery from bus-off starts after both independent events have become true:

- 128 occurrences of 11 consecutive recessive bits on the CAN bus have been monitored
- BOHOLD in MSCAN Miscellaneous Register (CANMISC) has been cleared by the user

These two events may occur in any order.

Table 14-4. PTUC Register Field Descriptions

Field	Description
0 PTULDOK	**Load Okay** — When this bit is set by the software, this allows the trigger generator to switch to the alternative list and load the trigger time values at the next reload event from the new list. If the reload event occurs when the PTULDOK bit is not set then the trigger generator generates a reload overrun event and uses the previously used list. At the next reload event this bit is cleared by control logic. Write 0 is only possible if TG0EN and TG1EN is cleared. The PTULDOK can be used by other module as global load OK (glb_ldok).

18.3.2.17 GDU Control Register 1 (GDUCTR1)

Module Base + 0x0010 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GSRMOD1	GSRMOD0	0	0	0	0	0	TDEL
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-19. GDU Control Register 1 (GDUCTR1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-21. GDUCTR1 Register Field Descriptions

Field	Description
7 GSRMOD1	GDU Switched Reluctance Motor Mode 1 — This bit cannot be modified after GWP bit is set. This bit controls the routing of the LDx pins to the low-side desaturation comparators for switched reluctance motor. See Figure 18-23 0 HSx routed to low-side desaturation comparator 1 LDx routed to low-side desaturation comparator
6 GSRMOD0	GDU Switched Reluctance Motor Mode 0 — This bit cannot be modified after GWP bit is set. 0 BLDC mode. Don't allow HGx and LGx high at the same time. 1 SR mode. Allow HGx and LGx high at the same time.
0 TDEL	**t_{delon} / t_{deloff} Control** — This bit controls the parameters t_{delon} and t_{deloff}. It cannot be modified after GWP bit is set. This bit must be set to meet the min and max values for t_{delon} and t_{deloff} specified in the electrical specification. If this bit is cleared the values for t_{delon} and t_{deloff} are out of spec.

NOTE

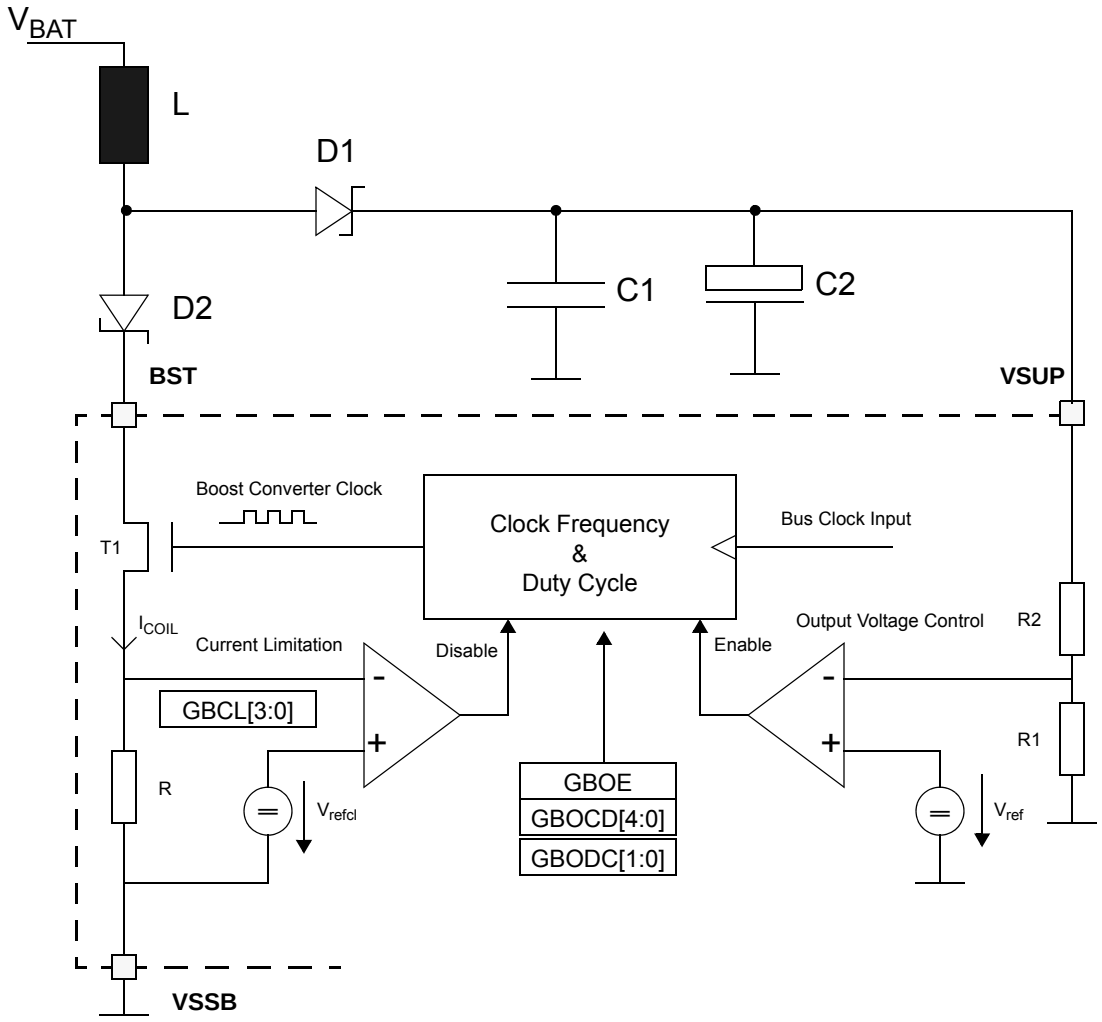
GDU Control Register 1 GDUCTR1 availability is defined at device level.

18.4.10 Boost Converter

The GDU module integrates the necessary hardware to build a boost converter with external components in case of low voltage condition. The external components needed are two Schottky diodes, one coil, and capacitors. See Figure 18-28. The boost converter clock which is driving the transistor T1 (see Figure 18-28) is derived from the bus clock. This clock can be divided down as described in Table 18-10. The boost converter also includes a circuit to limit the current through coil. This current limit can be adjusted with the bits GBCL[3:0] in the GDUBCL register. See GDU electrical parameters.

The output voltage of the boost converter on VSUP pin is divided down and compared with a reference voltage V_{ref} . As long as the divided voltage V_{VSUP} is below V_{ref} the boost converter clock is enabled assuming that GBOE (GDU Boost Option Enable) is set.

Figure 18-28. Boost Converter Option with external Components[1]



1. Diode D2 shown is optional if coil is connected behind reverse battery protection.

C.1.1 Factors Influencing Accuracy

Source resistance, source capacitance and current injection have an influence on the accuracy of the ADC .**Figure C-1.** A further factor is PortAD pins that are configured as output drivers.

C.1.1.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ADC accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ADC supply pins. Although internal design measures are implemented to minimize the effect of output driver noise, it is recommended to configure PortAD pins as outputs only for low frequency, low load outputs. The impact on ADC accuracy is load dependent and not specified. The values specified are valid under condition that no PortAD output drivers switch during conversion.

C.1.1.2 Source Resistance

Input pin leakage current in conjunction with the source resistance causes a voltage drop from the signal source to the ADC input. The maximum source resistance R_S results in an error (10-bit resolution) of less than 1/2 LSB (2.5 mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage induced error is acceptable, a larger source resistance of up to 10Kohm is allowed.

C.1.1.3 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB (10-bit resolution), then the external filter capacitor, $C_f \geq 1024 * (C_{INS}–C_{INN})$.

C.1.1.4 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (in 10-bit mode) for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL} unless the current is higher than specified as a disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as:

   $$V_{ERR} = K * R_S * I_{INJ}$$

   with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

C.1.1.5 VRH reference mapped to VDDS1 or VDDS2 (ZVMC256 only)

When using VDDS2 or VDDS1 as the VRH reference, the reference is impacted by a drop of between 4mV and 15mV across the internal short circuit protection switch. This can add an error of ≤ 3LSB (10-bit resolution).

C.1.2 ADC Accuracy

Table C-3. specifies the ADC conversion performance excluding any errors due to current injection, input capacitance and source resistance.

C.1.2.1 ADC Accuracy Definitions

For the following definitions see also **Figure C-2.**.
Differential non-linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The integral non-linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$