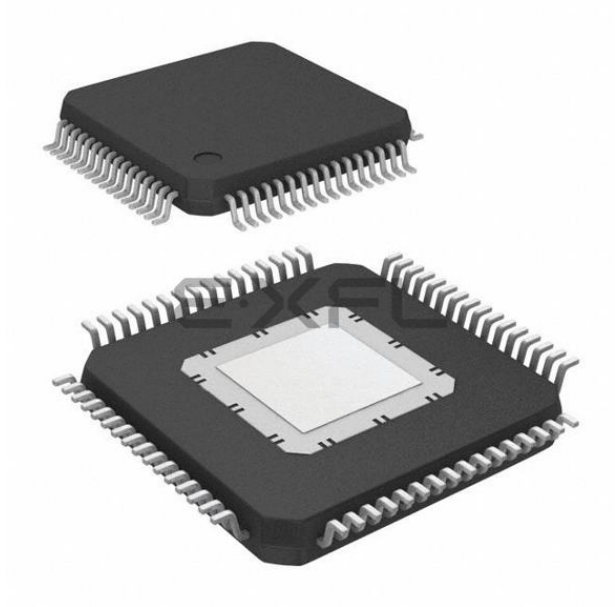

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f1wkh

1.9.1.2 Special Single-Chip Mode

This mode is used for debugging operation, boot-strapping, or security related operations. The background debug mode (BDM) is active on leaving reset in this mode

1.9.2 Debugging Modes

The background debug mode (BDM) can be activated by the BDC module or directly when resetting into Special Single-Chip mode. Detailed information can be found in the BDC module section.

Writing to internal memory locations using the debugger, whilst code is running or at a breakpoint, can change the flow of application code.

The MC9S12ZVM-Family supports BDC communication throughout the device Stop mode. During Stop mode, writes to control registers can alter the operation and lead to unexpected results. It is thus recommended not to reconfigure the peripherals during STOP using the debugger.

On the S12ZVML and S12ZVMC versions, the DBG module supports breakpoint, tracing and profiling features. At board level the profiling pins can use the same 6-pin connector typically used for the BDC BKGD pin. The connector pin mapping shown in Figure 1-7 is supported by device evaluation boards and leading development tool vendors.

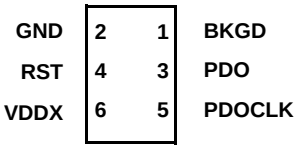


Figure 1-7. Standard Debug Connector Pin Mapping

1.9.3 Low Power Modes

The device has two dynamic-power modes (run and wait) and two static low-power modes stop and pseudo stop). For a detailed description refer to the CPMU section.

- Dynamic power mode: Run
  - Run mode is the main full performance operating mode with the entire device clocked. The user can configure the device operating speed through selection of the clock source and the phase locked loop (PLL) frequency. To save power, unused peripherals must not be enabled.
- Dynamic power mode: Wait
  - This mode is entered when the CPU executes the WAI instruction. In this mode the CPU does not execute instructions. The internal CPU clock is switched off. All peripherals can be active in system wait mode. For further power consumption the peripherals can individually turn off their local clocks. Asserting $\overline{\text{RESET}}$, $\overline{\text{XIRQ}}$, $\overline{\text{IRQ}}$, or any other interrupt that is not masked, either locally or globally by a CCR bit, ends system wait mode.
- Static power modes:
  Static power (Stop) modes are entered following the CPU STOP instruction unless an NVM command is active. When no NVM commands are active, the Stop request is acknowledged and

Field	Description
7-4 (MMCECL) ACC[3:0]	**Access Type Field** — The ACC[3:0] bits capture the type of memory access, which caused the access violation. The access type is captured in form of a 4 bit value which is assigned as follows: 0: none (no error condition detected) 1: opcode fetch 2: vector fetch 3: data load 4: data store 5-15: reserved
3-0 (MMCECL) ERR[3:0]	**Error Type Field** — The EC[3:0] bits capture the type of the access violation. The type is captured in form of a 4 bit value which is assigned as follows: 0: none (no error condition detected) 1: access to an illegal access 2: uncorrectable ECC error 3-15:reserved

The MMCEC register captures debug information about access violations. It is set to a non-zero value if a S12ZCPU access violation or an uncorrectable ECC error has occurred. At the same time this register is set to a non-zero value, access information is captured in the MMCPCn and MMCCCRn registers. The MMCECn, the MMCPCn and the MMCCCRn registers are not updated if the MMCECn registers contain a non-zero value. The MMCECn registers are cleared by writing the value 0xFFFF.

3.3.2.3 Captured S12ZCPU Condition Code Register (MMCCCRH, MMCCCRL)

Address: 0x0082 (MMCCCRH)

	7	6	5	4	3	2	1	0
R	CPUU	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Address: 0x0083 (MMCCCRL)

	7	6	5	4	3	2	1	0
R	0	CPUX	0	CPUI	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 3-6. Captured S12ZCPU Condition Code Register (MMCCCRH, MMCCCRL)

Read: Anytime

Write: Never

The procedure to change APICLK or APIR[15:0] is first to clear APIFE, then write to APICLK or APIR[15:0], and afterwards set APIFE.

The API Trimming bits ACLKTR[5:0] must be set so the minimum period equals 0.2 ms if stable frequency is desired.

See Table 8-21 for the trimming effect of ACLKTR[5:0].

NOTE

The first period after enabling the counter by APIFE might be reduced by API start up delay t_{sdel}.

It is possible to generate with the API a waveform at the external pin API_EXTCLK by setting APIFE and enabling the external access with setting APIEA.

8.7 Initialization/Application Information

8.7.1 General Initialization Information

Usually applications run in MCU Normal Mode.

It is recommended to write the CPMUCOP register in any case from the application program initialization routine after reset no matter if the COP is used in the application or not, even if a configuration is loaded via the flash memory after reset. By doing a “controlled” write access in MCU Normal Mode (with the right value for the application) the write once for the COP configuration bits (WCOP,CR[2:0]) takes place which protects these bits from further accidental change. In case of a program sequencing issue (code runaway) the COP configuration can not be accidentally modified anymore.

8.7.2 Application information for COP and API usage

In many applications the COP is used to check that the program is running and sequencing properly. Often the COP is kept running during Stop Mode and periodic wake-up events are needed to service the COP on time and maybe to check the system status.

For such an application it is recommended to use the ACLK as clock source for both COP and API. This guarantees lowest possible IDD current during Stop Mode. Additionally it eases software implementation using the same clock source for both, COP and API.

The Interrupt Service Routine (ISR) of the Autonomous Periodic Interrupt API should contain the write instruction to the CPMUARMCOP register. The value (byte) written is derived from the “main routine” (alternating sequence of $55 and $AA) of the application software.

Using this method, then in the case of a runtime or program sequencing issue the application “main routine” is not executed properly anymore and the alternating values are not provided properly. Hence the COP is written at the correct time (due to independent API interrupt request) but the wrong value is written (alternating sequence of $55 and $AA is no longer maintained) which causes a COP reset.

If the COP is stopped during any Stop Mode it is recommended to service the COP shortly before Stop Mode is entered.

9.5.2.12 ADC Conversion Interrupt Flag Register (ADCCONIF)

After being set any of these bits can be cleared by writing a value of 1’b1. All bits are cleared if bit ADC_EN is clear or via ADC soft-reset (bit ADC_SR set). Writing any flag with value 1’b0 does not clear the flag. Writing any flag with value 1’b1 does not set the flag.

Module Base + 0x000C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CON_IF[15:1]															EOL_IF
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-15. ADC Conversion Interrupt Flag Register (ADCCONIF)

Read: Anytime

Write: Anytime

Table 9-17. ADCCONIF Field Descriptions

Field	Description
15-1 CON_IF[15:1]	**Conversion Interrupt Flags** — These bits could be set by the binary coded interrupt select bits INTFLG_SEL[3:0] when the corresponding conversion command has been processed and related data has been stored to RAM. See also notes below.
0 EOL_IF	**End Of List Interrupt Flag** — This bit is set by the binary coded conversion command type select bits CMD_SEL[1:0] for “end of list” type of commands and after such a command has been processed and the related data has been stored RAM. See also second note below

NOTE

These bits can be used to indicate if a certain packet of conversion results is available. Clearing a flag indicates that conversion results have been retrieved by software and the flag can be used again (see also Section 9.9.6, “RVL swapping in RVL double buffer mode and related registers ADCIMDRI and ADCEOLRI.

NOTE

Overrun situation of a flag CON_IF[15:1] and EOL_IF are indicated by flag CONIF_OIF.

10.3.2.2 BATS Module Status Register (BATSR)

Module Base + 0x0001 Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	BVHC	BVLC
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

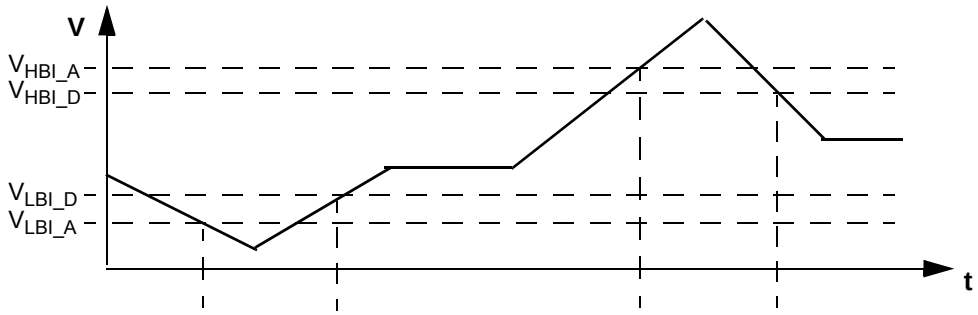
Figure 10-4. BATS Module Status Register (BATSR)

1. Read: Anytime
   Write: Never

Table 10-3. BATSR - Register Field Descriptions

Field	Description
1 BVHC	BATS Voltage Sense High Condition Bit — This status bit indicates that a high voltage at VSUP, depending on selection, is present. 0 $V_{measured} < V_{HBI\_A}$ (rising edge) or $V_{measured} < V_{HBI\_D}$ (falling edge) 1 $V_{measured} \geq V_{HBI\_A}$ (rising edge) or $V_{measured} \geq V_{HBI\_D}$ (falling edge)
0 BVLC	BATS Voltage Sense Low Condition Bit — This status bit indicates that a low voltage at VSUP, depending on selection, is present. 0 $V_{measured} \geq V_{LBI\_A}$ (falling edge) or $V_{measured} \geq V_{LBI\_D}$ (rising edge) 1 $V_{measured} < V_{LBI\_A}$ (falling edge) or $V_{measured} < V_{LBI\_D}$ (rising edge)

Figure 10-5. BATS Voltage Sensing



12.1.3 Block Diagrams

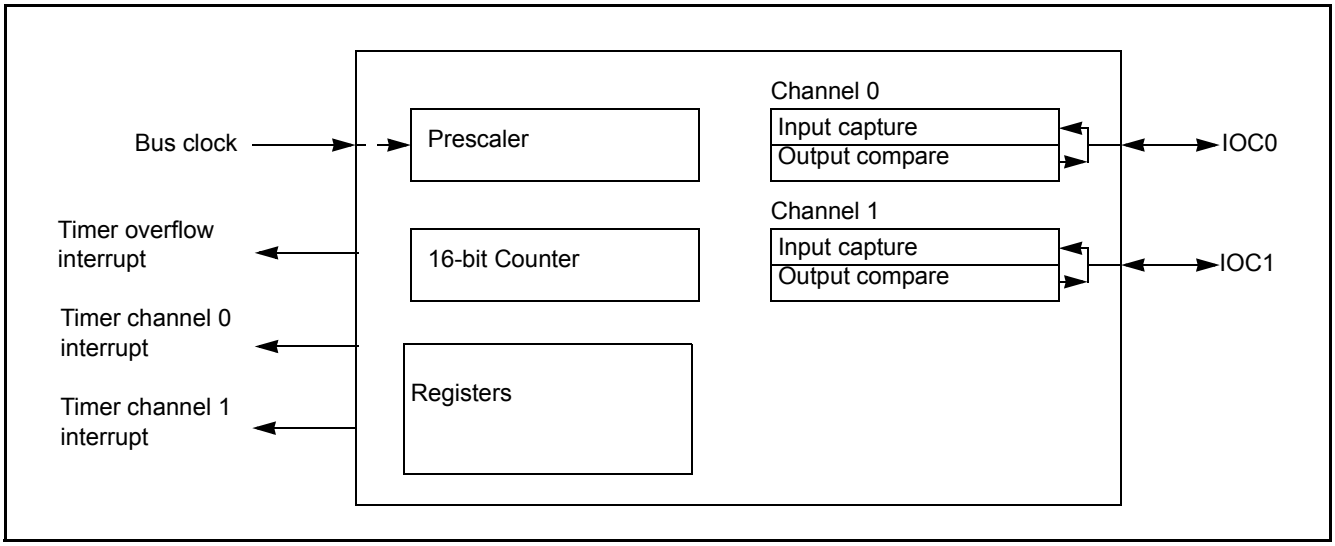


Figure 12-1. TIM16B2CV3 Block Diagram

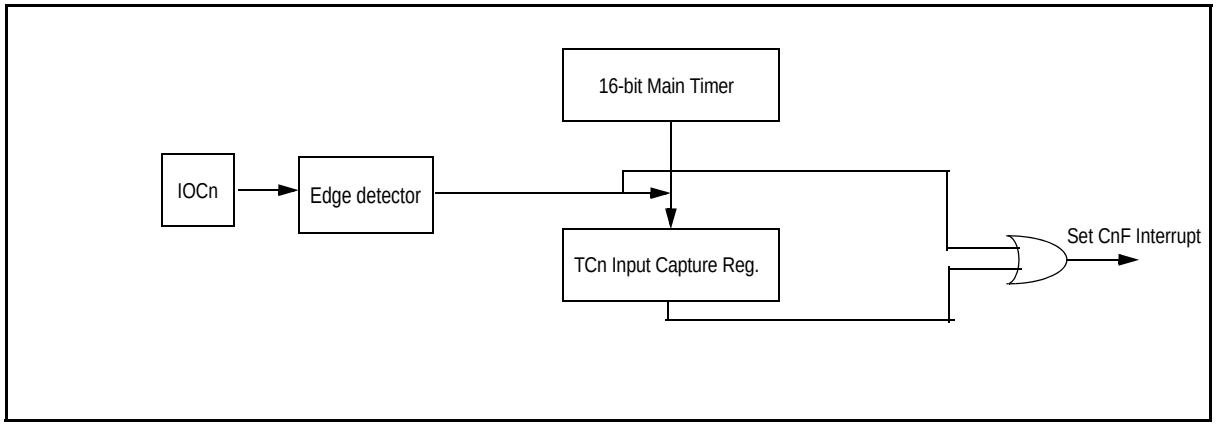


Figure 12-2. Interrupt Flag Setting

12.2 External Signal Description

The TIM16B2CV3 module has a selected number of external pins. Refer to device specification for exact number.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000C TIE	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	RESERVED	PR2	PR1	PR0
	W								
0x000E TFLG1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x001F TCxH–TCxL[1]	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 12-3. TIM16B2CV3 Register Summary (Sheet 2 of 2)

1. The register is available only if corresponding channel exists.

12.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 12-4. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

13.3.2.5 MSCAN Receiver Flag Register (CANRFLG)

A flag can be cleared only by software (writing a 1 to the corresponding bit position) when the condition which caused the setting is no longer valid. Every flag has an associated interrupt enable bit in the CANRIER register.

Module Base + 0x0004 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-8. MSCAN Receiver Flag Register (CANRFLG)

1. Read: Anytime
   Write: Anytime when not in initialization mode, except RSTAT[1:0] and TSTAT[1:0] flags which are read-only; write of 1 clears flag; write of 0 is ignored

NOTE

The CANRFLG register is held in the reset state[1] when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Table 13-10. CANRFLG Register Field Descriptions

Field	Description
7 WUPIF	**Wake-Up Interrupt Flag** — If the MSCAN detects CAN bus activity while in sleep mode (see Section 13.4.5.5, “MSCAN Sleep Mode,”) and WUPE = 1 in CANTCTL0 (see Section 13.3.2.1, “MSCAN Control Register 0 (CANCTL0)”), the module will set WUPIF. If not masked, a wake-up interrupt is pending while this flag is set. 0 No wake-up activity observed while in sleep mode 1 MSCAN detected activity on the CAN bus and requested wake-up
6 CSCIF	**CAN Status Change Interrupt Flag** — This flag is set when the MSCAN changes its current CAN bus status due to the actual value of the transmit error counter (TEC) and the receive error counter (REC). An additional 4-bit (RSTAT[1:0], TSTAT[1:0]) status register, which is split into separate sections for TEC/REC, informs the system on the actual CAN bus status (see Section 13.3.2.6, “MSCAN Receiver Interrupt Enable Register (CANRIER)”). If not masked, an error interrupt is pending while this flag is set. CSCIF provides a blocking interrupt. That guarantees that the receiver/transmitter status bits (RSTAT/TSTAT) are only updated when no CAN status change interrupt is pending. If the TECs/RECs change their current value after the CSCIF is asserted, which would cause an additional state change in the RSTAT/TSTAT bits, these bits keep their status until the current CSCIF interrupt is cleared again. 0 No change in CAN bus status occurred since last interrupt 1 MSCAN changed current CAN bus status

1. The RSTAT[1:0], TSTAT[1:0] bits are not affected by initialization mode.

Table 13-21. CANIDAR0–CANIDAR3 Register Field Descriptions

Field	Description
7-0 AC[7:0]	**Acceptance Code Bits** — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

Module Base + 0x0018 to Module Base + 0x001B — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 13-21. MSCAN Identifier Acceptance Registers (Second Bank) — CANIDAR4–CANIDAR7

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-22. CANIDAR4–CANIDAR7 Register Field Descriptions

Field	Description
7-0 AC[7:0]	**Acceptance Code Bits** — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

13.3.2.18 MSCAN Identifier Mask Registers (CANIDMR0–CANIDMR7)

The identifier mask register specifies which of the corresponding bits in the identifier acceptance register are relevant for acceptance filtering. To receive standard identifiers in 32 bit filter mode, it is required to program the last three bits (AM[2:0]) in the mask registers CANIDMR1 and CANIDMR5 to “don’t care.” To receive standard identifiers in 16 bit filter mode, it is required to program the last three bits (AM[2:0]) in the mask registers CANIDMR1, CANIDMR3, CANIDMR5, and CANIDMR7 to “don’t care.”

Module Base + 0x0014 to Module Base + 0x0017 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 13-22. MSCAN Identifier Mask Registers (First Bank) — CANIDMR0–CANIDMR3

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Module Base + 0x00X2

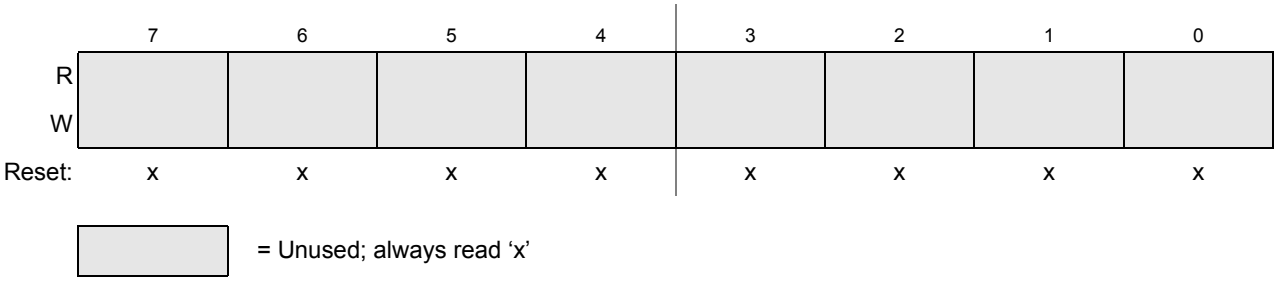


Figure 13-32. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

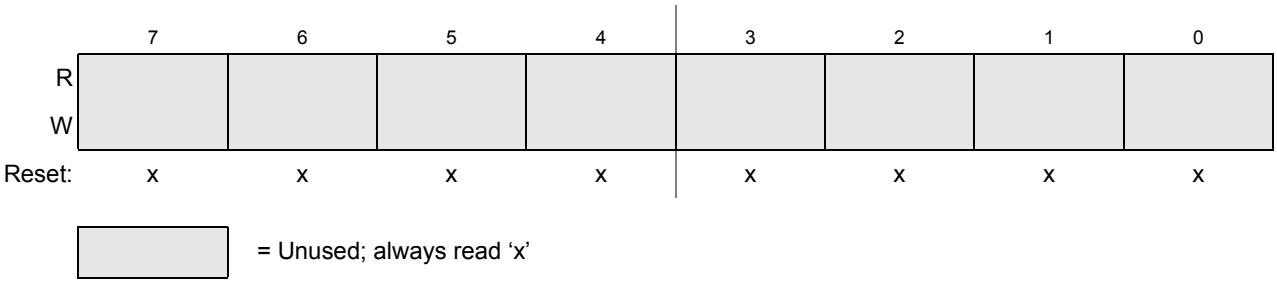


Figure 13-33. Identifier Register 3 — Standard Mapping

13.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

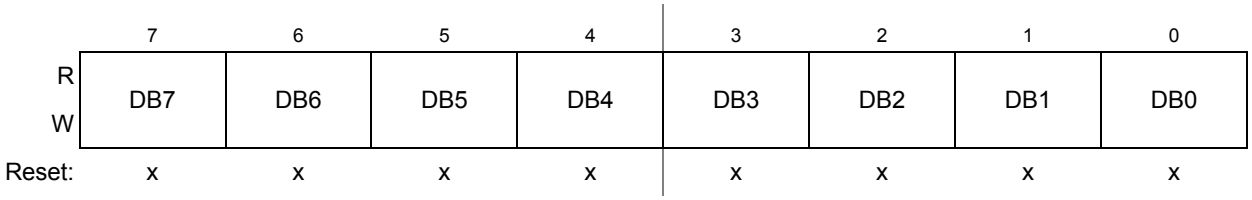


Figure 13-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 13-32. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	**Data bits 7-0**

Table 14-6. PTUIEL Register Field Descriptions

Field	Description
5 TG1TEIE	Trigger Generator 1 Timing Error Interrupt Enable — Enables trigger generator timing error interrupt. 0 No interrupt will be requested whenever TG1TEIF is set 1 Interrupt will be requested whenever TG1TEIF is set
4 TG1DIE	Trigger Generator 1 Done Interrupt Enable — Enables trigger generator done interrupt. 0 No interrupt will be requested whenever TG1DIF is set 1 Interrupt will be requested whenever TG1DIF is set
3 TG0AEIE	Trigger Generator 0 Memory Access Error Interrupt Enable — Enables trigger generator memory access error interrupt. 0 No interrupt will be requested whenever TG0AEIF is set 1 Interrupt will be requested whenever TG0AEIF is set
2 TG0REIE	Trigger Generator 0 Reload Error Interrupt Enable — Enables trigger generator reload error interrupt. 0 No interrupt will be requested whenever TG0REIF is set 1 Interrupt will be requested whenever TG0REIF is set
1 TG0TEIE	Trigger Generator 0 Timing Error Interrupt Enable — Enables trigger generator timing error interrupt. 0 No interrupt will be requested whenever TG0TEIF is set 1 Interrupt will be requested whenever TG0TEIF is set
0 TG0DIE	Trigger Generator 0 Done Interrupt Enable — Enables trigger generator done interrupt. 0 No interrupt will be requested whenever TG0DIF is set 1 Interrupt will be requested whenever TG0DIF is set

14.3.2.7 Trigger Generator 0 List Register (TG0LIST)

Module Base + 0x0006 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	TG0LIST
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-9. Trigger Generator 0 List Register (TG0LIST)

1. Read: Anytime
   Write: Anytime, if TG0EN bit is cleared

Table 14-9. TG0LIST Register Field Descriptions

Field	Description
0 TG0LIST	Trigger Generator 0 List — This bit shows the number of the current used list. 0 Trigger generator 0 is using list 0 1 Trigger generator 0 is using list 1

14.3.2.8 Trigger Generator 0 Trigger Number Register (TG0TNUM)

Module Base + 0x0007 Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	TG0TNUM[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-10. Trigger Generator 0 Trigger Number Register (TG0TNUM)

1. Read: Anytime
   Write: Never

Table 14-10. TG0TNUM Register Field Descriptions

Field	Description
4:0 TG0TNUM[4:0]	Trigger Generator 0 Trigger Number — This register shows the number of generated triggers since the last reload event. After the generation of 32 triggers this register shows zero. The next reload event clears this register. See also Figure 14-22.

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

16.4.6.3 Data Sampling

The RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 16-21) is re-synchronized immediatelly at bus clock edge:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s.When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

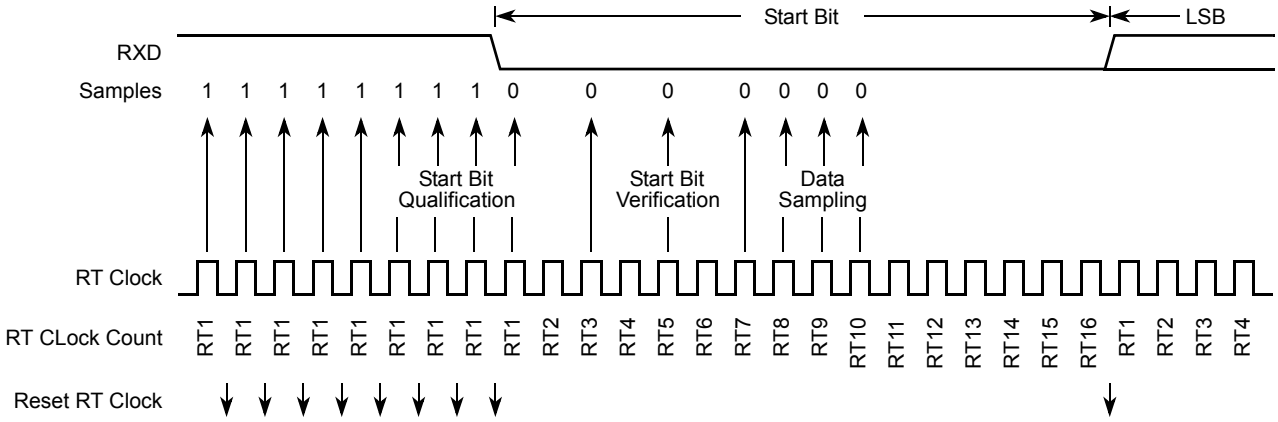


Figure 16-21. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Figure 16-17 summarizes the results of the start bit verification samples.

Table 16-17. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

Table 19-5. LPSLRM Field Description

Field	Description
7 LPDTDIS	TxD-dominant timeout disable Bit — This bit disables the TxD-dominant timeout feature. Disabling this feature is only recommended for using the LIN Physical Layer for other applications than LIN protocol. It is only writable in shutdown mode (LPE=0). 0 TxD-dominant timeout feature is enabled. 1 TxD-dominant timeout feature is disabled.
1-0 LPSLR[1:0]	Slew-Rate Bits — Please see section 19.4.2 for details on how the slew rate control works. These bits are only writable in shutdown mode (LPE=0). 00 Normal Slew Rate (optimized for 20 kbit/s). 01 Slow Slew Rate (optimized for 10.4 kbit/s). 10 Fast Mode Slew Rate (up to 250 kbit/s). This mode is not compliant with the LIN Protocol (LIN electrical characteristics like duty cycles, reference levels, etc. are not fulfilled). It is only meant to be used for fast data transmission. Please refer to section 19.4.2.2 for more details on fast mode.Please note that an external pullup resistor stronger than 1 kΩ might be necessary for the range 100 kbit/s to 250 kbit/s. 11 Reserved .

19.3.2.5 Reserved Register

Module Base + Address 0x0004 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

= Unimplemented

Figure 19-7. Reserved Register

1. Read: Anytime

   Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the module's functionality.

Table 19-6. Reserved Register Field Description

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.

If LPWUE is not set, no wake up feature is available and the standby mode has the same electrical properties as the shutdown mode. This allows a low-power consumption of the device in stop mode if the wake-up feature is not needed.

If LPWUE is set, the receiver is able to pass wake-up events to the SCI (Serial Communication Interface). If the LIN/HV Physical Layer receives a dominant level longer than t_{WUFR} followed by a rising edge, it sends a pulse to the SCI which can generate a wake-up interrupt.

Once the device exits stop mode, the LIN/HV Physical Layer returns to normal or receive only mode depending on the status of the RXONLY bit.

NOTE

Since the wake-up interrupt is requested by the SCI, the wake-up feature is not available if LPRxD is not connected to the SCI..

The internal pullup resistor is selectable only if LPWUE = 1 (wake-up enabled). If LPWUE = 0, the internal pullup resistor is not selectable and remains at 330 kΩ regardless of the state of the LPPUE bit.

If LPWUE = 1, selecting the 330 kΩ pullup resistor (LPPUE = 0) reduces the current consumption in standby mode.

NOTE

The use of the LIN wake-up feature in combination with other non-LIN device wake-up features (like a periodic time interrupt) must be handled with care.

If the device leaves stop mode while the LIN bus is dominant, the LIN/HV Physical Layer returns to normal or receive only mode and the LPRxD signal is re-routed to the RxD pin of the SCI and triggers the edge detection interrupt (if the interrupt's priority of the hardware that awakes the MCU is less than the priority of the SCI interrupt, then the SCI interrupt will execute first). It is up to the software to decide what to do in this case because the LIN/HV Physical Layer may not determine whether it was a valid wake-up pulse.

Table 20-16. FERCNFG Field Descriptions

Field	Description
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 20.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 20.3.2.8)

20.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0(1)	01

= Unimplemented or Reserved

Figure 20-11. Flash Status Register (FSTAT)

1. Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 20.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

Table 20-17. FSTAT Field Descriptions

Field	Description
7 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that a Flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress 1 Flash command has completed
5 ACCERR	**Flash Access Error Flag** — The ACCERR bit indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 20.4.5.2) or issuing an illegal Flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR. 0 No access error detected 1 Access error detected
4 FPVIOL	**Flash Protection Violation Flag** —The FPVIOL bit indicates an attempt was made to program or erase an address in a protected area of P-Flash or EEPROM memory during a command write sequence. The FPVIOL bit is cleared by writing a 1 to FPVIOL. Writing a 0 to the FPVIOL bit has no effect on FPVIOL. While FPVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected 1 Protection violation detected
3 MGBUSY	**Memory Controller Busy Flag** — The MGBUSY flag reflects the active state of the Memory Controller. 0 Memory Controller is idle 1 Memory Controller is busy executing a Flash command (CCIF = 0)

Chapter 21
CAN Physical Layer (S12CANPHYV3)

Table 21-1. Revision History Table

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.00	05 Nov 2012		• Added CPTXD-dominant timeout feature
V03.00	15 Apr 2013		• Made transmit driver (CANH & CANL) independent of CPCHVL condition • Changed CPCLVL condition to disable CANL only • Added mode to cover separation of CANH and CANL drivers • Added configurable wake-up filter

NOTE

The information given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed and are subject to change without notice.

21.1 Introduction

The CAN Physical Layer provides a physical layer for high speed CAN area network communication in automotive applications. It serves as an integrated interface to the CAN bus lines for the internally connected MSCAN controller through the pins CANH, CANL and SPLIT.

The CAN Physical Layer is designed to meet the CAN Physical Layer ISO 11898-2 and ISO 11898-5 standards.

21.1.1 Features

The CAN Physical Layer module includes these distinctive features:

- High speed CAN interface for baud rates of up to 1 Mbit/s
- ISO 11898-2 and ISO 11898-5 compliant for 12 V battery systems
- SPLIT pin driver for bus recessive level stabilization
- Low power mode with remote CAN wake-up handled by MSCAN module
- Configurable wake-up pulse filtering
- Over-current shutdown for CANH and CANL
- Voltage monitoring on CANH and CANL
- CPTXD-dominant timeout feature monitoring the CPTXD signal
- Fulfills the OEM “Hardware Requirements for (LIN,) CAN (and FlexRay) Interfaces in Automotive Applications” v1.3

Table C-3. ADC Conversion Performance 5 V range (Junction Temperature From –40°C To +150°C)

Supply voltage 4.5 V < V_{DDA} < 5.5 V, 4.5V < V_{REF} < 5.5 V. (V_{REF}= V_{RH} - V_{RL}). f_{ADCCLK} = 8.0 MHz
The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
1		Resolution (V_{REF} = 5.12V)	12-Bit	LSB	—	1.25	—	mV
2		Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3		Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4		Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5		Resolution (V_{REF} = 5.12V)	10-Bit	LSB	—	5	—	mV
6		Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7		Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8		Absolute Error	10-Bit	AE	-3	±2	3	counts
9		Resolution (V_{REF} = 5.12V)	8-Bit	LSB	—	20	—	mV
10		Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11		Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12		Absolute Error	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.
2. These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table C-4. ADC Conversion Performance 5 V range (Junction Temperature From 150°C To +175°C)

Supply voltage 4.5 V < V_{DDA} < 5.5 V, 4.5V < V_{REF} < 5.5 V. (V_{REF}= V_{RH} - V_{RL}). f_{ADCCLK} = 8.0 MHz
The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
1		Resolution (V_{REF} = 5.12V)	12-Bit	LSB	—	1.25	—	mV
2		Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3		Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4		Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5		Resolution (V_{REF} = 5.12V)	10-Bit	LSB	—	5	—	mV
6		Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7		Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8		Absolute Error	10-Bit	AE	-3	±2	3	counts
9		Resolution (V_{REF} = 5.12V)	8-Bit	LSB	—	20	—	mV
10		Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11		Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12		Absolute Error	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2. These values include the quantization error which is inherently 1/2 count for any A/D converter.

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0518	PMFVAL4	R	PMFVAL4							
		W								
0x0519	PMFVAL4	R	PMFVAL4							
		W								
0x051A	PMFVAL5	R	PMFVAL5							
		W								
0x051B	PMFVAL5	R	PMFVAL5							
		W								
0x051C	PMFROIE	R	0	0	0	0	0	PMFROIEC	PMFROIEB	PMFROIEA
		W								
0x051D	PMFROIF	R	0	0	0	0	0	PMFROIFC	PMFROIFB	PMFROIFA
		W								
0x051E	PMFICCTL	R	0	0	PECC	PECB	PECA	ICCC	ICCB	ICCA
		W								
0x051F	PMFCINV	R	0	0	CINV5	CINV4	CINV3	CINV2	CINV1	CINV0
		W								
0x0520	PMFENCA	R	PWMENA	GLDOKA	0	0	0	RSTRTA	LDOKA	PWMRIEA
		W								
0x0521	PMFFQCA	R	LDFQA				HALFA	PRSCA		PWMRFA
		W								
0x0522	PMFCNTA	R	0	PMFCNTA						
		W								
0x0523	PMFCNTA	R	PMFCNTA							
		W								
0x0524	PMFMODA	R	0	PMFMODA						
		W								
0x0525	PMFMODA	R	PMFMODA							
		W								
0x0526	PMFDTMA	R	0	0	0	0	PMFDTMA			
		W								
0x0527	PMFDTMA	R	PMFDTMA							
		W								
0x0528	PMFENCB	R	PWMENB	GLDOKB	0	0	0	RSTRTB	LDOKB	PWMRIEB
		W								

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0529	PMFFQCB	R	LDFQB				HALFB	PRSCB		PWMRFB
		W								
0x052A	PMFCNTB	R	0	PMFCNTB						
		W								
0x052B	PMFCNTB	R	PMFCNTB							
		W								
0x052C	PMFMODB	R	0	PMFMODB						
		W								
0x052D	PMFMODB	R	PMFMODB							
		W								
0x052E	PMFDTMB	R	0	0	0	0	PMFDTMB			
		W								
0x052F	PMFDTMB	R	PMFDTMB							
		W								
0x0530	PMFENCC	R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
		W								
0x0531	PMFFQCC	R	LDFQC				HALFC	PRSCC		PWMRFC
		W								
0x0532	PMFCNTC	R	0	PMFCNTC						
		W								
0x0533	PMFCNTC	R	PMFCNTC							
		W								
0x0534	PMFMODC	R	0	PMFMODC						
		W								
0x0535	PMFMODC	R	PMFMODC							
		W								
0x0536	PMFDTMC	R	0	0	0	0	PMFDTMC			
		W								
0x0537	PMFDTMC	R	PMFDTMC							
		W								
0x0538	PMFDMP0	R	DMP05		DMP04		DMP03	DMP02	DMP01	DMP00
		W								
0x0539	PMFDMP1	R	DMP15		DMP14		DMP13	DMP12	DMP11	DMP10
		W								