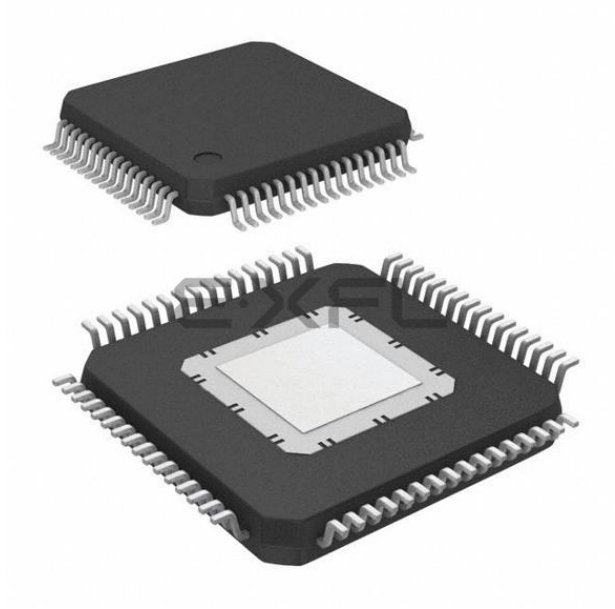

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f2vkh

Table 1-5. Module Register Address Ranges

Address	Module	Size (Bytes)
0x06E0–0x06EF	Reserved	16
0x06F0–0x06F7	BATS	8
0x06F8–0x06FF	Reserved	8
0x0700–0x0707	SCI0	8
0x0708–0x070F	Reserved	8
0x0710–0x0717	SCI1	8
0x0718–0x077F	Reserved	104
0x0780–0x0787	SPI0	8
0x0788–0x07FF	Reserved	120
0x0800–0x083F	CAN0	64
0x0840–0x097F	Reserved	320
0x0980–0x0987	LINPHY (S12ZVML derivatives)	8
0x0980–0x0987	HV Physical Interface (S12ZVM32, S12ZVM16 derivatives)	8
0x0988–0x098F	Reserved	8
0x0990–0x0997	CANPHY (ZVMC256 only)	8
0x0998–0x0FFF	Reserved	1640

1. Reading from the first 16 locations in this reserved range returns undefined data

2. Address range = 0x0690-0x069F on Maskset N06E

NOTE

Reserved register space shown above is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns zero.

1.6.1 Flash Module

This device family instantiates different flash modules, depending on derivative. The flash documentation for the all devices is featured in the FTMRZ section.

1.7.2.26.8 VDDC (Only Available On S12ZVMC Versions)

VDDC is the CANPHY supply. This is the output voltage of the external bipolar, whose base current is supplied by BCTLC. It is fed back to the MCU for regulation. On the ZVMC128 a diode is recommended between VDDA and VDDC, whereby the anode is connected to VDDC.

1.7.2.26.9 VSSC (Only Available On ZVMC256)

VSSC is the CANPHY ground.

1.7.2.27 Gate Drive Unit (GDU) Signals

These are associated with driving the external FETs.

1.7.2.27.1 HD — FET Predriver High side Drain Input

This is the drain connection of the external high-side FETs. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC via an analog multiplexer.

1.7.2.27.2 VBS[2:0] - Bootstrap Capacitor Connections

These signals are the bootstrap capacitor connections for phases HS[2:0]. The capacitor connected between HS[2:0] and these signals provides the gate voltage and current to drive the external FET.

1.7.2.27.3 HG[2:0] - High-Side Gate signals

The pins are the gate drives for the three high-side power FETs. The drivers provide a high current with low impedance to turn on and off the high-side power FETs.

1.7.2.27.4 HS[2:0] - High-Side Source signals

The pins are the source connection for the high-side power FETs and the drain connection for the low-side power FETs. The low voltage end of the bootstrap capacitor is also connected to this pin.

1.7.2.27.5 VLS[2:0] - Voltage Supply for Low -Side Drivers

The pins are the voltage supply pins for the three low-side FET pre-drivers. These pins should be connected to the voltage regulator output pin VLS_OUT.

1.7.2.27.6 LG[2:0] - Low-Side Gate signals

The pins are the gate drives for the low-side power FETs. The drivers provide a high current with low impedance to turn on and off the low-side power FETs.

1.7.2.27.7 LS[2:0] - Low-Side Source Signals

The pins are the low-side source connections for the low-side power FETs. The pins are the power ground pins used to return the gate currents from the low-side power FETs.

This byte can be erased and programmed like any other Flash location. Two bits of this byte are used for security (SEC[1:0]). The contents of this byte are copied into the Flash security register (FSEC) during a reset sequence.

The meaning of the security bits SEC[1:0] is shown in Table 1-14. For security reasons, the state of device security is controlled by two bits. To put the device in unsecured mode, these bits must be programmed to SEC[1:0] = ‘10’. All other combinations put the device in a secured mode. The recommended value to put the device in secured state is the inverse of the unsecured state, i.e. SEC[1:0] = ‘01’.

Table 1-14. Security Bits

SEC[1:0]	Security State
00	1 (secured)
01	1 (secured)
10	0 (unsecured)
11	1 (secured)

NOTE

Please refer to the Flash block description for more security byte details.

1.10.3 Operation of the Secured Microcontroller

By securing the device, unauthorized access to the EEPROM and Flash memory contents is prevented. Secured operation has the following effects on the microcontroller:

1.10.3.1 Normal Single Chip Mode (NS)

- Background debug controller (BDC) operation is completely disabled.
- Execution of Flash and EEPROM commands is restricted (described in flash block description).

1.10.3.2 Special Single Chip Mode (SS)

- Background debug controller (BDC) commands are restricted
- Execution of Flash and EEPROM commands is restricted (described in flash block description).

In special single chip mode the device is in active BDM after reset. In special single chip mode on a secure device, only the BDC mass erase and BDC control and status register commands are possible. BDC access to memory mapped resources is disabled. The BDC can only be used to erase the EEPROM and Flash memory without giving access to their contents.

1.10.4 Unsecuring the Microcontroller

Unsecuring the microcontroller can be done using three different methods:

1. Backdoor key access
2. Reprogramming the security bits
3. Complete memory erase

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0338–0x0339	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x033A	PTABYPL[2]	R	0	0	0	0	0	0	0	PTABYPL0
		W								
0x033B	PTADIRL[2]	R	0	0	0	0	0	0	0	PTADIRL0
		W								
0x033C	DIENL[2]	R	0	0	0	0	0	0	0	DIENL0
		W								
0x033D	PTAENL[2]	R	0	0	0	0	0	0	0	PTAENL0
		W								
0x033E	PIRL[2]	R	0	0	0	0	0	0	0	PIRL0
		W								
0x033F	PTTEL[2]	R	0	0	0	0	0	0	0	PTTEL0
		W								

1. Only available for ZVML128, ZVML64, ZVML32, and ZVML31
2. Only available for ZVMC256
3. PWMPRR[1] only writable for ZVMC256
4. Only available for ZVMC256, ZVML31, ZVM32, ZVM16
5. Not available for ZVMC256

2.3.2 PIM Registers 0x0200-0x020F

This section details the specific purposes of register implemented in address range 0x0200-0x020F. These registers serve for specific PIM related functions not part of the generic port registers.

- If not stated differently, writing to reserved bits has no effect and read returns zero.
- All register read accesses are synchronous to internal clocks.
- Register bits can be written at any time if not stated differently.

6.4.5 Trace Buffer Operation

The trace buffer is a 64 lines deep by 64-bits wide RAM array. If the TSOURCE bit is set the DBG module can store trace information in the RAM array in a circular buffer format. Data is stored in mode dependent formats, as described in the following sections. After each trace buffer entry, the counter register DBGCNT is incremented. Trace buffer rollover is possible when configured for End- or Mid-Aligned tracing, such that older entries are replaced by newer entries. Tracing of CPU activity is disabled when the BDC is active.

The RAM array can be accessed through the register DBGTB using 16-bit wide word accesses. After each read, the internal RAM pointer is incremented so that the next read will receive fresh information. Reading the trace buffer whilst the DBG is armed returns invalid data and the trace buffer pointer is not incremented.

In Detail mode the address range for CPU access tracing can be limited to a range specified by the TRANGE bits in DBGTCRH. This function uses comparators C and D to define an address range inside which accesses should be traced. Thus traced accesses can be restricted, for example, to particular register or RAM range accesses.

The external event pin can be configured to force trace buffer entries in Normal or Loop1 trace modes. All tracing modes support trace buffer gating. In Pure PC and Detail modes external events do not force trace buffer entries.

If the external event pin is configured to gate trace buffer entries then any trace mode is valid.

6.4.5.1 Trace Trigger Alignment

Using the TALIGN bits (see Section 6.3.2.3”) it is possible to align the trigger with the end, the middle, or the beginning of a tracing session.

If End or Mid-Alignment is selected, tracing begins when the ARM bit in DBGC1 is set and State1 is entered. The transition to Final State if End-Alignment is selected, ends the tracing session. The transition to Final State if Mid-Alignment is selected signals that another 32 lines are traced before ending the tracing session. Tracing with Begin-Alignment starts at the trigger and ends when the trace buffer is full.

Table 6-47. Tracing Alignment

TALIGN	Tracing Begin	Tracing End
00	On arming	At trigger
01	At trigger	When trace buffer is full
10	On arming	When 32 trace buffer lines have been filled after trigger
11	Reserved	

6.4.5.1.1 Storing with Begin-Alignment

Storing with Begin-Alignment, data is not stored in the trace buffer until the Final State is entered. Once the trigger condition is met the DBG module remains armed until 64 lines are stored in the trace buffer.

8.3.2.12 S12CPMU_UHV_V10_V6 COP Control Register (CPMUCOP)

This register controls the COP (Computer Operating Properly) watchdog.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit (see also Table 8-8).
In Stop Mode with PSTP=1 (Pseudo Stop Mode), COPOSCSEL0=1 and COPOSCEL1=0 and PCE=1 the COP continues to run, else the COP counter halts in Stop Mode with COPOSCSEL1 =0.
In Full Stop Mode and Pseudo Stop Mode with COPOSCSEL1=1 the COP continues to run.

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W			WRTMASK					
Reset	F	0	0	0	0	F	F	F

After de-assert of System Reset the values are automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 8-17. S12CPMU_UHV_V10_V6 COP Control Register (CPMUCOP)

Read: Anytime

Write:

1. RSBCK: Anytime in Special Mode; write to “1” but not to “0” in Normal Mode
2. WCOP, CR2, CR1, CR0:
   - — Anytime in Special Mode, when WRTMASK is 0, otherwise it has no effect
   - — Write once in Normal Mode, when WRTMASK is 0, otherwise it has no effect.
     - – Writing CR[2:0] to “000” has no effect, but counts for the “write once” condition.
     - – Writing WCOP to “0” has no effect, but counts for the “write once” condition.

When a non-zero value is loaded from Flash to CR[2:0] the COP time-out period is started.

A change of the COPOSCSEL0 or COPOSCSEL1 bit (writing a different value) or loosing UPOSC status while COPOSCSEL1 is clear and COPOSCSEL0 is set, re-starts the COP time-out period.

In Normal Mode the COP time-out period is restarted if either of these conditions is true:

1. Writing a non-zero value to CR[2:0] (anytime in special mode, once in normal mode) with WRTMASK = 0.
2. Writing WCOP bit (anytime in Special Mode, once in Normal Mode) with WRTMASK = 0.
3. Changing RSBCK bit from “0” to “1”.

In Special Mode, any write access to CPMUCOP register restarts the COP time-out period.

Table 8-14. CPMUCOP Field Descriptions

Field	Description
7 WCOP	**Window COP Mode Bit** — When set, a write to the CPMUARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period generates a COP reset. As long as all writes occur during this window, $55 can be written as often as desired. Once $AA is written after the $55, the time-out logic restarts and the user must wait until the next window before writing to CPMUARMCOP. Table 8-15 shows the duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation
6 RSBCK	COP and RTI Stop in Active BDM Mode Bit 0 Allows the COP and RTI to keep running in Active BDM mode. 1 Stops the COP and RTI counters whenever the part is in Active BDM mode.
5 WRTMASK	**Write Mask for WCOP and CR[2:0] Bit** — This write-only bit serves as a mask for the WCOP and CR[2:0] bits while writing the CPMUCOP register. It is intended for BDM writing the RSBCK without changing the content of WCOP and CR[2:0]. 0 Write of WCOP and CR[2:0] has an effect with this write of CPMUCOP 1 Write of WCOP and CR[2:0] has no effect with this write of CPMUCOP. (Does not count for “write once”.)
2–0 CR[2:0]	**COP Watchdog Timer Rate Select** — These bits select the COP time-out rate (see Table 8-15 and Table 8-16). Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a System Reset. This can be avoided by periodically (before time-out) initializing the COP counter via the CPMUARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest time-out period (2^{24} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in Special Mode

Table 8-15. COP Watchdog Rates if COPOSCSEL1=0. (default out of reset)

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is either IRCCLK or OSCCLK depending on the COPOSCSEL0 bit)
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

9.9.10 Fully Timing Controlled Conversion

As described previously, in “Trigger Mode” a Restart Event automatically causes a trigger. To have full and precise timing control of the beginning of any conversion/sequence the “Restart Mode” is available. In “Restart Mode” a Restart Event does not cause a Trigger automatically; instead, the Trigger must be issued separately and with correct timing, which means the Trigger is not allowed before the Restart Event (conversion command loading) is finished (bit RSTA=1’b0 again). The time required from Trigger until sampling phase starts is given (refer to Section 9.5.2.6, “ADC Conversion Flow Control Register (ADCFLWCTL), Timing considerations) and hence timing is fully controllable by the application. Additionally, if a Trigger occurs before a Restart Event is finished, this causes the TRIG_EIF flag being set. This allows detection of false flow control sequences.

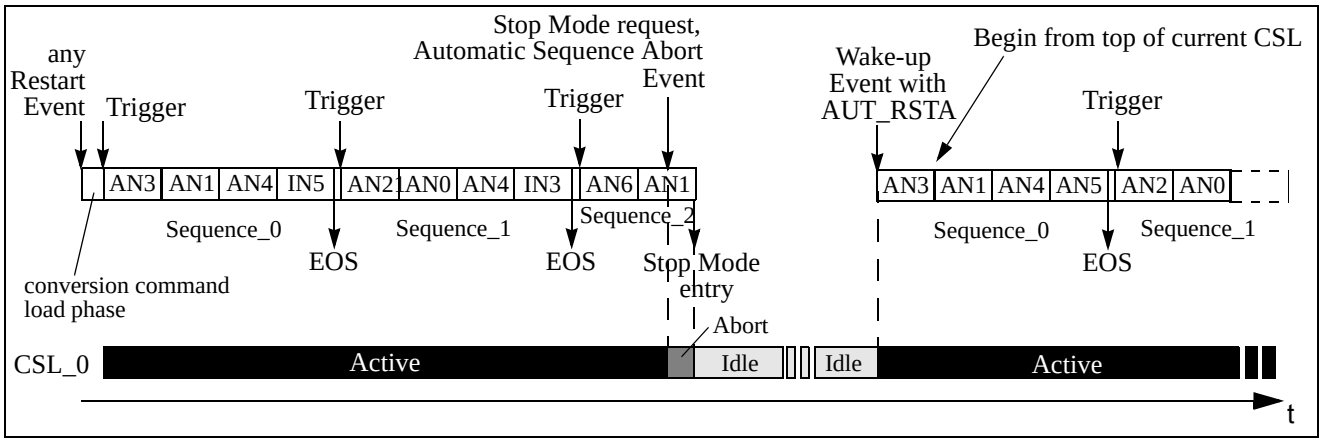


Figure 9-44. Conversion Flow Control Diagram — Fully Timing Controlled Conversion (with Stop Mode)

Unlike the Stop Mode entry shown in Figure 9-43 and Figure 9-44 it is recommended to issue the Stop Mode at sequence boundaries (when ADC is idle and no conversion/conversion sequence is ongoing).

Any of the Conversion flow control application use cases described above (Continuous, Triggered, or Fully Timing Controlled Conversion) can be used with CSL single buffer mode or with CSL double buffer mode. If using CSL double buffer mode, CSL swapping is performed by issuing a Restart Event with bit LDOK set.

14.1.3 Block Diagram

Figure 14-1 shows a block diagram of the PTU module.

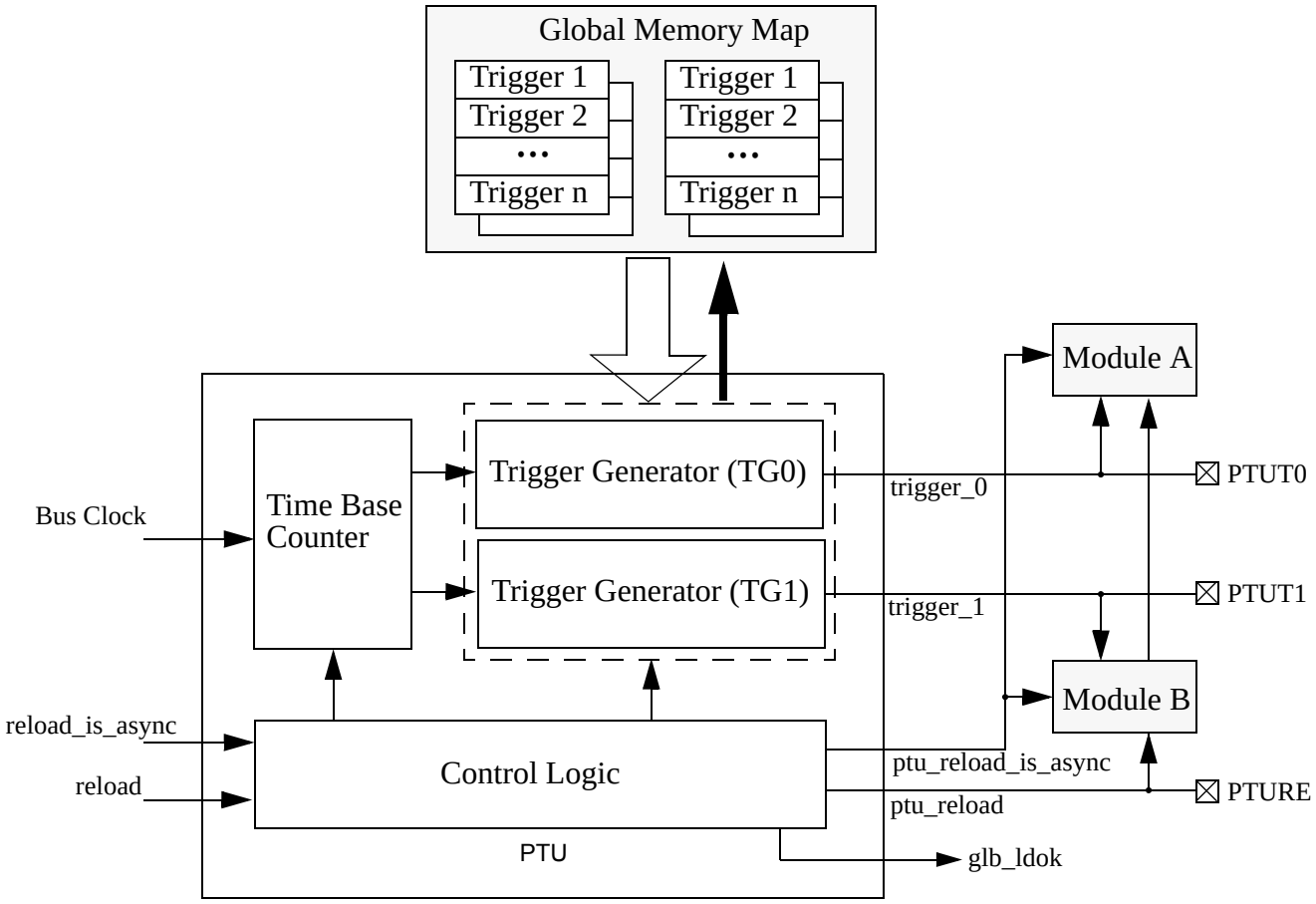


Figure 14-1. PTU Block Diagram

14.2 External Signal Description

This section lists the name and description of all external ports.

14.2.1 PTUT0 — PTU Trigger 0

If enabled (PTUT0PE is set) this pin shows the internal trigger_0 event.

14.2.2 PTUT1 — PTU Trigger 1

If enabled (PTUT1PE is set) this pin shows the internal trigger_1 event.

15.3.2 Register Descriptions

15.3.2.1 PMF Configure 0 Register (PMFCFG0)

Address: Module Base + 0x0000 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
Reset	0	0	0	0	0	0	0	0

Figure 15-3. PMF Configure 0 Register (PMFCFG0)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

Table 15-6. PMFCFG0 Field Descriptions

Field	Description
7 WP	**Write Protect**— This bit enables write protection to be used for all write-protectable registers. While clear, WP allows write-protected registers to be written. When set, WP prevents any further writes to write-protected registers. Once set, WP can be cleared only by reset. 0 Write-protectable registers may be written 1 Write-protectable registers are write-protected
6 MTG	**Multiple Timebase Generators** — This bit determines the number of timebase counters used. This bit cannot be modified after the WP bit is set. If MTG is set, PWM generators B and C and registers 0x0028 – 0x0037 are availabled.The three generators have their own variable frequencies and are not synchronized. If MTG is cleared, PMF registers from 0x0028 – 0x0037 can not be written and read zeroes, and bits EDGEC and EDGEB are ignored. Pair A, Pair B, and Pair C PWMs are synchronized to PWM generator A and use registers from 0x0020 – 0x0027. 0 Single timebase generator 1 Multiple timebase generators
5 EDGEC	**Edge-Aligned or Center-Aligned PWM for Pair C —** This bit determines whether PWM4 and PWM5 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are center-aligned PWMs 1 PWM4 and PWM5 are edge-aligned PWMs
4 EDGEB	**Edge-Aligned or Center-Aligned PWM for Pair B —** This bit determines whether PWM2 and PWM3 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are center-aligned PWMs 1 PWM2 and PWM3 are edge-aligned PWMs
3 EDGEA	**Edge-Aligned or Center-Aligned PWM for Pair A—** This bit determines whether PWM0 and PWM1 channels will use edge-aligned or center-aligned waveforms. It determines waveforms for Pair B and Pair C if the MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM0 and PWM1 are center-aligned PWMs 1 PWM0 and PWM1 are edge-aligned PWMs
2 INDEPC	**Independent or Complementary Operation for Pair C**— This bit determines if the PWM channels 4 and 5 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are complementary PWM pair 1 PWM4 and PWM5 are independent PWMs

Table 15-16. PMFOUTC Field Descriptions

Field	Description
5–0 OUTCTL[5:0]	**OUTCTL*n* Bits** — These bits enable software control of their corresponding PWM output. When OUTCTL*n* is set, the OUT*n* bit takes over the directly controls the level of the PWM*n* output. **Note:** OUTCTL*n* is buffered if ENCE is set. If ENCE is set, then the value written does not take effect until the next commutation cycle begins. Reading OUTCTLn returns the value in the buffer and not necessarily the value the output control is currently using.If ENCE is not set, then the OUTn bits take immediately effect when OUTCTLn bit is set. If the OUTCTLn bit is cleared then the OUTn control is disabled at the next PMF cycle start. When operating the PWM in complementary mode, these bits must be switched in pairs for proper operation. That is OUTCTL0 and OUTCTL1 must have the same value; OUTCTL2 and OUTCTL3 must have the same value; and OUTCTL4 and OUTCTL5 must have the same value. Otherwise see the behavior described on chapter Section 15.8.2, “BLDC 6-Step Commutation”. 0 Software control disabled 1 Software control enabled *n* is 0, 1, 2, 3, 4 and 5.

15.3.2.11 PMF Output Control Bit Register (PMFOUTB)

Address: Module Base + 0x000D — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-14. PMF Output Control Bit Register (PMFOUTB)

1. Read: Anytime
   Write: Anytime

Table 15-17. PMFOUTB Field Descriptions

Field	Description
5–0 OUT[5:0]	**OUT*n* Bits** — If the corresponding OUTCTL*n* bit is set, these bits control the PWM outputs, illustrated in Table 15-18. If the related OUTCTLn=1 a read returns the register contents OUTn else the current PWM output states are returned(1) On module version V3 the read returns always the register value. **Note:** OUT*n* is buffered if ENCE is set. The value written does not take effect until the next commutation cycle begins. Reading OUT*n* (with OUTCTL*n*=1) returns the value in the buffer and not necessarily the value the output control is currently using. *n* is 0. 1. 2. 3. 4 and 5.

1. only valid for module version V4

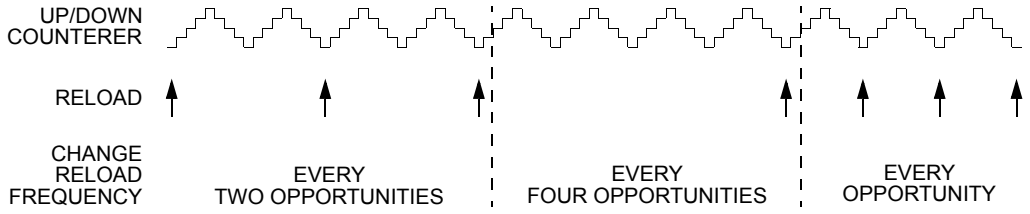


Figure 15-73. Full Cycle Reload Frequency Change

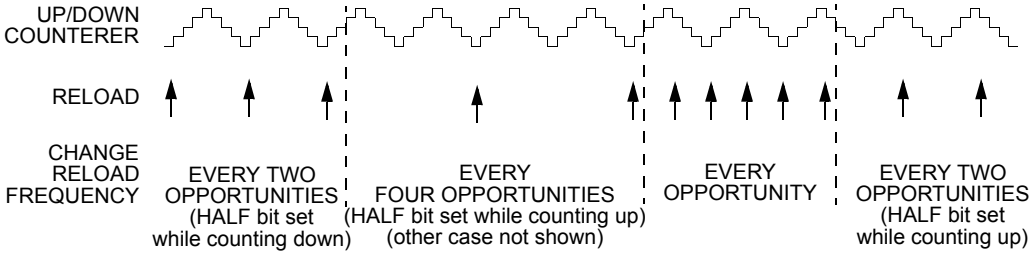


Figure 15-74. Half Cycle Reload Frequency Change

15.4.12.4 Reload Flag

The PWMRF reload flag is set at every reload opportunity, regardless of whether an actual reload occurs (as determined by the related LDOK bit or global load OK). If the PWM reload interrupt enable bit PWMRIE is set, the PWMRF flag generates CPU interrupt requests allowing software to calculate new PWM parameters in real time. When PWMRIE is not set, reloads still occur at the selected reload rate without generating CPU interrupt requests.

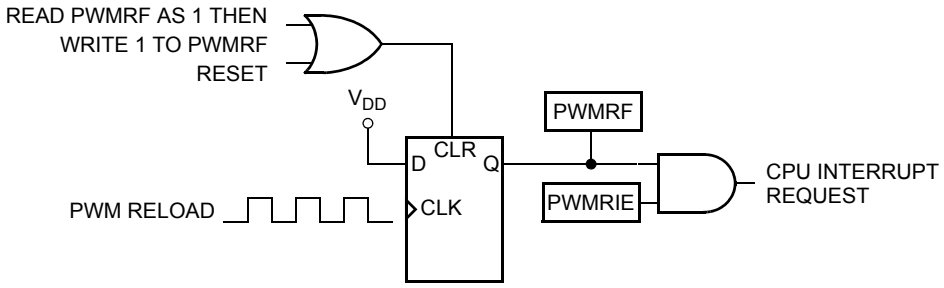


Figure 15-75. PWMRF Reload Interrupt Request

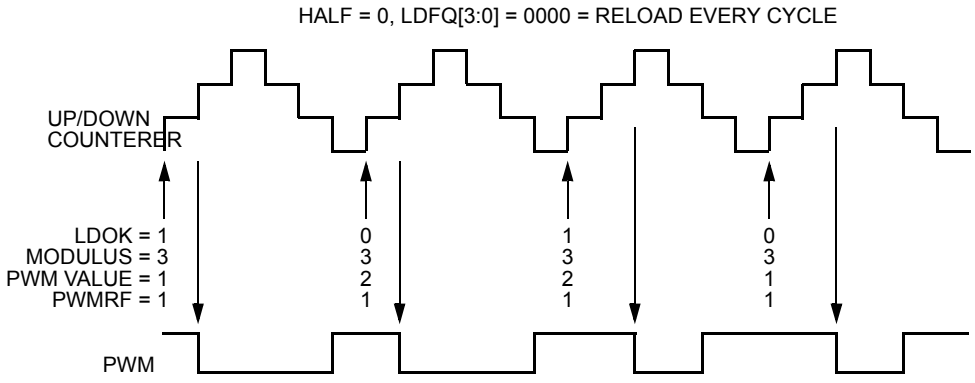


Figure 15-76. Full-Cycle Center-Aligned PWM Value Loading

the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. Mode fault error doesn't occur in slave mode.

If a mode fault error occurs, the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So SCK, MISO, and MOSI pins are forced to be high impedance inputs to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for a SPI system configured in master mode, output enable of the MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to SPI control register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

NOTE

If a mode fault error occurs and a received data byte is pending in the receive shift register, this data byte will be lost.

17.4.7 Low Power Mode Options

17.4.7.1 SPI in Run Mode

In run mode with the SPI system enable (SPE) bit in the SPI control register clear, the SPI system is in a low-power, disabled state. SPI registers remain accessible, but clocks to the core of this module are disabled.

17.4.7.2 SPI in Wait Mode

SPI operation in wait mode depends upon the state of the SPISWAI bit in SPI control register 2.

- If SPISWAI is clear, the SPI operates normally when the CPU is in wait mode
- If SPISWAI is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
  - If SPISWAI is set and the SPI is configured for master, any transmission and reception in progress stops at wait mode entry. The transmission and reception resumes when the SPI exits wait mode.
  - If SPISWAI is set and the SPI is configured as a slave, any transmission and reception in progress continues if the SCK continues to be driven from the master. This keeps the slave synchronized to the master and the SCK.

    If the master transmits several bytes while the slave is in wait mode, the slave will continue to send out bytes consistent with the operation mode at the start of wait mode (i.e., if the slave is currently sending its SPIDR to the master, it will continue to send the same byte. Else if the slave is currently sending the last received byte from the master, it will continue to send each previous master byte).

18.2 External Signal Description

18.2.1 HD — High-Side Drain Connection

This pin is the power supply for the 3-phase bridge (DC-link voltage).

NOTE

The HD pin should be connected as near as possible to the drain connections of the high-side MOSFETs.

18.2.2 VBS[2:0] — Bootstrap Capacitor Connection Pins

The pins are the bootstrap capacitor connections for phases HS[2:0]. The capacitor is connected between HS[2:0] and this pin. The bootstrap capacitor provides the gate voltage and current to drive the gate of the external power FET.

18.2.3 HG[2:0] — High-Side Gate Pins

The pins are the gate drives for the high-side power FETs. The drivers provide a high current with low impedance to turn on and off the high-side power FETs.

18.2.4 HS[2:0] — High-Side Source Pins

The pins are the source connection for the high-side power FETs and the drain connection for the low-side power FETs. The low voltage end of the bootstrap capacitor is also connected to this pin.

18.2.5 VLS[2:0] — Voltage Supply for Low-Side Pre-Drivers

The pins are the voltage supply pins for the three low-side FET pre-drivers. These pins should be connected to the voltage regulator output pin VLS_OUT. The output voltage on VLS_OUT pin is typically V_{VLS}=11V.

NOTE

It is recommended to add a 110nF-220nF X7R ceramic capacitor close to each VLS pin.

18.2.6 LG[2:0] — Low-Side Gate Pins

The pins are the gate drives for the low-side power FETs. The drivers provide a high current with low impedance to turn on and off the the low-side power FETs.

18.2.7 LD[2:0] — Low-Side Gate Pins (only on GDUV6)

These pins are the drain connections for the low-side power FETs.

19.4 Functional Description

19.4.1 General

The LIN/HV Physical Layer module implements the physical layer of the LIN/HV interface. In the LIN version, this physical layer can be driven by the SCI (Serial Communication Interface) module or directly through the LPDR register.In the HV Phy version, the input can be routed to an internal timer to measure the frequency and duty cycle of the PWM input signal. If required, the output can directly be controlled by the LPDR register, e.g. to send diagnostic feedback.

19.4.2 Slew Rate and LIN Mode Selection

The slew rate can be selected for Electromagnetic Compatibility (EMC) optimized operation at 10.4 kbit/s and 20 kbit/s as well as at fast baud rate (up to 250 kbit/s) for test and programming. The slew rate can be chosen with the bits LPSLR[1:0] in the LIN Slew Rate Mode Register (LPSLRM). The default slew rate corresponds to 20 kbit/s.

In the HV Phy version, the TxD-dominant timeout must be disabled (LPDTDIS=1) in order e.g. to transmit a PWM pulse.

Changing the slew rate (LPSLRM Register) during transmission is not allowed in order to avoid unwanted effects. To change the register, the LIN/HV Physical Layer must first be disabled (LPE=0). Once it is updated, the LIN/HV Physical Layer can be enabled again.

NOTE

For 20 kbit/s and Fast Mode communication speeds, the corresponding slew rate ***MUST*** be set; otherwise, the communication is not guaranteed (violation of the specified LIN duty cycles). For 10.4 kbit/s, the 20 kbit/s slew rate ***can*** be set but the EMC performance is worse. The up to 250 kbit/s slew rate must be chosen ***ONLY*** for fast mode, not for any of the 10.4 kbit/s or 20 kbit/s LIN compliant communication speeds.

19.4.2.1 10.4 kbit/s and 20 kbit/s

When the slew rate is chosen for 10.4 kbit/s or 20 kbit/s communication, a control loop is activated within the module to make the rise and fall times of the LIN bus independent from VLINSUP and the load on the bus.

19.4.2.2 Fast Mode (not LIN compliant)

Choosing this slew rate allows baud rates up to 250 kbit/s by having much steeper edges (please refer to electricals). As for the 10.4 kbit/s and 20 kbit/s modes, the slope control loop is also engaged. This mode is used for fast communication only, and the LIN electricals are not supported (for example, the LIN duty cycles).

20.6 Initialization

On each system reset the flash module executes an initialization sequence which establishes initial values for the Flash Block Configuration Parameters, the FPROT and DFPROT protection registers, and the FOPT and FSEC registers. The initialization routine reverts to built-in default values that leave the module in a fully protected and secured state if errors are encountered during execution of the reset sequence. If a double bit fault is detected during the reset sequence, both MGSTAT bits in the FSTAT register will be set.

CCIF is cleared throughout the initialization sequence. The Flash module holds off all CPU access for a portion of the initialization sequence. Flash reads are allowed once the hold is removed. Completion of the initialization sequence is marked by setting CCIF high which enables user commands.

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

Appendix C
ADC Electrical Specifications

NOTE: ADC1 is only tested to 10-bit accuracy in the 48LQFP-EP package options.

NOTE: VRL_0 is the preferred reference for low noise.

NOTE: (ZVMC256 only) When using VDDS2 or VDDS1 as the VRH reference, the reference is impacted by a drop of between 4mV and 15mV across the internal short circuit protection switch.

C.1 ADC Operating Characteristics

The Table C-1 shows conditions under which the ADC operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$.

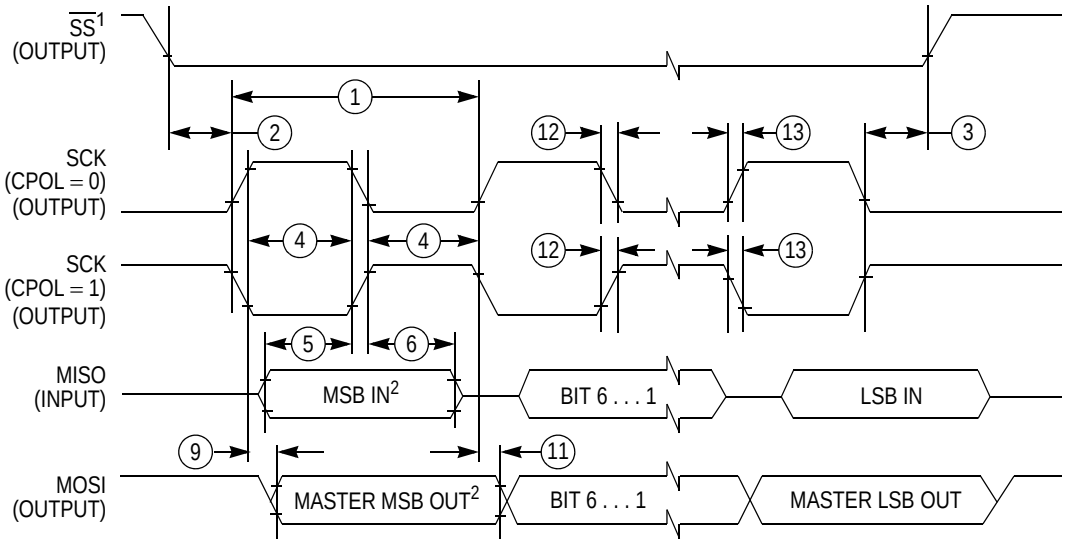
This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table C-1. ADC Operating Characteristics

Supply voltage 4.5 V < V_{DDA} < 5.5 V, Junction Temperature From –40×°C To +175°C							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Reference potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$	 — —	 $V_{DDA}/2$ V_{DDA}	 V V
2		Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	-0.1	0	0.1	V
3		Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.1	0	0.1	V
4		Differential reference voltage[1]	V_{RH}-V_{RL}	3.13	5.0	5.5	V
5		ADC Clock Frequency (derived from bus clock via the prescaler).	f_{ATDCLK}	0.25	—	8.33	MHz
6		Buffer amplifier turn on time (delay after module start/recovery from Stop mode)	t_{REC}	—	—	1	μs
7		ADC disable time	$t_{DISABLE}$	—	—	3	bus clock cycles
8		ADC Conversion Period [2] 12 bit resolution: 10 bit resolution: 8 bit resolution:	 N_{CONV12} N_{CONV10} N_{CONV8}	 19 18 16	 — — —	 39 38 36	 ADC clock cycles

1. Full accuracy is not guaranteed when differential voltage is less than 4.50 V

2. The minimum time assumes a sample time of 4 ATD clock cycles; maximum time assumes a sample time of 24 ATD clock cycles.



1. If enabled.

2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-3. SPI Master Timing (CPHA=1)

Table I-1. SPI Master Mode Timing Characteristics (Junction Temperature From -40°C To +175°C)

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1		SCK Frequency	f_{sck}	1/2048	—	$1/2^{(1)(2)}$	f_{bus}
1		SCK Period	t_{sck}	2	—	2048	t_{bus}
2		Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3		Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4		Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5		Data Setup Time (Inputs)	t_{su}	4	—	—	ns
6		Data Hold Time (Inputs)	t_{hi}	5	—	—	ns
9		Data Valid after SCK Edge	t_{vsck}	—	—	10	ns
10		Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	9	ns
11		Data Hold Time (Outputs)	t_{ho}	-1.2	—	—	ns
12		Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13		Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

1. See **Figure I-4.**

2. f_{bus} max is 40MHz at temperatures above 150°C

M.8 0x0400-0x042F TIM1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0400	TIM1TIOS	R W							IOS1	IOS0
0x0401	TIM1CFORC	R W							0 FOC1	0 FOC0
0x0402	Reserved	R W								
0x0403	Reserved	R W								
0x0404	TIM1TCNTH	R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
0x0405	TIM1TCNTL	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
0x0406	TIM1TSCR1	R W	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
0x0407	TIM1TTOV	R W							TOV1	TOV0
0x0408	TIM1TCTL1	R W								
0x0409	TIM1TCTL2	R W					OM1	OL1	OM0	OL0
0x040A	TIM1TCTL3	R W								
0x040B	TIM1TCTL4	R W					EDG1B	EDG1A	EDG0B	EDG0A
0x040C	TIM1TIE	R W							C1I	C0I
0x040D	TIM1TSCR2	R W	TOI	0	0	0		PR2	PR1	PR0
0x040E	TIM1TFLG1	R W							C1F	C0F
0x040F	TIM1TFLG2	R W	TOF	0	0	0	0	0	0	0
0x0410	TIM1TC0H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0411	TIM1TC0L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0529	PMFFQCB	R	LDFQB				HALFB	PRSCB		PWMRFB
		W								
0x052A	PMFCNTB	R	0	PMFCNTB						
		W								
0x052B	PMFCNTB	R	PMFCNTB							
		W								
0x052C	PMFMODB	R	0	PMFMODB						
		W								
0x052D	PMFMODB	R	PMFMODB							
		W								
0x052E	PMFDTMB	R	0	0	0	0	PMFDTMB			
		W								
0x052F	PMFDTMB	R	PMFDTMB							
		W								
0x0530	PMFENCC	R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
		W								
0x0531	PMFFQCC	R	LDFQC				HALFC	PRSCC		PWMRFC
		W								
0x0532	PMFCNTC	R	0	PMFCNTC						
		W								
0x0533	PMFCNTC	R	PMFCNTC							
		W								
0x0534	PMFMODC	R	0	PMFMODC						
		W								
0x0535	PMFMODC	R	PMFMODC							
		W								
0x0536	PMFDTMC	R	0	0	0	0	PMFDTMC			
		W								
0x0537	PMFDTMC	R	PMFDTMC							
		W								
0x0538	PMFDMP0	R	DMP05		DMP04		DMP03	DMP02	DMP01	DMP00
		W								
0x0539	PMFDMP1	R	DMP15		DMP14		DMP13	DMP12	DMP11	DMP10
		W								