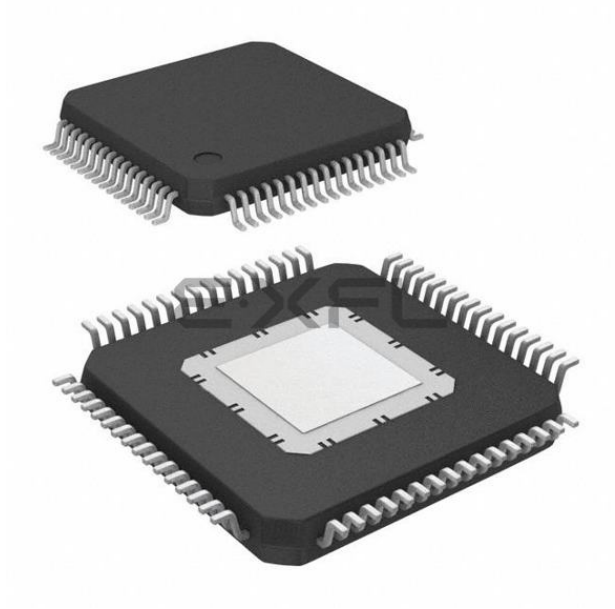

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f3mkh

The exposed pad on the package bottom must be connected to a grounded contact pad on the PCB.

The LIN0 pin is mapped to the HV physical interface

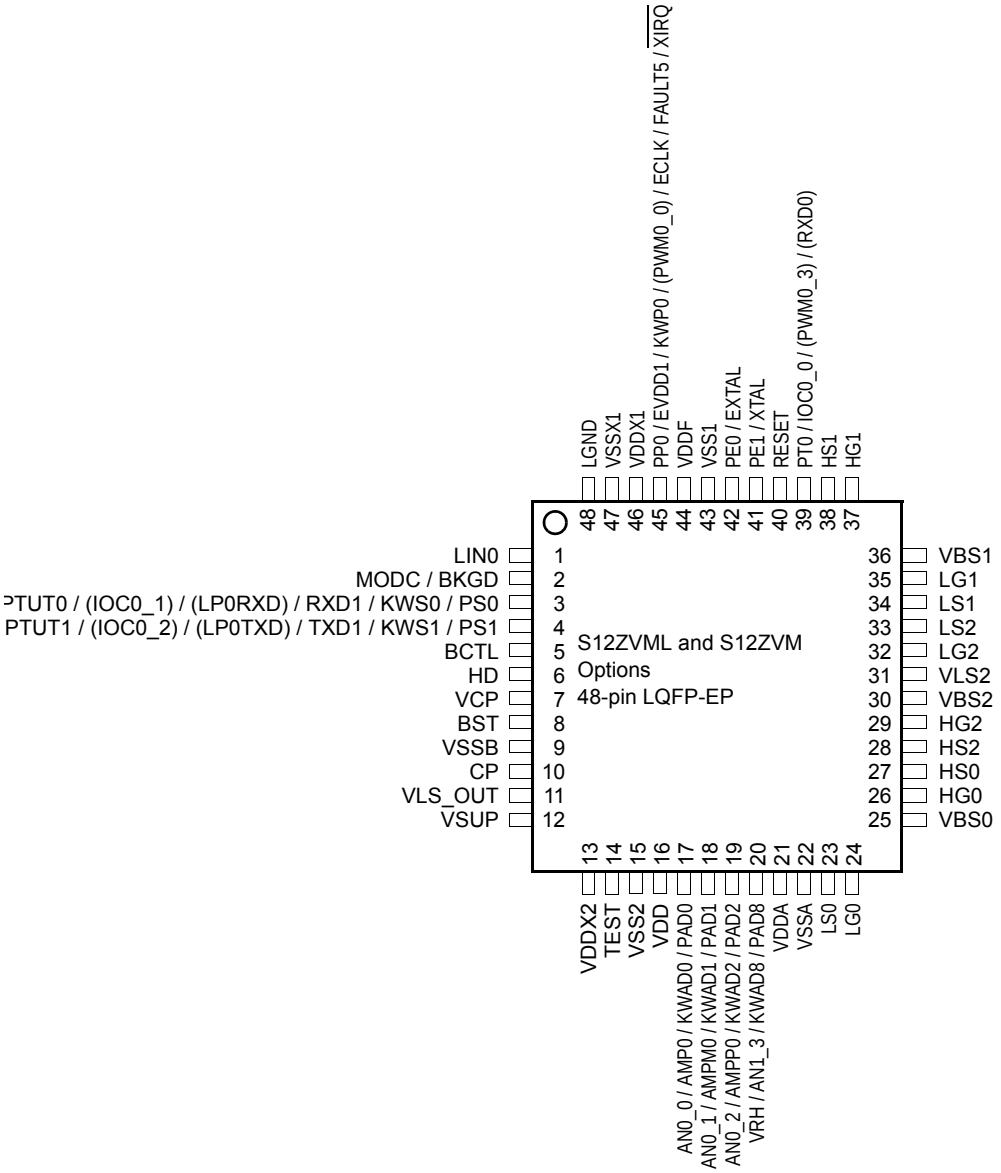

Figure 1-6. S12ZVM, S12ZVML Option 48-pin LQFP

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02D6	PIES	R	0	0	PIES5[5]	PIES4[5]	PIES3	PIES2	PIES1	PIES0
		W								
0x02D7	PIFS	R	0	0	PIFS5[5]	PIFS4[5]	PIFS3	PIFS2	PIFS1	PIFS0
		W								
0x02D8–0x02DE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02DF	WOMS	R	0	0	WOMS5[5]	WOMS4[5]	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x02E0–0x02EF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F0	PTP	R	0	0	0	0	0	PTP2[5]	PTP1	PTP0
		W								
0x02F1	PTIP	R	0	0	0	0	0	PTIP2[5]	PTIP1	PTIP0
		W								
0x02F2	DDRP	R	0	0	0	0	0	DDRP2[5]	DDRP1	DDRP0
		W								
0x02F3	PERP	R	0	0	0	0	0	PERP2[5]	PERP1	PERP0
		W								
0x02F4	PPSP	R	0	0	0	0	0	PPSP2[5]	PPSP1	PPSP0
		W								
0x02F5	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F6	PIEP	R	OCIE1	0	0	0	0	PIEP2[5]	PIEP1	PIEP0
		W								
0x02F7	PIFP	R	OCIF1	0	0	0	0	PIFP2[5]	PIFP1	PIFP0
		W								

2.3.2.3 Module Routing Register 2 (MODRR2)

Address 0x0202 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	T0C2RR1-0[2]		T0C1RR[2]	T1IC0RR[3]	T0IC3RR1-0		T0IC1RR	T0IC1RR0[2]
	IOC0_2		IOC0_1	IC1_0	TIM0 IC3		TIM0 IC1	TIM0 IC1
Reset	0	0	0	0	0	0	0	0

Figure 2-5. Module Routing Register 2 (MODRR2)

1. Read: Anytime
   Write: Once in normal, anytime in special mode
2. Only available for ZVMC256, ZVML31, ZVM32, and ZVM16
3. Only available for ZVMC256

Table 2-13. MODRR2 Routing Register Field Descriptions

Field	Description
7-6 T0C2RR1-0	**Module Routing Register** — TIM0 IOC0_2 routing (ZVMC256, ZVML31, ZVM32, and ZVM16 only) 11 reserved 10[1] TIM0 IC0_2 is routed to the HVI, OC0_2 is disconnected from GPIO 01 TIM0 IOC0_2 is routed to PS1 00 TIM0 IOC0_2 is routed to PT2
5 T0C1RR	**Module Routing Register** — TIM0 IOC0_1 routing (ZVMC256, ZVML31, ZVM32, and ZVM16 only) 1 TIM0 IOC0_1 is routed to PS0 0 TIM0 IOC0_1 is routed to PT1
4 T1IC0RR	**Module Routing Register** — TIM1 IOC1_0 routing (ZVMC256 only) 1 TIM1 IOC1_0 is routed to the GDU delay measurement feature (t_{delon}) 0 TIM1 IOC1_0 is routed to PS2
3-2 T0IC3RR1-0	**Module Routing Register** — TIM0 IC3 routing One out of four different sources can be selected as input to timer channel 3. 11 TIM0 input capture channel 3 is connected to ACLK 10 TIM0 input capture channel 3 is connected to RXD1 01 TIM0 input capture channel 3 is connected to RXD0 00 TIM0 input capture channel 3 is connected to PT3

Table 5-6. BDCCSRL Field Descriptions (continued)

Field	Description
0 ILLCMD	**Illegal Command Flag** — Indicates an illegal BDC command. This bit is set in the following cases: When an unimplemented BDC command opcode is received. When a DUMP_MEM{_WS}, FILL_MEM{_WS} or READ_SAME{_WS} is attempted in an illegal sequence. When an active BDM command is received whilst BDM is not active When a non Always-available command is received whilst the BDC is disabled or a flash mass erase is ongoing. When a non Always-available command is received whilst the device is secure Read commands return a value of 0xEE for each data byte Writing a “1” to this bit, clears the bit. 0 No illegal command detected. 1 Illegal BDC command detected.

5.4 Functional Description

5.4.1 Security

If the device resets with the system secured, the device clears the BDCCSR UNSEC bit. In the secure state BDC access is restricted to the BDCCSR register. A mass erase can be requested using the ERASE_FLASH command. If the mass erase is completed successfully, the device programs the security bits to the unsecure state and sets the BDC UNSEC bit. If the mass erase is unsuccessful, the device remains secure and the UNSEC bit is not set.

For more information regarding security, please refer to device specific security information.

5.4.2 Enabling BDC And Entering Active BDM

BDM can be activated only after being enabled. BDC is enabled by setting the ENBDC bit in the BDCCSR register, via the single-wire interface, using the command WRITE_BDCCSR.

After being enabled, BDM is activated by one of the following[1]:

- The BDC BACKGROUND command
- A CPU BGND instruction
- The DBG Breakpoint mechanism

Alternatively BDM can be activated directly from reset when resetting into Special Single Chip Mode.

The BDC is ready for receiving the first command 10 core clock cycles after the deassertion of the internal reset signal. This is delayed relative to the external pin reset as specified in the device reset documentation. On S12Z devices an NVM initialization phase follows reset. During this phase the BDC commands classified as always available are carried out immediately, whereas other BDC commands are subject to delayed response due to the NVM initialization phase.

NOTE

After resetting into SSC mode, the initial PC address must be supplied by the host using the WRITE_Rn command before issuing the GO command.

1. BDM active immediately out of special single-chip reset.

Table 6-23. DBGEFR Field Descriptions

Field	Description
4 EEVF	**External Event Flag** — Indicates the occurrence of an external event during the debug session. 0 No external event 1 External event
3–0 ME[3:0]	**Match Event[3:0]**— Indicates a comparator match event on the corresponding comparator channel**.**

6.3.2.11 Debug Status Register (DBGSR)

Address: 0x010B

	7	6	5	4	3	2	1	0
R	TBF	0	0	PTACT	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-13. Debug Status Register (DBGSR)

Read: Anytime.

Write: Never.

Table 6-24. DBGSR Field Descriptions

Field	Description
7 TBF	**Trace Buffer Full** — The TBF bit indicates that the trace buffer has been filled with data since it was last armed. If this bit is set, then all trace buffer lines contain valid data, regardless of the value of DBGCNT bits CNT[6:0]. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit
4 PTACT	**Profiling Transmission Active** — The PTACT bit, when set, indicates that the profiling transmission is still active. When clear, PTACT then profiling transmission is not active. The PTACT bit is set when profiling begins with the first PTS format entry to the trace buffer. The PTACT bit is cleared when the profiling transmission ends.
2–0 SSF[2:0]	**State Sequencer Flag Bits** — The SSF bits indicate the current State Sequencer state. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal event, then the state sequencer returns to State0 and these bits are cleared to indicate that State0 was entered during the session. On arming the module the state sequencer enters State1 and these bits are forced to SSF[2:0] = 001. See Table 6-25**.**

Table 6-25. SSF[2:0] — State Sequence Flag Bit Encoding

SSF[2:0]	Current State
000	State0 (disarmed)
001	State1
010	State2
011	State3

9.5.2 Register Descriptions

This section describes in address order all the ADC12B_LBA registers and their individual bits.

9.5.2.1 ADC Control Register 0 (ADCCTL_0)

Module Base + 0x0000

	15	14	13	12	11	10	9	8
R W	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-4. ADC Control Register 0 (ADCCTL_0)

Read: Anytime

Write:

- Bits ADC_EN, ADC_SR, FRZ_MOD and SWAI writable anytime
- Bits MOD_CFG, STR_SEQA and ACC_CFG[1:0] writable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-3. ADCCTL_0 Field Descriptions

Field	Description
15 ADC_EN	**ADC Enable Bit** — This bit enables the ADC (e.g. sample buffer amplifier etc.) and controls accessibility of ADC register bits. When this bit gets cleared any ongoing conversion sequence will be aborted and pending results or the result of current conversion gets discarded (not stored). The ADC cannot be re-enabled before any pending action or action in process is finished or aborted, which could take up to a maximum latency time of $t_{DISABLE}$ (see device reference manual for more details). Because internal components of the ADC are turned on/off with this bit, the ADC requires a recovery time period (t_{REC}) after ADC is enabled until the first conversion can be launched via a trigger. 0 ADC disabled. 1 ADC enabled.
14 ADC_SR	ADC Soft-Reset — This bit causes an ADC Soft-Reset if set after a severe error occurred (see list of severe errors in Section 9.5.2.9, “ADC Error Interrupt Flag Register (ADCEIF) that causes the ADC to cease operation). It clears all overrun flags and error flags and forces the ADC state machine to its idle state. It also clears the Command Index Register, the Result Index Register, and the CSL_SEL and RVL_SEL bits (to be ready for a new control sequence to load new command and start execution again from top of selected CSL). A severe error occurs if an error flag is set which cause the ADC to cease operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. Once this bit is set it can not be cleared by writing any value. It is cleared only by ADC hardware after the Soft-Reset has been executed. 0 No ADC Soft-Reset issued. 1 Issue ADC Soft-Reset.
13 FRZ_MOD	Freeze Mode Configuration — This bit influences conversion flow during Freeze Mode. 0 ADC continues conversion in Freeze Mode. 1 ADC freezes the conversion at next conversion boundary at Freeze Mode entry.
12 SWAI	Wait Mode Configuration — This bit influences conversion flow during Wait Mode. 0 ADC continues conversion in Wait Mode. 1 ADC halts the conversion at next conversion boundary at Wait Mode entry.

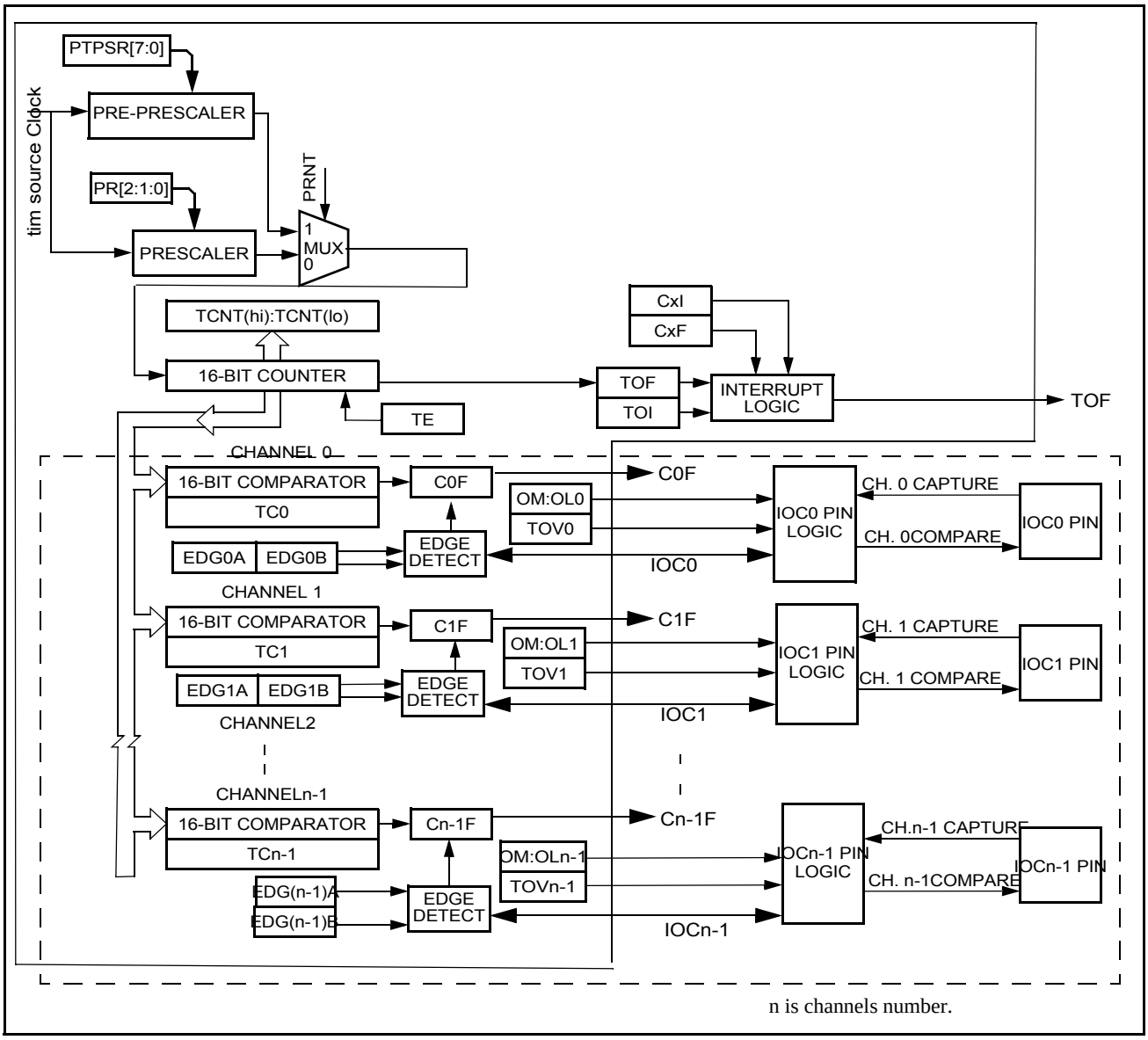

Figure 11-22. Detailed Timer Block Diagram

11.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

12.3.2.6 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 12-10. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 12-11. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 12-6. TCTL1/TCTL2 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
1:0 OMx	**Output Mode** — These two pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.
1:0 OLx	**Output Level** — These two pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.

Table 12-7. Compare Result Output Action

OMx	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0009 TG0TVL	R	TG0TV[7:0]							
	W								
0x000A TG1LIST	R	0	0	0	0	0	0	0	TG1LIST
	W								
0x000B TG1TNUM	R	0	0	0	TG1TNUM[4:0]				
	W								
0x000C TG1TVH	R	TG1TV[15:8]							
	W								
0x000D TG1TVL	R	TG1TV[7:0]							
	W								
0x000E PTUCNTH	R	PTUCNT[15:8]							
	W								
0x000F PTUCNTL	R	PTUCNT[7:0]							
	W								
0x0010 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0011 PTUPTRH	R	PTUPTR[23:16]							
	W								
0x0012 PTUPTRM	R	PTUPTR[15:8]							
	W								
0x0013 PTUPTRL	R	PTUPTR[7:1]							0
	W								
0x0014 TG0L0IDX	R	0	TG0L10DX[6:0]						
	W								
0x0015 TG0L1IDX	R	0	TG0L1IDX[6:0]						
	W								
0x0016 TG1L0IDX	R	0	TG1L0IDX[6:0]						
	W								
0x0017 TG1L1IDX	R	0	TG1L1IDX[6:0]						
	W								

= Unimplemented

Figure 14-2. PTU Register Summary

Table 15-9. PMFCFG3 Field Descriptions (continued)

Field	Description
4–3 VLMODE [1:0]	**Value Register Load Mode** — This field determines the way the value registers are being loaded. This register cannot be modified after the WP bit is set. 00 Each value register is accessed independently 01 Writing to value register zero also writes to value registers one to five 10 Writing to value register zero also writes to value registers one to three 11 Reserved (defaults to independent access)
2 PINVC	**PWM Invert Complement Source Pair C** — This bit controls PWM4/PWM5 pair. When set, this bit inverts the COMPSRCC signal. This bit has no effect in independent mode. **Note:** PINVC is buffered. The value written does not take effect until the LDOK bit or global load OK is set and the next PWM load cycle begins. Reading PINVC returns the value in the buffer and not necessarily the value in use. 0 No inversion 1 COMPSRCC inverted only in complementary mode
1 PINVB	**PWM Invert Complement Source Pair B** — This bit controls PWM2/PWM3 pair. When set, this bit inverts the COMPSRCB signal. This bit has no effect in independent mode. **Note:** PINVB is buffered. The value written does not take effect until the LDOK bit or global load OK is set and the next PWM load cycle begins. Reading PINVB returns the value in the buffer and not necessarily the value in use. 0 No inversion 1 COMPSRCB inverted only in complementary mode
0 PINVA	**PWM Invert Complement Source Pair A** — This bit controls PWM0/PWM1 pair. When set, this bit inverts the COMPSRCA signal. This bit has no effect on in independent mode. **Note:** PINVA is buffered. The value written does not take effect until the LDOKA bit or global load OK is set and the next PWM load cycle begins. Reading PINVA returns the value in the buffer and not necessarily the value in use. 0 No inversion 1 COMPSRCA inverted only in complementary mode

15.3.2.5 PMF Fault Enable Register (PMFFEN)

Address: Module Base + 0x0004 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	FEN5	0	FEN4	FEN3	FEN2	FEN1	FEN0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-7. PMF Fault Enable Register (PMFFEN)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

Table 15-18. Software Output Control

OUT*n* Bit	Complementary Channel Operation	Independent Channel Operation
OUT0	1 — PWM0 is active 0 — PWM0 is inactive	1 — PWM0 is active 0 — PWM0 is inactive
OUT1	1 — PWM1 is complement of PWM0 0 — PWM1 is inactive	1 — PWM1 is active 0 — PWM1 is inactive
OUT2	1 — PWM2 is active 0 — PWM2 is inactive	1 — PWM2 is active 0 — PWM2 is inactive
OUT3	1 — PWM3 is complement of PWM2 0 — PWM3 is inactive	1 — PWM3 is active 0 — PWM3 is inactive
OUT4	1 — PWM4 is active 0 — PWM4 is inactive	1 — PWM4 is active 0 — PWM4 is inactive
OUT5	1 — PWM5 is complement of PWM4 0 — PWM5 is inactive	1 — PWM5 is active 0 — PWM5 is inactive

15.3.2.12 PMF Deadtime Sample Register (PMFDTMS)

Address: Module Base + 0x000E

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	DT5	DT4	DT3	DT2	DT1	DT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-15. PMF Deadtime Sample Register (PMFDTMS)

1. Read: Anytime
   Write: Never

Table 15-19. PMFDTMS Field Descriptions

Field	Description
5–0 DT[5:0]	**DT*n* Bits** — The DT*n* bits are grouped in pairs, DT0 and DT1, DT2 and DT3, DT4 and DT5. Each pair reflects the corresponding $\overline{IS}$ input value as sampled at the end of deadtime. *n* is 0, 1, 2, 3, 4 and 5.

15.3.2.13 PMF Correction Control Register (PMFCCTL)

Address: Module Base + 0x000F

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	ISENS		0	IPOLC	IPOLB	IPOLA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-16. PMF Correction Control Register (PMFCCTL)

15.4 Functional Description

15.4.1 Block Diagram

A block diagram of the PMF is shown in Figure 15-1**.** The MTG bit allows the use of multiple PWM generators (A, B, and C) or just a single generator (A). PWM0 and PWM1 constitute Pair A, PWM2 and PWM3 constitute Pair B, and PWM4 and PWM5 constitute Pair C.

Figure 15-41 depicts Pair A signal paths of PWM0 and PWM1. Pairs B and C have the same structure.

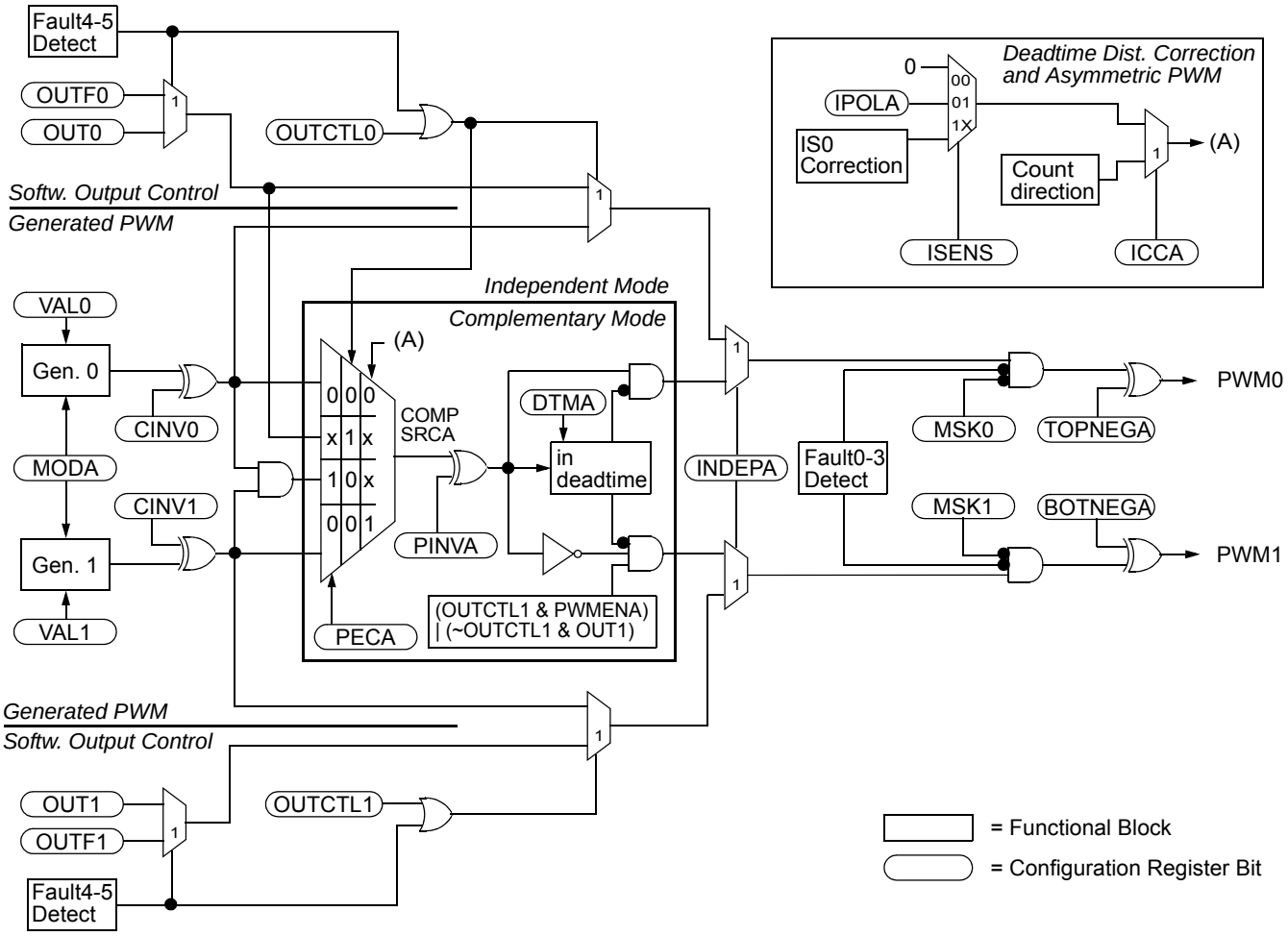

Figure 15-41. Detail of PWM0 and PWM1 Signal Paths

NOTE

It is possible to have both channels of a complementary pair to be high. For example, if the TOPNEGA (negative polarity for PWM0), BOTNEGA (negative polarity for PWM1), MSK0 and MSK1 bits are set, both the PWM complementary outputs of generator A will be high. See Section 15.3.2.2, “PMF Configure 1 Register (PMFCFG1)” for the description of TOPNEG and BOTNEG bits, and Section 15.3.2.3, “PMF Configure 2 Register (PMFCFG2)” for the description of the MSK0 and MSK1 bits.

18.3.2.9 GDU Boost Current Limit Register (GDUBCL)

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	GBCL[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-11. GDU Boost Current Limit Register (GDUBCL)

1. Read: Anytime
   Write: Anytime if GWP=0

Table 18-12. GDU Boost Current Limit Register Field Descriptions

Field	Description
GBCL[3:0]	GDU Boost Current Limit Register— These bits are used to adjust the boost coil current limit $I_{COIL0,16}$ on the BST pin. These bits cannot be modified after GWP bit is set. See GDU electrical parameters.

18.3.2.10 GDU Phase Mux Register (GDUPHMUX)

Module Base + 0x0009 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	GPHMX[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-12. GDU Phase Mux Register (GDUPHMUX)

1. Read: Anytime
   Write: Anytime

Table 18-13. GDU Phase Mux Register Field Descriptions

Field	Description
[1:0] GPHMUX	GDU Phase Multiplexer — These buffered bits are used to select the voltage which is routed to internal ADC channel.The value written to the GDUPHMUX register does not take effect until the LDOK bit is set and the next PWM reload cycle begins. Reading GDUPHMUX register reads the value in the buffer. It is not necessary the value which is currently used. 00 Pin HD selected , V_{HD} / 12 connected to ADC channel 01 Pin HS0 selected , V_{HS0} / 6 connected to ADC channel 10 Pin HS1 selected , V_{HS1} / 6 connected to ADC channel 11 Pin HS2 selected, V_{HS2} / 6 connected to ADC channel

Table 20-27. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Register	Byte	FCCOB Parameter Fields (NVM Command Mode)
011	FCCOB3	HI	Data 1 [15:8]
		LO	Data 1 [7:0]
100	FCCOB4	HI	Data 2 [15:8]
		LO	Data 2 [7:0]
101	FCCOB5	HI	Data 3 [15:8]
		LO	Data 3 [7:0]

20.4 Functional Description

20.4.1 Modes of Operation

The module provides the modes of operation normal and special. The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and DFPROT registers (see Table 20-29).

20.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x1F_C0B6. The contents of the word are defined in Table 20-28.

Table 20-28. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

20.4.3 Flash Block Read Access

If data read from the Flash block results in a double-bit fault ECC error (meaning that data is detected to be in error and cannot be corrected), the read data will be tagged as invalid during that access (please look

to VSSC via high-ohmic input resistors of the receiver. The SPLIT pin as well as the internal mid-point reference are set to high-impedance.

Shutdown mode cannot be re-entered until reset.

21.5.2.2 Normal Mode

In normal mode the full transceiver functionality is available. In this mode, the CAN bus is controlled by the CPTXD input and the CAN bus state (recessive, dominant) is reported on the CPRXD output. The voltage failure, over-current and CPTXD-dominant timeout monitors are enabled. The SPLIT pin is driving a 2.5 V bias if enabled. The internal mid-point reference is set to 2.5 V.

If CPTXD is high, the transmit driver is set into recessive state, and CANH and CANL lines are biased to the voltage set at VDDC divided by 2, approx. 2.5 V.

If CPTXD is low, the transmit driver is set into dominant state, and CANH and CANL drivers are active. CANL is pulled low and CANH is pulled high.

The receiver reports the bus state on CPRXD. If the differential voltage V_{CANH} minus V_{CANL} at CANH and CANL is below the internal threshold, the bus is recessive and CPRXD is set high, otherwise a dominant bus is detected and CPRXD is set low.

When detecting a voltage high failure, over-current or CPTXD-dominant timeout event the CAN Physical Layer enters listen-only mode. A voltage low failure on CANL results in entering pseudo-normal mode. A voltage low failure on CANH maintains normal mode.

NOTE

After entering normal mode from shutdown or standby mode a settling time of t_{CP_set} must have passed until flags can be considered as valid.

21.5.2.3 Pseudo-Normal Mode

Pseudo-normal mode is identical to normal mode except for CANL driver being disabled as a result of a voltage low failure that has been detected on the CANL bus line (CPCLVL=1). CANH remains functional in this mode to allow transmission. Normal mode will automatically be re-entered after the error condition has ceased.

21.5.2.4 Listen-only Mode

Listen-only mode is entered upon detecting a CAN bus error condition (except for CPCLVL=1) or CPTXD-dominant timeout event. The entire transmitter is forced off. All other functions of the normal mode are maintained.

Application software action is required to re-enter normal mode by clearing the related flags if the bus error condition was caused by an over-current (refer to 21.6.3). In case of a voltage failure, normal mode will automatically be re-entered if the condition has passed. If the listen-only mode was caused by CPTXD-dominant timeout event, the related flag can only be cleared after the CPTXD has returned to recessive level.

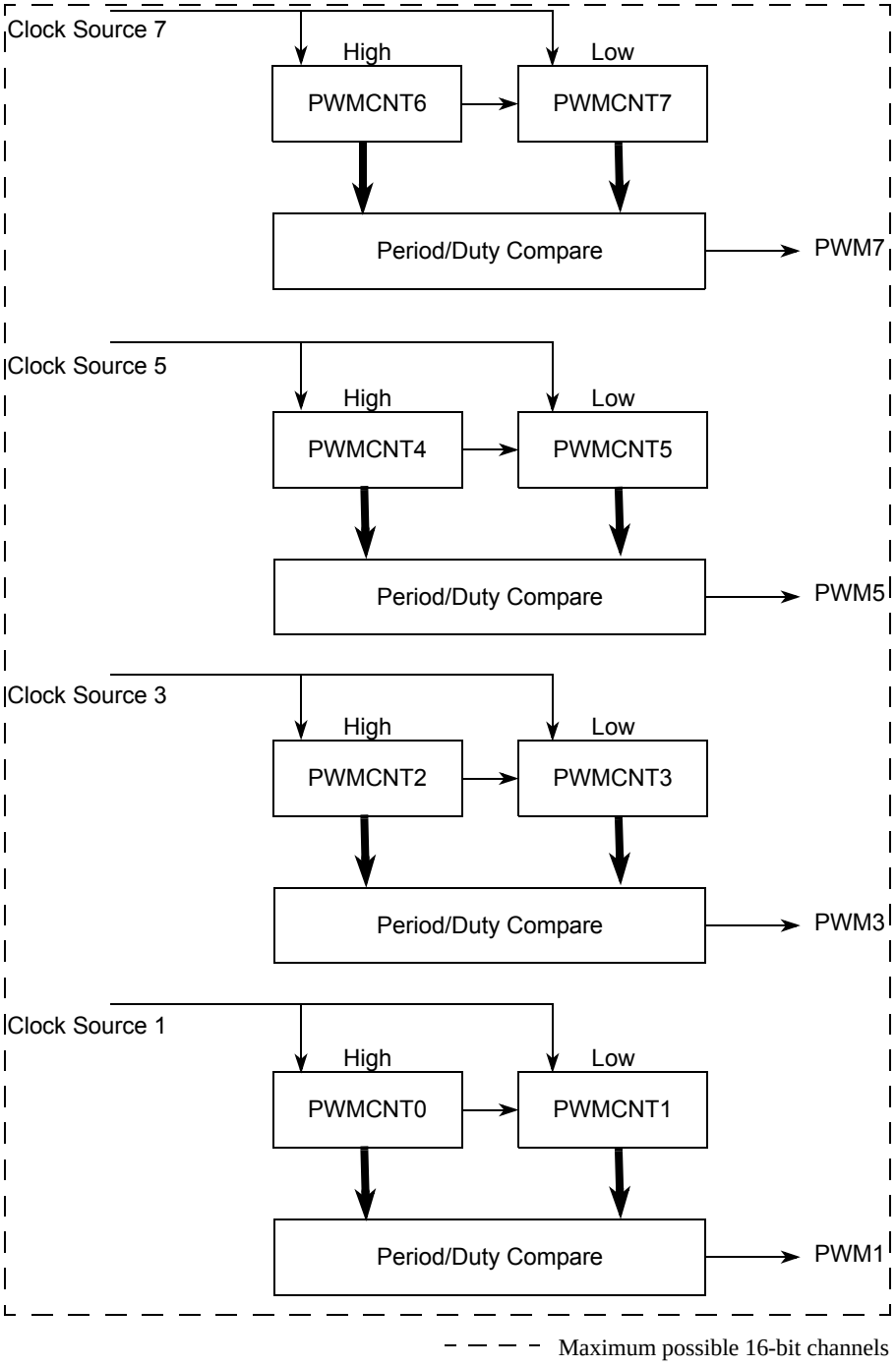

Figure 22-21. PWM 16-Bit Mode

Once concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low order PWMEx bit. In this case, the high order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

B.3 IRC and OSC Electrical Specifications

Table B-4. IRC electrical characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1a		Junction Temperature - 40 to 150 Celsius Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.9895	1.002	1.0145	MHz
1b		Junction Temperature 150 to 175 Celsius Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.9855	—	1.0145	MHz

Table B-5. OSC electrical characteristics (Junction Temperature From –40°C To +175°C)

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1		Nominal crystal or resonator frequency	f_{OSC}	4.0	—	20	MHz
2		Startup Current	i_{OSC}	100	—	—	μA
3a		Oscillator start-up time (4MHz)(1)	t_{UPOSC}	—	2	10	ms
3b		Oscillator start-up time (8MHz)[1]	t_{UPOSC}	—	1.6	8	ms
3c		Oscillator start-up time (16MHz)[1]	t_{UPOSC}	—	1	5	ms
3d		Oscillator start-up time (20MHz)[1]	t_{UPOSC}	—	1	4	ms
4		Clock Monitor Failure Assert Frequency	f_{CMFA}	200	450	1200	KHz
5		Input Capacitance (EXTAL, XTAL pins)	C_{IN}	—	7	—	pF
6		EXTAL Pin Input Hysteresis	$V_{HYS,EXTAL}$	—	120	—	mV
7		EXTAL Pin oscillation amplitude (loop controlled Pierce)	$V_{PP,EXTAL}$	—	1.0	—	V
8		EXTAL Pin oscillation required amplitude(2)	$V_{PP,EXTAL}$	0.8	—	1.5	V

1. These values apply for carefully designed PCB layouts with capacitors that match the crystal/resonator requirements.

2. Needs to be measured at room temperature on the application board using a probe with very low (<=5pF) input capacitance.

B.4 Phase Locked Loop

B.4.1 Jitter Information

With each transition of the feedback clock, the deviation from the reference clock is measured and the input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the VCOCLK frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure B-1.**.

Table H-2. Static Electrical Characteristics

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
5	Input Resistance	R_{IN}	5	32.5	50	kΩ
6	Differential Input Resistance	R_{IND}	10	65	100	kΩ
7	Common mode input resistance matching	R_{INM}	-3	0	+3	%
8	CANH Output Voltage (R_L = 60Ω), (Normal mode) TXD Dominant State TXD Recessive State	V_{CANH}	 2.75 2.0	 3.5 2.5	 4.5 3.0	 V V
9	CANL Output Voltage (R_L = 60Ω), (Normal mode) TXD Dominant State TXD Recessive State	V_{CANL}	 0.5 2.0	 1.5 2.5	 2.25 3.0	 V V
10	Differential Output Voltage (R_L = 60Ω), (Normal mode) TXD Dominant State TXD Recessive State	V_{OH} - V_{OL}	 1.5 -0.5	 2.0 0	 3.0 0.05	 V V
11	CANH, CANL driver symmetry (Normal mode) (V_{CANH} + V_{CANL}) / VDDC	V_{SYM}	0.9	1	1.1	—
12	Output Current Capability (Dominant State) CANH CANL	 I_{CANH} I_{CANL}	 —	 55 55	 —	 mA mA
13	CANH, CANL Overcurrent Detection (Tj >=25^{O}C) CANH CANL	 I_{CANHOC} I_{CANLOC}	 70 70	 85 85	 100 100	 mA mA
14	CANH, CANL Output Voltage (no load, Standby mode) CANH CANL	 V_{CANH} V_{CANL}	 -0.1 -0.1	 0 0	 0.1 0.1	 V V
15	CANH and CANL Input Current (Standby mode) V_{CANH}, V_{CANL} from 0 V to 5.0 V V_{CANH}, V_{CANL} = - 2.0 V V_{CANH}, V_{CANL} = 7.0 V	I_{CAN1}	—	—	20 -75 250	uA uA uA
16	CANH and CANL Input Current (Device unsupplied) (VSUP tied to ground or left open) V_{CANH}, V_{CANL} from 0V to 5 V V_{CANH}, V_{CANL} = - 2.0 V V_{CANH}, V_{CANL} = 7.0 V	I_{CAN2}	—	—	10 -75 250	uA uA uA
17	CANH, CANL Input capacitance (Normal mode) CANH CANL	 C_{CANH} C_{CANL}	 —	 14 16	 —	 pF pF
18	CANH to CANL differential capacitance (Normal mode)	C_{HLDIFF}	—	6	—	pF
DIAGNOSTIC INFORMATION (CANH AND CANL)						
15	CANL to 0 V Threshold	V_{L0}	-0.75	-0.15	0	V
16	CANH to 0 V Threshold	V_{H0}	-0.75	-0.15	0	V

Appendix M
Detailed Register Address Map

Registers listed are a superset of all registers in the S12ZVM-Family.

The device overview section specifies module (version) assignment to individual devices.

M.1 0x0000–0x0003 Part ID

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	PARTID0	R	0	0	0	0	0	0	0	0
		W								
0x0001	PARTID1	R	0	0	0	1	Derivative Dependent (see Table 1-6)			
		W								
0x0002	PARTID2	R	0	0	0	0	0	0	0	0
		W								
0x0003	PARTID3	R	Revision Dependent							
		W								

M.2 0x0010–0x001F S12ZINT

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	IVBR	R	IVB_ADDR[15:8]							
		W								
0x0011		R	IVB_ADDR[7:1]							0
		W								
0x0012-0x0016	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0017	INT_CFADDR	R	0	INT_CFADDR[6:3]				0	0	0
		W								
0x0018	INT_CFDATA0	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x0019	INT_CFDATA1	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001A	INT_CFDATA2	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001B	INT_CFDATA3	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001C	INT_CFDATA4	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001D	INT_CFDATA5	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001E	INT_CFDATA6	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0284	DDRADH	R	DDRADH7[2]	DDRADH6[2]	DDRADH5[2]	DDRADH4[2]	DDRADH3[2]	DDRADH2[2]	DDRADL1[2]	DDRADH0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	PERADH	R	PERADH7[2]	PERADH6[2]	PERADH5[2]	PERADH4[2]	PERADH3[2]	PERADH2[2]	PERADH1[2]	PERADH0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	PPSADH	R	PPSADH7[2]	PPSADH6[2]	PPSADH5[2]	PPSADH4[2]	PPSADH3[2]	PPSADH2[2]	PPSADH1[2]	PPSADH0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								
0x028A–0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	PIEADH	R	PIEADH7[2]	PIEADH6[2]	PIEADH5[2]	PIEADH4[2]	PIEADH3[2]	PIEADH2[2]	PIEADH1[2]	PIEADH0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								
0x028E	PIFADH	R	PIFADH7[2]	PIFADH6[2]	PIFADH5[2]	PIFADH4[2]	PIFADH3[2]	PIFADH2[2]	PIFADH1[2]	PIFADH0
		W								
0x028F	PIFADL	R	PIFADL7	PIFADL6	PIFADL5	PIFADL4	PIFADL3	PIFADL2	PIFADL1	PIFADL0
		W								
0x0290–0x0297	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0298	DIENADH	R	DIENADH7[2]	DIENADH6[2]	DIENADH5[2]	DIENADH4[2]	DIENADH3[2]	DIENADH2[2]	DIENADH1[2]	DIENADH0
		W								
0x0299	DIENADL	R	DIENADL7	DIENADL6	DIENADL5	DIENADL4	DIENADL3	DIENADL2	DIENADL1	DIENADL0
		W								