E·XFL



Welcome to <u>E-XFL.COM</u>

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f3vkh

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Chapter 2 Port Integration Module (S12ZVMPIMV3)

• Port AD

GPIO/KWU	ADC1	ADC0	SPI0	GDU	PTU	DBG	Pins
PTADH7		AN0_7				PDOCLK -	PAD15 ¹
PTADH6		AN0_6				PDO —	PAD14 ¹
PTADH5		AN0_5			PTURE		PAD13 ¹
PTADH4	AN1_7						PAD12 ¹
PTADH3	AN1_6						PAD11 ¹
PTADH2	AN1_5						PAD10 ¹
PTADH1	AN1_4						PAD9 ¹
PTADH0	AN1_3	VRH ²					PAD8
PTADL7	AN1_2			AMPP1			PAD7
PTADL6	AN1_1		<u>SS0</u>	AMPM1			PAD6
PTADL5	AN1_0			AMP1			PAD5
PTADL4		AN0_4					PAD4
PTADL3		AN0_3					PAD3
PTADL2		AN0_2		AMPP0			PAD2
PTADL1		AN0_1		AMPM0			PAD1
PTADL0		AN0_0		AMP0			PAD0
				L			

1. Only available for ZVMC256

2. Not available for ZVMC256

Most I/O pins can be configured by register bits to select data direction and to enable and select pullup or pulldown devices.

Chapter 4 Interrupt (S12ZINTV0)



1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001F



1. Please refer to the notes following the PRIOLVL[2:0] description below.

Read: Anytime

Write: Anytime

Table 4-6. INT_CFDATA0-7 Field Descriptions

Field	Description
2–0 PRIOLVL[2:0]	 Interrupt Request Priority Level Bits — The PRIOLVL[2:0] bits configure the interrupt request priority level of the associated interrupt request. Out of reset all interrupt requests are enabled at the lowest active level ("1"). Please also refer to Table 4-7 for available interrupt request priority levels. Note: Write accesses to configuration data registers of unused interrupt channels are ignored and read accesses return all 0s. For information about what interrupt channels are used in a specific MCU, please refer to the Device Reference Manual for that MCU.
	Note: When non I-bit maskable request vectors are selected, writes to the corresponding INT_CFDATA registers are ignored and read accesses return all 0s. The corresponding vectors do not have configuration data registers associated with them.
	Note: Write accesses to the configuration register for the spurious interrupt vector request (vector base + 0x0001DC) are ignored and read accesses return 0x07 (request is handled by the CPU, PRIOLVL = 7).

Table	4-7.	Interrup	t Priority	v Levels
Tuble	-	micinup		

Priority	PRIOLVL2	PRIOLVL1	PRIOLVL0	Meaning
	0	0	0	Interrupt request is disabled
low	0	0	1	Priority level 1
	0	1	0	Priority level 2
	0	1	1	Priority level 3

5.4.4.20 STEP1 Step1 Active Background 0x09 $host \rightarrow A$ target CK

This command is used to step through application code. In active BDM this command executes the next CPU instruction in application code. If enabled an ACK is driven.

If a STEP1 command is issued and the CPU is not halted, the command is ignored.

Using STEP1 to step through a CPU WAI instruction is explained in Section 5.1.3.3.2.

5.4.5 BDC Access Of Internal Resources

Unsuccessful read accesses of internal resources return a value of 0xEE for each data byte. This enables a debugger to recognize a potential error, even if neither the ACK handshaking protocol nor a status command is currently being executed. The value of 0xEE is returned in the following cases.

- Illegal address access, whereby ILLACC is set
- Invalid READ_SAME or DUMP_MEM sequence
- Invalid READ_Rn command (BDM inactive or CRN incorrect)
- Internal resource read with timeout, whereby NORESP is set

5.4.5.1 BDC Access Of CPU Registers

The CRN field of the READ_Rn and WRITE_Rn commands contains a pointer to the CPU registers. The mapping of CRN to CPU registers is shown in Table 5-9. Accesses to CPU registers are always 32-bits wide, regardless of implemented register width. This means that the BDC data transmission for these commands is 32-bits long. The valid bits of the transfer are listed in the Valid Data Bits column. The other bits of the transmission are redundant.

Attempted accesses of CPU registers using a CRN of 0xD,0xE or 0xF is invalid, returning the value 0xEE for each byte and setting the ILLACC bit.

CPU Register	Valid Data Bits	Command	Opcode	Command	Opcode
D0	[7:0]	WRITE_D0	0x40	READ_D0	0x60
D1	[7:0]	WRITE_D1	0x41	READ_D1	0x61
D2	[15:0]	WRITE_D2	0x42	READ_D2	0x62
D3	[15:0]	WRITE_D3	0x43	READ_D3	0x63
D4	[15:0]	WRITE_D4	0x44	READ_D4	0x64
D5	[15:0]	WRITE_D5	0x45	READ_D5	0x65
D6	[31:0]	WRITE_D6	0x46	READ_D6	0x66

Table 5-9. CPU Register Number (CRN) Mapping

MC9S12ZVM Family Reference Manual Rev. 2.11

Chapter 5 Background Debug Controller (S12ZBDCV2)

to start the bit up to one target clock cycle earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 5-6 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD pin. Internal glitch detect logic requires the pin be driven high no later than eight target clock cycles after the falling edge for a logic 1 transmission.

Since the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.



Figure 5-6. BDC Host-to-Target Serial Bit Timing

Figure 5-7 shows the host receiving a logic 1 from the target system. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive at the latest after 6 clock cycles, before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

6.3.2.4 Debug Trace Control Register Low (DBGTCRL)

Address: 0x0103



Figure 6-6. Debug Trace Control Register Low (DBGTCRL)

Read: Anytime.

Write: Anytime the module is disarmed and PTACT is clear.

This register configures the profiling and timestamp features

Table 6-13. DBGTCRL Field Descriptions

Field	Description
4 PREND	 Profiling End — This bit, when set, forces the profiling session to end when the trace buffer has been filled. This prevents a rollover of the trace buffer from overwriting the initial entry containing the start address 0 Trace buffer rollover is enabled during profiling. After the last line has been filled, the entries continue, starting at line0 and overwriting the older data 1 Trace buffer rollover is disabled during profiling. When the trace buffer is full, the profiling session ends, the PTBOVF bit is set and the ARM bit is cleared.
3 DSTAMP	 Comparator D Timestamp Enable — This bit, when set, enables Comparator D matches to generate timestamps in Detail, Normal and Loop1 trace modes. 0 Comparator D match does not generate timestamp 1 Comparator D match generates timestamp if timestamp function is enabled
2 PDOE	 Profile Data Out Enable — This bit, when set, configures the device profiling pins for profiling. 0 Device pins not configured for profiling 1 Device pins configured for profiling
1 PROFILE	Profile Enable — This bit, when set, enables the profile function, whereby a subsequent arming of the DBG activates profiling. When PROFILE is set, the TRCMOD bits are ignored. 0 Profile function disabled 1 Profile function enabled
0 STAMP	Timestamp Enable — This bit, when set, enables the timestamp function. The timestamp function adds a timestamp to each trace buffer entry in Detail, Normal and Loop1 trace modes. 0 Timestamp function disabled 1 Timestamp function enabled

Chapter 7 ECC Generation Module (SRAM_ECCV1)

Rev. No. (Item No.)	Date	Sections Affected	Substantial Change(s)
V01.00	15-Oct-13	all	Initial Module Version
V01.10	19-March-15	7.3.1	add feature description for S12ZVMC256 in case of non-aligned write to memory data word containing a double bit ECC error

Table 7-1. Revision History Table

7.1 Introduction

The purpose of ECC logic is to detect and correct as much as possible memory data bit errors. These soft errors, mainly generated by alpha radiation, can occur randomly during operation. "Soft error" means that only the information inside the memory cell is corrupt; the memory cell itself is not damaged. A write access with correct data solves the issue. If the ECC algorithm is able to correct the data, then the system can use this corrected data without any issues. If the ECC algorithm is able to detect, but not correct the error, then the system is able to ignore the memory read data to avoid system malfunction.

The ECC value is calculated based on an aligned 2 byte memory data word. The ECC algorithm is able to detect and correct single bit ECC errors. Double bit ECC errors will be detected but the system is not able to correct these errors. This kind of ECC code is called SECDED code. This ECC code requires 6 additional parity bits for each 2 byte data word.

7.1.1 Features

The SRAM_ECC module provides the ECC logic for the system memory based on a SECDED algorithm. The SRAM_ECC module includes the following features:

- SECDED ECC code
 - Single bit error detection and correction per 2 byte data word
 - Double bit error detection per 2 byte data word
- Memory initialization function
- Byte wide system memory write access
- Automatic single bit ECC error correction for read and write accesses
- Debug logic to read and write raw use data and ECC values

Chapter 7 ECC Generation Module (SRAM_ECCV1)

7.2.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field functions follow the register diagrams, in bit order.

7.2.2.1 ECC Status Register (ECCSTAT)



Write: Never

Figure 7-2. ECC Status Register (ECCSTAT)

Table 7-2. ECCSTAT Field Description

Field	Description
0 RDY	ECC Ready— Shows the status of the ECC module. 0 Internal SRAM initialization is ongoing, access to the SRAM is disabled 1 Internal SRAM initialization is done, access to the SRAM is enabled

7.2.2.2 ECC Interrupt Enable Register (ECCIE)

Access: User read/write⁽¹⁾ Module Base + 0x00001 7 6 5 4 3 2 1 0 R 0 0 0 0 0 0 0 SBEEIE W 0 0 0 0 0 0 0 0 Reset

1. Read: Anytime Write: Anytime

Figure 7-3. ECC Interrupt Enable Register (ECCIE)

Table 7-3. ECCIE Field Description

Field	Description
0 SBEEIE	Single bit ECC Error Interrupt Enable — Enables Single ECC Error interrupt. 0 Interrupt request is disabled 1 Interrupt will be requested whenever SBEEIF is set

MC9S12ZVM Family Reference Manual Rev. 2.11

8.1.1 Differences between S12CPMU_UHV_V10 and S12CPMU_UHV_V6

- The following device pins exist only in V10: VDDS1, VDDS2, BCTLS1, BCTLS2, SNPS1, SNPS2,
- The feature of switching VDDS1/2 to VRH1/2 (which connects to ADC) exists only in V10
- The following register and bits exist only in V10: CPMUVREGCTL register: Bits VRH2EN, VRH1EN, EXTS1ON, EXTS2ON CPMULVCTL register: Bit VDDSIE CPMUVDDS register
- The VDDS Integrity Interrupt only exists in V10

9.5.2.13 ADC Intermediate Result Information Register (ADCIMDRI)

This register is cleared when bit ADC_SR is set or bit ADC_EN is clear.

Module Base + 0x000E



Read: Anytime

Write: Never

Field	Description
15 CSL_IMD	 Active CSL At Intermediate Event — This bit indicates the active (used) CSL at the occurrence of a conversion interrupt flag (CON_IF[15:1]) (occurrence of an intermediate result buffer fill event) or when a Sequence Abort Event gets executed. 0 CSL_0 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set. 1 CSL_1 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set.
14 RVL_IMD	 Active RVL At Intermediate Event — This bit indicates the active (used) RVL buffer at the occurrence of a conversion interrupt flag (CON_IF[15:1]) (occurrence of an intermediate result buffer fill event) or when a Sequence Abort Event gets executed. 0 RVL_0 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set. 1 RVL_1 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set.
5-0 RIDX_IMD[5:0]	RES_IDX Value At Intermediate Event — These bits indicate the result index (RES_IDX) value at the occurrence of a conversion interrupt flag (CON_IF[15:1]) (occurrence of an intermediate result buffer fill event) or occurrence of EOL_IF flag or when a Sequence Abort Event gets executed to abort an ongoing conversion (the result index RES_IDX is captured at the occurrence of a result data store).
	 When a Sequence Abort Event has been processed flag SEQAD_IF is set and the RES_IDX value of the last stored result is provided. Hence in case an ongoing conversion is aborted the RES_IDX value captured in RIDX_IMD bits depends on bit STORE_SEQA: STORE_SEQA =1: The result index of the aborted conversion is provided STORE_SEQA =0: The result index of the last stored result at abort execution time is provided In case a CSL is aborted while no conversion is ongoing (ADC waiting for a Trigger Event) the last captured result index is provided. In case a Sequence Abort Event was initiated by hardware due to MCU entering Stop Mode or Wait Mode with bit SWAI set, the result index of the last stored result is captured by bits RIDX_IMD but flag SEQAD_IF is not set

Table 9-18. ADCIMDRI Field Descriptions

The comparator outputs BVLC and BVHC are forced to zero if the comparator is disabled (configuration bit BSUSE is cleared). If the software disables the comparator during a high or low Voltage condition (BVHC or BVLC active), then an additional interrupt is generated. To avoid this behavior the software must disable the interrupt generation before disabling the comparator.

The BATS interrupt vector is named in Table 10-6. Vector addresses and interrupt priorities are defined at MCU level.

The module internal interrupt sources are combined into one module interrupt signal.

Table 10-6. BATS Interrupt Sources

Module Interrupt Source	Module Interrupt Source Module Internal Interrupt Source	
BATS Interrupt (BATI)	BATS Voltage Low Condition Interrupt (BVLI)	BVLIE = 1
	BATS Voltage High Condition Interrupt (BVHI)	BVHIE = 1

10.4.2.1 BATS Voltage Low Condition Interrupt (BVLI)

To use the Voltage Low Interrupt the Level Sensing must be enabled (BSUSE =1).

If measured when

a) V_{LBI1} selected with BVLS[1:0] = 0x0

 $V_{measure} < V_{LBI1_A}$ (falling edge) or $V_{measure} < V_{LBI1_D}$ (rising edge)

or when

b) V_{LBI2} selected with BVLS[1:0] = 0x1 at pin VSUP
 V_{measure} < V_{LBI2} A (falling edge) or V_{measure} < V_{LBI2} D (rising edge)

or when

c) V_{LBI3} selected with BVLS[1:0] = 0x2 V_{measure} < V_{LBI3_A} (falling edge) or V_{measure} < V_{LBI3_D} (rising edge)

or when

d) V_{LBI4} selected with BVLS[1:0] = 0x3
 V_{measure} < V_{LBI4_A} (falling edge) or V_{measure} < V_{LBI4_D} (rising edge)

then BVLC is set. BVLC status bit indicates that a low voltage at pin VSUP is present. The Low Voltage Interrupt flag (BVLIF) is set to 1 when the Voltage Low Condition (BVLC) changes state. The Interrupt flag BVLIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVLIE the module requests an interrupt to MCU (BATI).

10.4.2.2 BATS Voltage High Condition Interrupt (BVHI)

To use the Voltage High Interrupt the Level Sensing must be enabled (BSUSE=1).

MC9S12ZVM Family Reference Manual Rev. 2.11

Field	Description
6-4 TSEG2[2:0]	Time Segment 2 — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 13-44). Time segment 2 (TSEG2) values are programmable as shown in Table 13-8.
3-0 TSEG1[3:0]	Time Segment 1 — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 13-44). Time segment 1 (TSEG1) values are programmable as shown in Table 13-9.

Table 13-7. CANBTR1 Register Field Descriptions (continued)

1. In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

TSEG22	TSEG21	TSEG20	Time Segment 2
0	0	0	1 Tq clock cycle ⁽¹⁾
0	0	1	2 Tq clock cycles
:	:	:	:
1	1	0	7 Tq clock cycles
1	1	1	8 Tq clock cycles

Table 13-8. Time Segment 2 Values	Table	13-8.	Time	Segment	2	Values
-----------------------------------	-------	-------	------	---------	---	--------

1. This setting is not valid. Please refer to Table 13-36 for valid settings.

TSEG13	TSEG12	TSEG11	TSEG10	Time segment 1
0	0	0	0	1 Tq clock cycle ⁽¹⁾
0	0	0	1	2 Tq clock cycles ¹
0	0	1	0	3 Tq clock cycles ¹
0	0	1	1	4 Tq clock cycles
:	:	:	:	:
1	1	1	0	15 Tq clock cycles
1	1	1	1	16 Tq clock cycles

Table 13-9. Time Segment 1 Values

1. This setting is not valid. Please refer to Table 13-36 for valid settings.

The bit time is determined by the oscillator frequency, the baud rate prescaler, and the number of time quanta (Tq) clock cycles per bit (as shown in Table 13-8 and Table 13-9).

Eqn. 13-1

Bit Time= $\frac{(Prescaler value)}{f_{CANCLK}} \cdot (1 + TimeSegment1 + TimeSegment2)$



13.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

	7	6	5	4	3	2	1	0
R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reset:	x	x	x	x	x	x	x	x

Figure 13-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Field	Description
7-0 DB[7:0]	Data bits 7-0

15.3.2.22 PMF Counter Modulo A Register (PMFMODA)



1. Read: Anytime

Write: Anytime. Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKA bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODA returns the value in the buffer. It is not necessarily the value the PWM generator A is currently using.

15.3.2.23 PMF Deadtime A Register (PMFDTMA)



1. Read: Anytime

Write: This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to the maximum value of 0x0FFF, selecting a deadtime of 4095 PWM clock cycles. Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows:

$$T_{DEAD_A} = PMFDTMA / f_{PWM_A} = PMFDTMA \times P_A \times T_{core}$$
 Eqn. 15-1

Chapter 16 Serial Communication Interface (S12SCIV6)

16.2 External Signal Description

The SCI module has a total of two external pins.

16.2.1 TXD — Transmit Pin

The TXD pin transmits SCI (standard or infrared) data. It will idle high in either mode and is high impedance anytime the transmitter is disabled.

16.2.2 RXD — Receive Pin

The RXD pin receives SCI (standard or infrared) data. An idle line is detected as a line high. This input is ignored when the receiver is disabled and should be terminated to a known voltage.

16.3 Memory Map and Register Definition

This section provides a detailed description of all the SCI registers.

16.3.1 Module Memory Map and Register Definition

The memory map for the SCI module is given below in Figure 16-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the SCI module and the address offset for each register.

16.4.6.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the actual stop bit. A noise error will occur if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error will occur if the receiver clock is misaligned in such a way that the majority of the RT8, RT9, and RT10 stop bit samples are a logic zero.

As the receiver samples an incoming frame, it re-synchronizes the RT clock on any valid falling edge within the frame. Re synchronization within frames will correct a misalignment between transmitter bit times and receiver bit times.

16.4.6.5.1 Slow Data Tolerance

Figure 16-28 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.



Figure 16-28. Slow Data

Let's take RTr as receiver RT clock and RTt as transmitter RT clock.

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles +7 RTr cycles = 151 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 16-28, the receiver counts 151 RTr cycles at the point when the count of the transmitting device is 9 bit times x 16 RTt cycles = 144 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data character with no errors is:

 $((151 - 144) / 151) \ge 100 = 4.63\%$

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 7 RTr cycles = 167 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 16-28, the receiver counts 167 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

 $((167 - 160) / 167) \ge 100 = 4.19\%$

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	R	0	0	0	0	0	0		LPDR0
LPDR	W								
0x0001	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
LFOR	vv								
0x0002 Reserved	R W	Reserved							
0x0003	R		0	0	0	0	0		
LPSLRM	W							LPSLRT	LPSLR0
0x0004 Reserved	R W	Reserved							
0x0005	R	LPDT	0	0	0	0	0	0	0
LPSR	W								
0x0006	R			0	0	0	0	0	0
LPIE	W	LFDTIE	LFOCIE						
0x0007	R			0	0	0	0	0	0
LPIF	W		LFUGIF						

Figure 19-2. Register Summary

that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 20-4.

Global Address	Size (Bytes)	Description	
0xFF_FE00-0xFF_FE07	8	Backdoor Comparison Key Refer to Section 20.4.7.11, "Verify Backdoor Access Key Command," and Section 20.5.1, "Unsecuring the MCU using Backdoor Key Access"	
0xFF_FE08-0xFF_FE09 ¹	2	Protection Override Comparison Key. Refer to Section 20.4.7.17, "Protection Override Command"	
0xFF_FE0A- 0xFF_FE0B ⁽¹⁾	2	Reserved	
0xFF_FE0C ¹	1	P-Flash Protection byte. Refer to Section 20.3.2.9, "P-Flash Protection Register (FPROT)"	
0xFF_FE0D ¹	1	EEPROM Protection byte. Refer to Section 20.3.2.10, "EEPROM Protection Register (DFPROT)"	
0xFF_FE0E ¹	1	Flash Nonvolatile byte Refer to Section 20.3.2.11, "Flash Option Register (FOPT)"	
0xFF_FE0F ¹	1	Flash Security byte Refer to Section 20.3.2.2, "Flash Security Register (FSEC)"	

Table 20	-4. Flash	Configuration	Field
----------	-----------	---------------	-------

1. 0xFF_FE08-0xFF_FE0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0xFF_FE0A - 0xFF_FE0B reserved field should be programmed to 0xFF.

Chapter 20 Flash Module (S12ZFTMRZ)



MC9S12ZVM Family Reference Manual Rev. 2.11



Figure 22-21. PWM 16-Bit Mode

Once concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low order PWMEx bit. In this case, the high order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

Table A-16. CPMU Cor	nfiguration for Run/Wait an	d Full Stop Current Measurement
----------------------	-----------------------------	---------------------------------

CPMU REGISTER Bit settings/Conditions					
API settings for STOP current measurement					
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0				
CPMUACLKTR	trimmed to >=20Khz				
CPMUAPIRH/RL	set to 0xFFFF				

Table A-17. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
SCI	Continuously transmit data (0x55) at speed of 19200 baud
SPI	Configured to master mode, continuously transmit data (0x55) at 1Mbit/s
ADC	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on a single input channel
MSCAN	Configured in loop back mode with a bit rate of 500kbit/s.
DBG	The module is disabled, as in typical final applications
PTU	The module is enabled, bits TG1EN and TG0EN are set. PTUFRE is also set to generate automatic reload events.
PMF	The module is configured with a modulus rate of 10 kHz
TIM	The peripheral is configured to output compare mode,
GDU	LDO enabled. Charge pump enabled. Current sense0 enabled. Boost disabled. No output activity (too load dependent)
COP & RTI	Enabled
BATS	Enabled
LINPHY	Connected to SCI and continuously transmit data (0x55) at speed of 19200 baud
CANPHY (ZVMC256)	Enabled and connected to MSCAN module