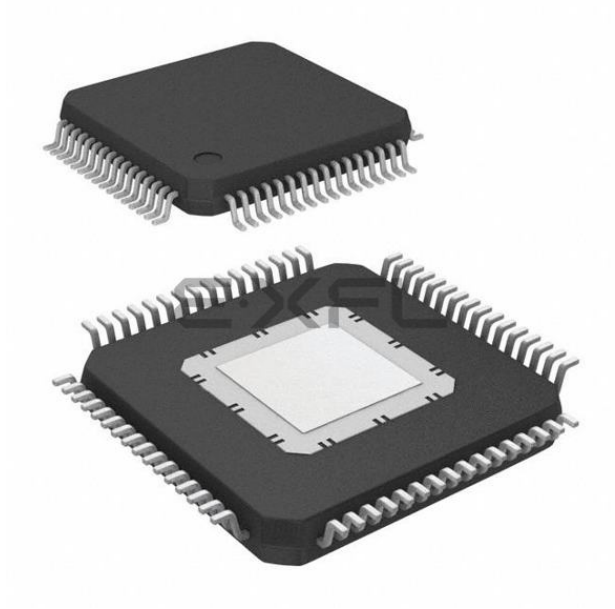

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvmc64f3wkh

Table 1-9. Pin Summary For 80-Pin Package Option (ZVMC256 Only) (Sheet 5 of 5)

Pin #	Pin Name	Function (Priority and routing options defined in PIM chapter)							Supply	Internal Pull Resistor	
		1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.		CTRL	Reset State
71	PS1	KWS1	TXD1	SCK0	PTUT1	CPDR0	TXCAN 0	IOC0_2	V_{DDX}	PERS/ PPSS	Up
72	PS0	KWS0	RXD1	$\overline{SS0}$	PTUT0	RXCAN 0	IOC0_1	—	V_{DDX}	PERS/ PPSS	Up
73	VDDF	—	—	—	—	—	—	—	V_{DDF}	—	—
74	VSS1	—	—	—	—	—	—	—	V_{DD}	—	—
75	VDD	—	—	—	—	—	—	—	V_{DD}	—	—
76	PP1	KWP1	PWM1_ 1	PWM0_ 1	IRQ	—	—	—	V_{DDX}	PPRP/ PPSP	Off
77	PP0/ EVDD1	KWP0	PWM1_ 5	ECLK	FAULT5	XIRQ	—	—	V_{DDX}	PPRP/ PPSP	Off
78	VDDX1	—	—	—	—	—	—	—	V_{DDX}	—	—
79	VSSX1	—	—	—	—	—	—	—	V_{DDX}	—	—
80	BKGD	MODC	—	—	—	—	—	—	V_{DDX}	—	Up

1.8 Internal Signal Mapping

This section specifies the mapping of inter-module signals at device level.

1.8.1 ADC Connectivity

1.8.1.1 ADC Reference Voltages

The ZVMC256 includes ADC12B_LBA V3 which features VRH_2, VRH_1, VRH_0 and VRL_0. On these devices for each ADC instance VRH_0 is mapped to VDDA, VRH_1 is mapped to VDDS1 and VRH_2 is mapped to VDDS2. VRL_0 is mapped to VSSA. Both VDDS1 and VDDS2 must be enabled by bits in the CPMUVREGCTL register before they can be used as references. When using VDDS1 or VDDS2 as VRH reference, the reference is impacted by a voltage drop across the internal short circuit protection switch. This is specified in Section C.1.1.5.

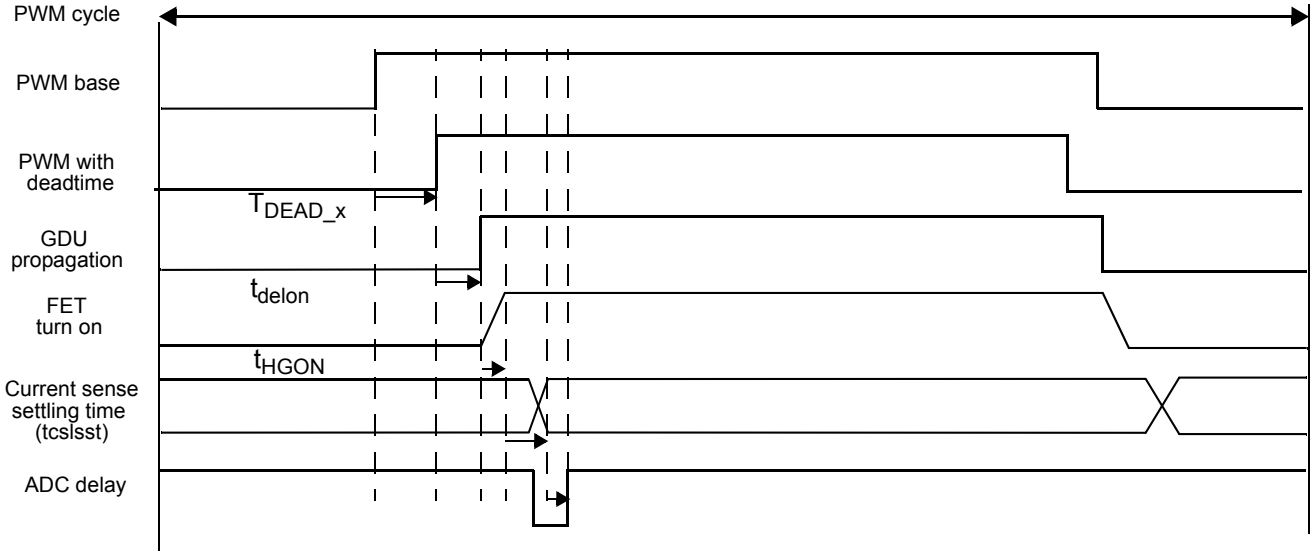
All other devices in the family include ADC12B_LBA V1, which features VRH_1, VRH_0, VRL_1 and VRL_0. On these devices, for both ADC instances, VRL_0 and VRL_1 are mapped to VSSA, whereby VRL_0 is the preferred reference for low noise. For both ADC instances VRH_1 is mapped to VDDA and VRH_0 is mapped to PAD8.

1.13.3.2 Control Loop Timing Considerations

Delays within the separate control loop elements require consideration to ensure correct synchronization.

Regarding the raw PWM0 signal as the starting point and stepping through the control loop stages, the factors shown in Figure 1-10 contribute to delays within the control loop, starting with the deadtime insertion, going through the external FETs and back into the internal ADC measurements of external voltages and currents.

Figure 1-10. Control Loop Delay Overview



The PWM deadtime (T_{DEAD_X}) is an integral number of bus clock cycles, configured by the PMF deadtime registers.

The GDU propagation delays (t_{delon}, t_{deloff}) are specified in the electrical parameter Table E-1.

The FET turn on times (t_{HGON}) are load dependent but are specified for particular loads in the electrical parameter Table E-1.

The current sense amplifier delay is highly dependent on external components.

The ADC delay until a result is available is specified as the conversion period N_{CONV} in Table C-1.

1.13.3.3 Static Timing Operation

The timing frame is static if it is the same in every control cycle (defined by reload frequency) and is relative to start of the control cycle. The only settings modified from one control cycle to the next one are the PWM duty cycle registers.

The main control cycle synchronization event is the PMF **reload** event. The PMF **reload** event can be generated every *n* PWM periods.
This mode can optionally be extended by a timer channel trigger to PMF to change the PWM channel operation (e.g. used for BLDCM commutation). In this case, the PMF configuration can propagate the

Table 2-11. MODRR1 Routing Register Field Descriptions

Field	Description
7-5 M0C0RR2-0	**Module Routing Register** — MSCAN0-CANPHY0 routing Selection of MSCAN0-CANPHY0 interface routing options to support probing and conformance testing. Refer to Figure 2-4 for an illustration and Table 2-12 for preferred settings. MSCAN0 must be enabled for TXCAN0 routing to take effect on pin. CANPHY0 must be enabled for CPRXD0 and CP0DR[CPDR1] routings to take effect on pins.
4-3 PWMPRR1-0	**Module Routing Register** — PMF probe Internal PMF outputs can be probed on related external pins. Probing can be enabled independent of the PWM54RR, PWM32RR, and PWM10RR settings. 11 PMF channels 1, 3, 5 connected to related PWM1_x pins (only available for ZVMC256) 10 PMF channels 0, 2, 4 connected to related PWM1_x pins (only available for ZVMC256) 01 All PMF channels connected to related PWM1_x pins 00 No PMF channels connected to related PWM1_x pins
2 PWM54RR	**Module Routing Register** — PWM1_4 and PWM1_5 routing The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low. 1 PWM1_4 to PT1; PWM1_5 to PT2 (PP0 for S12ZVMC256) 0 PWM1_4 to GDU; PWM1_5 to GDU
1 PWM32RR	**Module Routing Register** — PWM1_2 and PWM1_3 routing The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low. 1 PWM1_2 to PP2 (PT3 for S12ZVMC256); PWM1_3 to PT0 0 PWM1_2 to GDU; PWM1_3 to GDU
0 PWM10RR	**Module Routing Register** — PWM1_0 and PWM1_1 routing The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low. 1 PWM1_0 to PP0 (PT2 for S12ZVMC256); PWM1_1 to PP1 0 PWM1_0 to GDU; PWM1_1 to GDU

Table 2-40. Effect of Enabled Features

Enabled Feature[1]	Related Signal(s)	Effect on I/O state	Effect on enabled pull device
ADCx	ANx_y	None[2 6]	None[3]
	VRH, VRL		
AMPx	AMPx, AMPPx, AMPMx	None[2 6]	None[3]
IRQ	$\overline{\text{IRQ}}$	Forced input	None[3]
XIRQ	$\overline{\text{XIRQ}}$	Forced input	None[3]
LINPHY0/ HVPHY0	LPTXD0	Forced input	None[3]
	LPRXD0	Forced output	Forced off

1. If applicable the appropriate routing configuration must be set for the signals to take effect on the pins.
2. DDR maintains control
3. PER/PPS maintain control
4. DDR maintains control
5. PER/PPS maintain control
6. To use the digital input function the related bit in Digital Input Enable Register (DIENADx) must be set to logic level “1”.

2.4.3 Pin I/O Control

Figure 2-35 illustrates the data paths to and from an I/O pin. Input and output data can always be read via the input register (PTIx, Section 2.3.3.2, “Port Input Register”) independent if the pin is used as general-purpose I/O or with a shared peripheral function. If the pin is configured as input (DDRx=0, Section 2.3.3.3, “Data Direction Register”), the pin state can also be read through the data register (PTx, Section 2.3.3.1, “Port Data Register”).

The general-purpose data direction configuration can be overruled by an enabled peripheral function shared on the same pin (Table 2-40). If more than one peripheral function is available and enabled at the same time, the highest ranked module according the predefined priority scheme in Table 2-7 will take precedence on the pin.

6.3.2.5 Debug Trace Buffer Register (DBGTB)

Address: 0x0104, 0x0105

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Other Resets	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Figure 6-7. Debug Trace Buffer Register (DBGTB)

Read: Only when unlocked AND not armed and the TSOURCE bit is set, otherwise an error code (0xEE) is returned. Only aligned word read operations are supported. Misaligned word reads or byte reads return the error code 0xEE for each byte.

Write: Aligned word writes when the DBG is disarmed and the PTACT is clear unlock the trace buffer for reading but do not affect trace buffer contents.

Table 6-14. DBGTB Field Descriptions

Field	Description
15–0 Bit[15:0]	**Trace Buffer Data Bits** — The Trace Buffer Register is a window through which the lines of the trace buffer may be read 16 bits at a time. Each valid read of DBGTB increments an internal trace buffer pointer which points to the next address to be read. When the ARM bit is written to 1 the trace buffer is locked to prevent reading. The trace buffer can only be unlocked for reading by writing to DBGTB with an aligned word write when the module is disarmed. The DBGTB register can be read only as an aligned word. Byte reads or misaligned access of these registers returns 0xEE and does not increment the trace buffer pointer. Similarly word reads while the debugger is armed or trace buffer is locked return 0xEEEE. The POR state is undefined Other resets do not affect the trace buffer contents.

6.3.2.6 Debug Count Register (DBGCNT)

Address: 0x0106

	7	6	5	4	3	2	1	0
R	0	CNT						
W								
Reset	0	—	—	—	—	—	—	—
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-8. Debug Count Register (DBGCNT)

Read: Anytime.

Write: Never.

9.5.2.6 ADC Conversion Flow Control Register (ADCFLWCTL)

Bit set and bit clear instructions should not be used to access this register.

When the ADC is enabled the bits of ADCFLWCTL register can be modified after a latency time of three Bus Clock cycles.
All bits are cleared if bit ADC_EN is clear or via ADC soft-reset.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-9. ADC Conversion Flow Control Register (ADCFLWCTL)

Read: Anytime

Write:

- Bits SEQA, TRIG, RSTA, LDOK can only be set if bit ADC_EN is set.
- Writing 1’b0 to any of these bits does not have an effect

Timing considerations (Trigger Event - channel sample start) depending on ADC mode configuration:

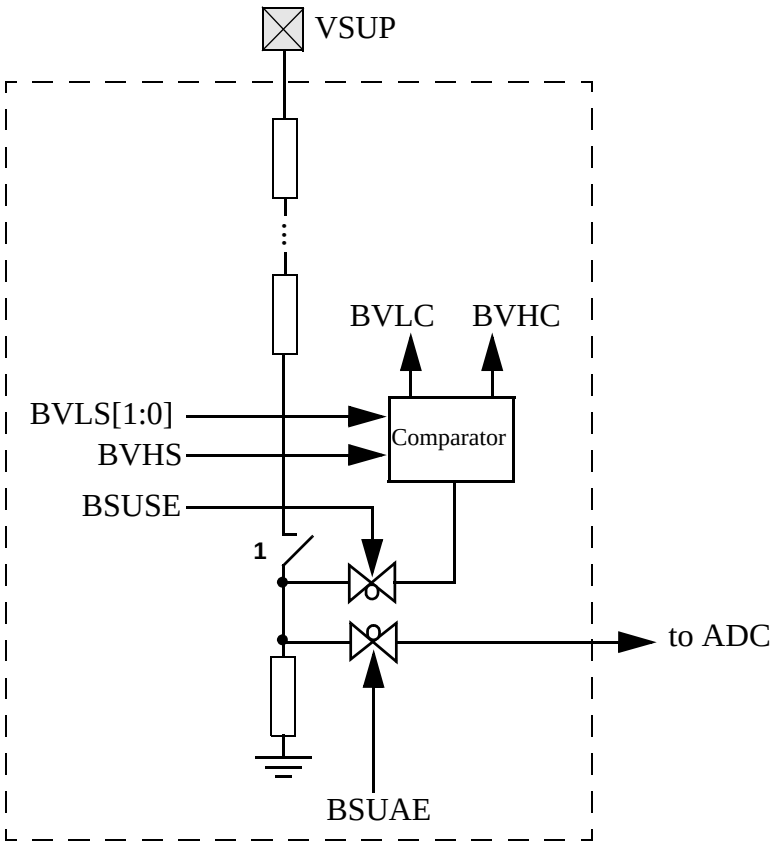
- Restart Mode
  When the Restart Event has been processed (initial command of current CSL is loaded) it takes two Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from the Trigger Event (bit TRIG set) until the select channel starts to sample.
  During a conversion sequence (back to back conversions) it takes five Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from current conversion period end until the newly selected channel is sampled in the following conversion period.
- Trigger Mode
  When a Restart Event occurs a Trigger Event is issued simultaneously. The time required to process the Restart Event is mainly defined by the internal read data bus availability and therefore can vary. In this mode the Trigger Event is processed immediately after the Restart Event is finished and both conversion flow control bits are cleared simultaneously. From de-assert of bit TRIG until sampling begins five Bus Clock cycles are required. Hence from occurrence of a Restart Event until channel sampling it takes five Bus Clock cycles plus an uncertainty of a few Bus Clock cycles.

For more details regarding the sample phase please refer to Section 9.6.2.2, “Sample and Hold Machine with Sample Buffer Amplifier.

10.1.3 Block Diagram

Figure 10-1 shows a block diagram of the BATS module. See device guide for connectivity to ADC channel.

Figure 10-1. BATS Block Diagram



1 automatically closed if BSUSE and/or BSUAE is active, open during Stop mode

10.2 External Signal Description

This section lists the name and description of all external ports.

10.2.1 VSUP — Voltage Supply Pin

This pin is the chip supply. It can be internally connected for voltage measurement. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC or to a comparator.

11.2 External Signal Description

The TIM16B4CV3 module has a selected number of external pins. Refer to device specification for exact number.

11.2.1 IOC3 - IOC0 — Input Capture and Output Compare Channel 3-0

Those pins serve as input capture or output compare for TIM16B4CV3 channel .

NOTE

For the description of interrupts see Section 11.6, “Interrupts”.

11.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

11.3.1 Module Memory Map

The memory map for the TIM16B4CV3 module is given below in Figure 11-3. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B4CV3 module and the address offset for each register.

11.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Only bits related to implemented channels are valid.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	RESERVED	RESERVED	RESERVED	RESERVED	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	RESERVED	RESERVED	RESERVED	RESERVED	FOC3	FOC2	FOC1	FOC0
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
	W								
0x0007 TTOV	R	RESERVED	RESERVED	RESERVED	RESERVED	TOV3	TOV2	TOV1	TOV0
	W								
0x0008 TCTL1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								

Figure 11-3. TIM16B4CV3 Register Summary (Sheet 1 of 2)

11.3.2.13 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 11-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 11-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	Output Compare Pin Disconnect Bits 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

11.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 11-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

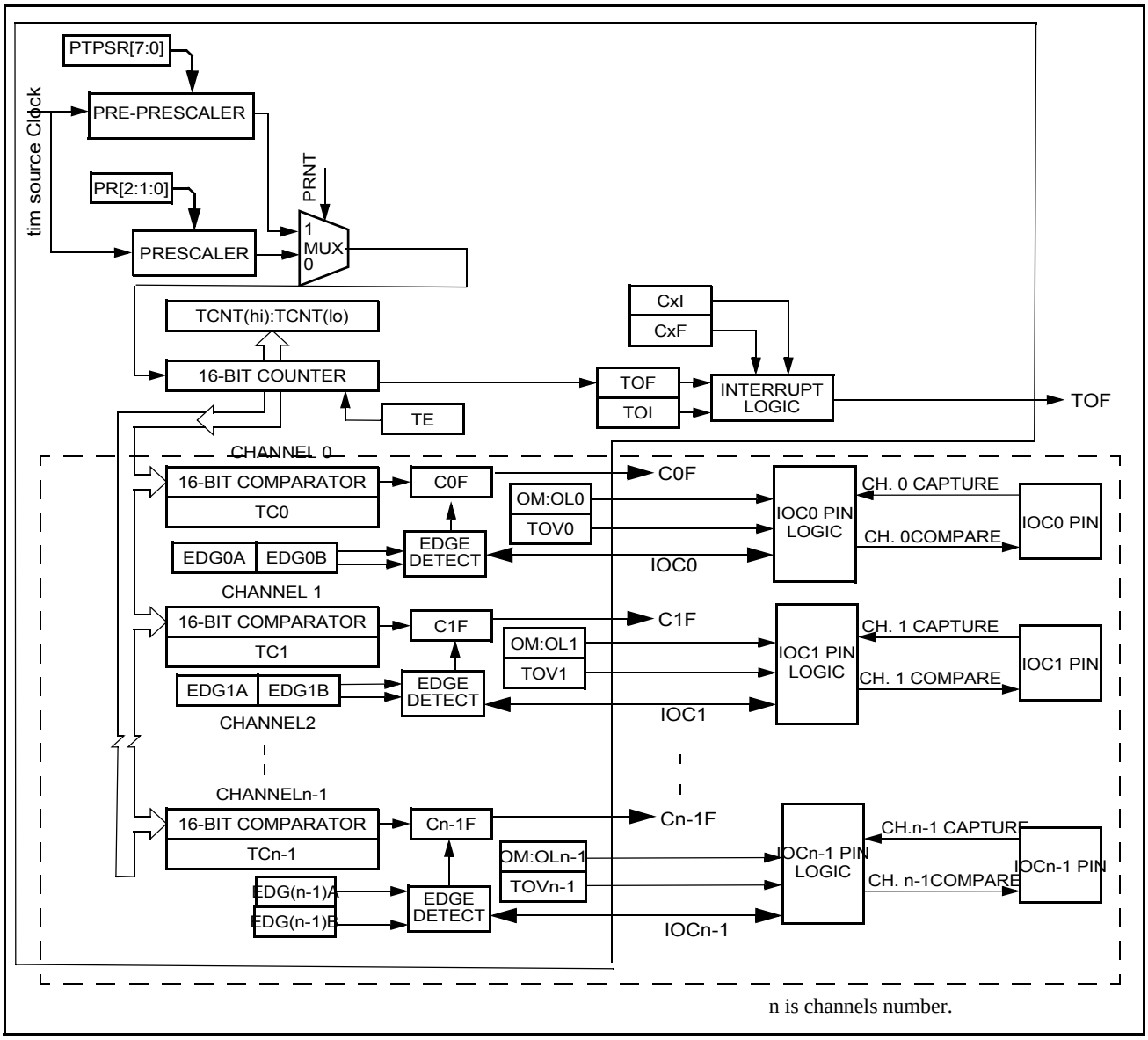


Figure 11-22. Detailed Timer Block Diagram

11.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

Table 13-25. Message Buffer Organization

Offset Address	Register	Access
0x00X0	IDR0 — Identifier Register 0	R/W
0x00X1	IDR1 — Identifier Register 1	R/W
0x00X2	IDR2 — Identifier Register 2	R/W
0x00X3	IDR3 — Identifier Register 3	R/W
0x00X4	DSR0 — Data Segment Register 0	R/W
0x00X5	DSR1 — Data Segment Register 1	R/W
0x00X6	DSR2 — Data Segment Register 2	R/W
0x00X7	DSR3 — Data Segment Register 3	R/W
0x00X8	DSR4 — Data Segment Register 4	R/W
0x00X9	DSR5 — Data Segment Register 5	R/W
0x00XA	DSR6 — Data Segment Register 6	R/W
0x00XB	DSR7 — Data Segment Register 7	R/W
0x00XC	DLR — Data Length Register	R/W
0x00XD	TBPR — Transmit Buffer Priority Register(1)	R/W
0x00XE	TSRH — Time Stamp Register (High Byte)	R
0x00XF	TSRL — Time Stamp Register (Low Byte)	R

1. Not applicable for receive buffers

Figure 13-24 shows the common 13-byte data structure of receive and transmit buffers for extended identifiers. The mapping of standard identifiers into the IDR registers is shown in Figure 13-25.

All bits of the receive and transmit buffers are ‘x’ out of reset because of RAM-based implementation[1]. All reserved or unused bits of the receive and transmit buffers always read ‘x’.

1. Exception: The transmit buffer priority registers are 0 out of reset.

Table 13-35. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the CAN bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node in receive mode samples the CAN bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

The synchronization jump width (see the Bosch CAN 2.0A/B specification for details) can be programmed in a range of 1 to 4 time quanta by setting the SJW parameter.

The SYNC_SEG, TSEG1, TSEG2, and SJW parameters are set by programming the MSCAN bus timing registers (CANBTR0, CANBTR1) (see Section 13.3.2.3, “MSCAN Bus Timing Register 0 (CANBTR0)” and Section 13.3.2.4, “MSCAN Bus Timing Register 1 (CANBTR1)”).

Table 13-36 gives an overview of the Bosch CAN 2.0A/B specification compliant segment settings and the related parameter values.

NOTE

It is the user’s responsibility to ensure the bit time settings are in compliance with the CAN standard.

Table 13-36. Bosch CAN 2.0A/B Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronization Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

13.4.4 Modes of Operation

13.4.4.1 Normal System Operating Modes

The MSCAN module behaves as described within this specification in all normal system operating modes. Write restrictions exist for some registers.

15.4.12 PWM Generator Loading

15.4.12.1 Load Enable

The load okay bit, LDOK, enables loading the PWM generator with:

- A prescaler divisor—from the PRSC bits in PMFFQC register
- A PWM period—from the PWM counter modulus registers
- A PWM pulse width—from the PWM value registers

LDOK prevents reloading of these PWM parameters before software is finished calculating them. Setting LDOK allows the prescaler bits, PMFMOD and PMFVAL registers to be loaded into a set of buffers. The loaded buffers are used by the PWM generator at the beginning of the next PWM reload cycle. Set LDOK by reading it when it is a logic zero and then writing a logic one to it. After the PWM reload event, LDOK is automatically cleared.

If LDOK is set in the same cycle as the PWM reload event occurs, then the current buffers will be used and the LDOK is valid at the next PWM reload event. See Figure 15-71.

If an asserted LDOK bit is attempted to be set again one cycle prior to the PWM reload event, then the buffers will loaded and LDOK will be cleared automatically. Else if the write access to the set LDOK bit occurs in the same cycle with the reload event, the buffers will also be loaded but the LDOK remains valid also for the next PWM reload event. See Figure 15-72.

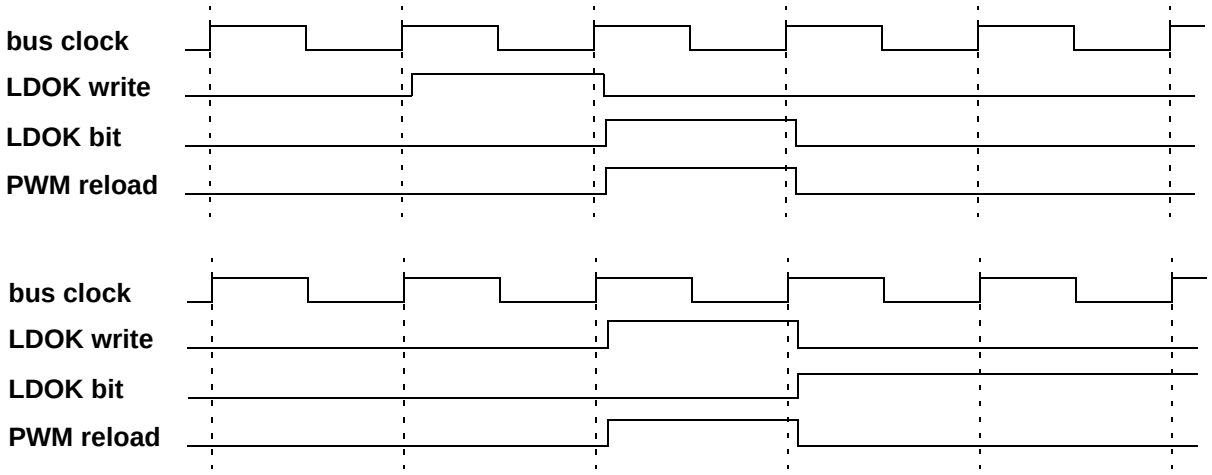


Figure 15-71. Setting cleared LDOK bit at PWM reload event

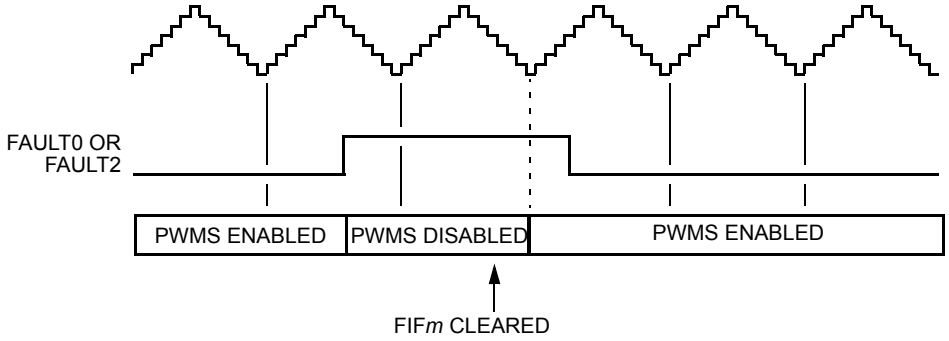


Figure 15-85. Manual Fault Recovery (Faults 0 and 2) — QSMP = 01, 10, or 11

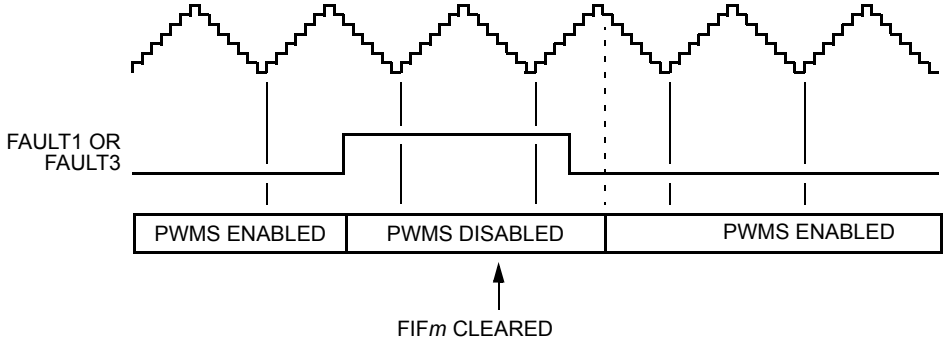


Figure 15-86. Manual Fault Recovery (Faults 1 and 3-5)

NOTE

PWM half-cycle boundaries occur at both the PWM cycle start and when the counter equals the modulus, so in edge-aligned operation full-cycles and half-cycles are equal.

NOTE

Fault protection also applies during software output control when the OUTCTL*n* bits are set. Fault recovery still occurs at half PWM cycle boundaries while the PWM generator is engaged, PWMEN equals one. But the OUT*n* bits can control the PWM outputs while the PWM generator is off, PWMEN equals zero. Thus, fault recovery occurs at IPbus cycles while the PWM generator is off and at the start of PWM cycles when the generator is engaged.

15.5 Resets

All PMF registers are reset to their default values upon any system reset.

15.6 Clocks

The gated system core clock is the clock source for all PWM generators. The system clock is used as a clock source for any other logic in this module. The system bus clock is used as clock for specific control registers and flags (LDOK*x*, PWMRF*x*, PMFOUTB).

When transmitting in 9-bit data format and using 8-bit write instructions, write first to SCI data register high (SCIDRH), then SCIDRL.

18.3.2.3 GDU Interrupt Enable Register (GDUIE)

Module Base + 0x0002 — Access: User read write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	GOCIE[1:0]		GDSEIE	GHHDIE	GLVLSIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-5. GDU Interrupt Enable Register (GDUIE)

1. Read: Anytime
   Write: Anytime

Table 18-5. GDUIE Register Field Descriptions

Field	Description
4-3 GOCIE[1:0]	GDU Overcurrent Interrupt Enable — Enables overcurrent interrupt. 0 No interrupt will be requested if any of the flags GOCIF[1:0] in the GDUF register is set 1 Interrupt will be requested if any of the flags GOCIF[1:0] in the GDUF register is set
2 GDSEIE	GDU Desaturation Error Interrupt Enable — Enables desaturation error interrupt on low-side or high-side drivers 0 No interrupt will be requested if any of the flags in the GDUDSE register is set 1 Interrupt will be requested if any of the flags in the GDUDSE register is set
1 GHHDIE	GDU High HD Interrupt Enable — Enables the high HD interrupt. 0 No interrupt will be requested whenever GHHDIF flag is set 1 Interrupt will be requested whenever GHHDIF flag is set
0 GLVLSIE	GDU Low VLS Interrupt Enable — Enables the interrupt which indicates low VLS supply 0 No interrupt will be requested whenever GLVLSIF flag is set 1 Interrupt will be requested whenever GLVLSIF flag is set

18.3.2.4 GDU Desaturation Error Flag Register (GDUDSE)

Module Base + 0x0003 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	GDHSIF[2:0]			0	GDLSIF[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-6. GDU Desaturation Error Flag Register (GDUDSE)

1. Read: Anytime
   Write: Anytime, write 1 to clear

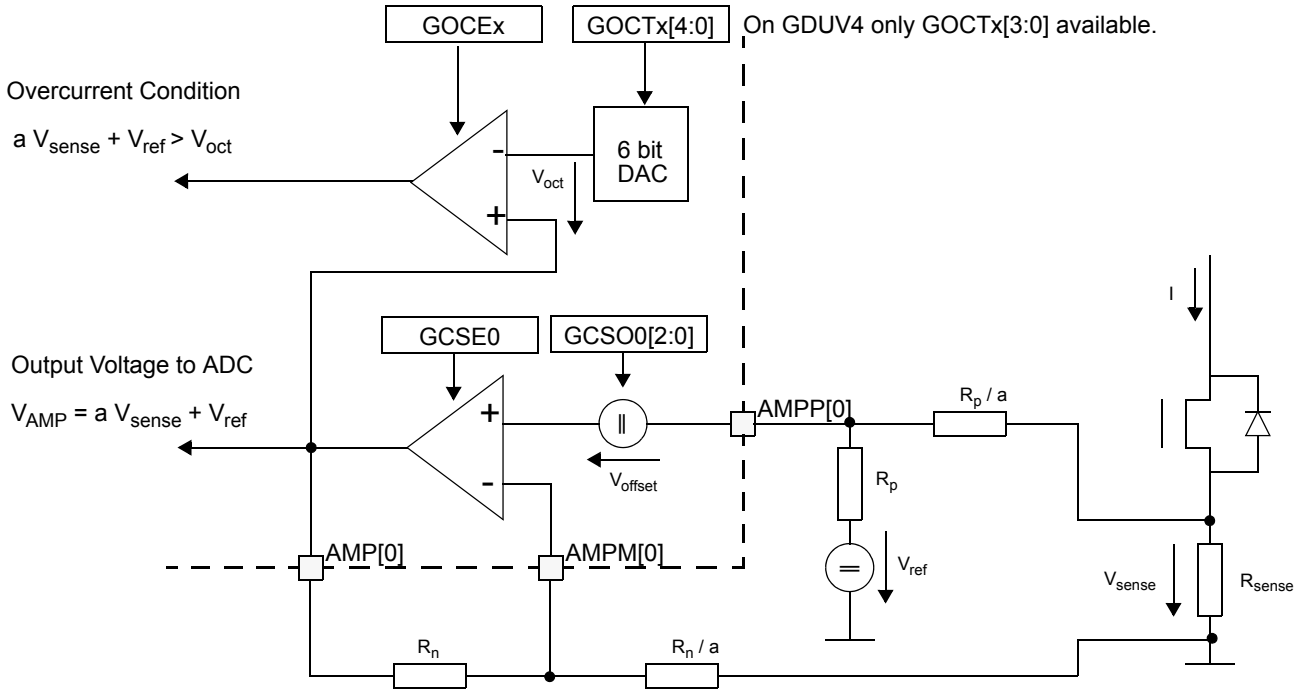
18.4.8 Current Sense Amplifier and Overcurrent Comparator

The current sense amplifier is usually connected as a differential amplifier (see Figure 18-27). It senses the current flowing through the external power FET as a voltage across the current sense resistor R_{sense}. In order to measure both positive and negative currents, an external reference has to be used. The output of the current sense amplifier can be connected to an ADC channel. For more details on ADC channel assignment, refer to Device Overview Internal Signal Mapping Section. The input offset voltage of the current sense amplifier can be adjusted with the GCSO[2:0] bits in the GDUCSO register. (see Figure 18-13) The output of the current sense amplifier is connected to the plus input of the overcurrent comparator. The minus input is driven by the output voltage of a 6 Bit DA converter. The digital input of the DA converter is {11,GOCTx[3:0]}. In order to use the overcurrent comparator GOCEx and GCSxE have to be set.

NOTE

If both overcurrent comparators are used both action bits GOCA0 and GOCA1 must have the same value. For example GOCA0=0 and GOCA1=1 is not allowed. Only GOCA0=GOCA1=1 or GOCA0=GOCA1=0 is allowed.

Figure 18-27. Current Sense Amplifier Connected as Differential Amplifier



18.4.9 GDU DC Link Voltage Monitor

In addition to the feature described in Section 18.3.2.10, “GDU Phase Mux Register (GDUPHMUX) the voltage on pin HD divide by 5 is routed to an ADC channel. See device specific information for ADC channel number. This feature is only available if GFDE is set.

19.2 External Signal Description

This section lists and describes the signals that connect off chip as well as internal supply nodes and special signals.

19.2.1 LIN — LIN Bus Pin

This pad is connected to the single-wire LIN data bus.

19.2.2 LGND — LIN Ground Pin

This pin is the device LIN ground connection. It is used to sink currents related to the LIN Bus pin. A de-coupling capacitor external to the device (typically 220 pF, X7R ceramic) between LIN and LGND can further improve the quality of this ground and filter noise.

19.2.3 VLINSUP — Positive Power Supply

External power supply to the chip. The VLINSUP supply mapping is described in device level documentation.

19.2.4 LPTxD — LIN Transmit Pin

This pin can be routed to the SCI, LPDR1 register bit, an external pin, or other options. Please refer to the PIM chapter of the device specification for the available routing options.

In the HV Phy version, LPTxD can be used to send diagnostic feedback.

This input is only used in normal mode; in other modes the value of this pin is ignored.

19.2.5 LPRxD — LIN Receive Pin

This pin can be routed to the SCI, an external pin, or other options like a timer. Please refer to the PIM chapter of the device specification for the available routing options.

In the HV Phy version, LPRxD can be used to receive control information since it can be connected to an internal timer channel.

In standby mode this output is disabled, and sends only a short pulse in case the wake-up functionality is enabled and a valid wake-up pulse was received in the LIN Bus.

19.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the LIN/HV Physical Layer.

19.3.1 Module Memory Map

A summary of the registers associated with the LIN/HV Physical Layer module is shown in Table 19-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

21.1.2 Modes of Operation

There are five modes the CAN Physical Layer can take (refer to 21.5.2 for details):

1. Shutdown mode

   In shutdown mode the CAN Physical Layer is fully de-biased including the wake-up receiver.
2. Normal mode

   In normal mode the transceiver is fully biased and functional. The SPLIT pin drives 2.5 V if enabled.
3. Pseudo-normal mode
   Same as normal mode with CANL driver disabled.
4. Listen-only mode
   Same as normal mode with transmitter de-biased.
5. Standby mode with configurable wake-up feature

   In standby mode the transceiver is fully de-biased. The wake-up receiver is enabled out of reset.

- CPU Run Mode
  The CAN Physical Layer is able to operate normally in modes 1 to 4.
- CPU Wait Mode
  The CAN Physical Layer operation is the same as in CPU run mode.
- CPU Stop Mode
  The CAN Physical Layer enters standby mode when the device voltage regulator switches to reduced performance mode (“RPM”) after a CPU stop mode request.
  If enabled, the wake-up pulse filtering mechanism is activated immediately at CPU stop mode entry.

21.1.3 Block Diagram

Figure 21-1 shows a block diagram of the CAN Physical Layer. The module consists of a precision receiver, a low-power wake-up receiver, an output driver and diagnostics.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

Wait: The prescaler keeps on running, unless PSWAI in PWMCTL is set to 1.

Freeze: The prescaler keeps on running, unless PFRZ in PWMCTL is set to 1.

22.1.3 Block Diagram

Figure 22-1 shows the block diagram for the 8-bit up to 8-channel scalable PWM block.

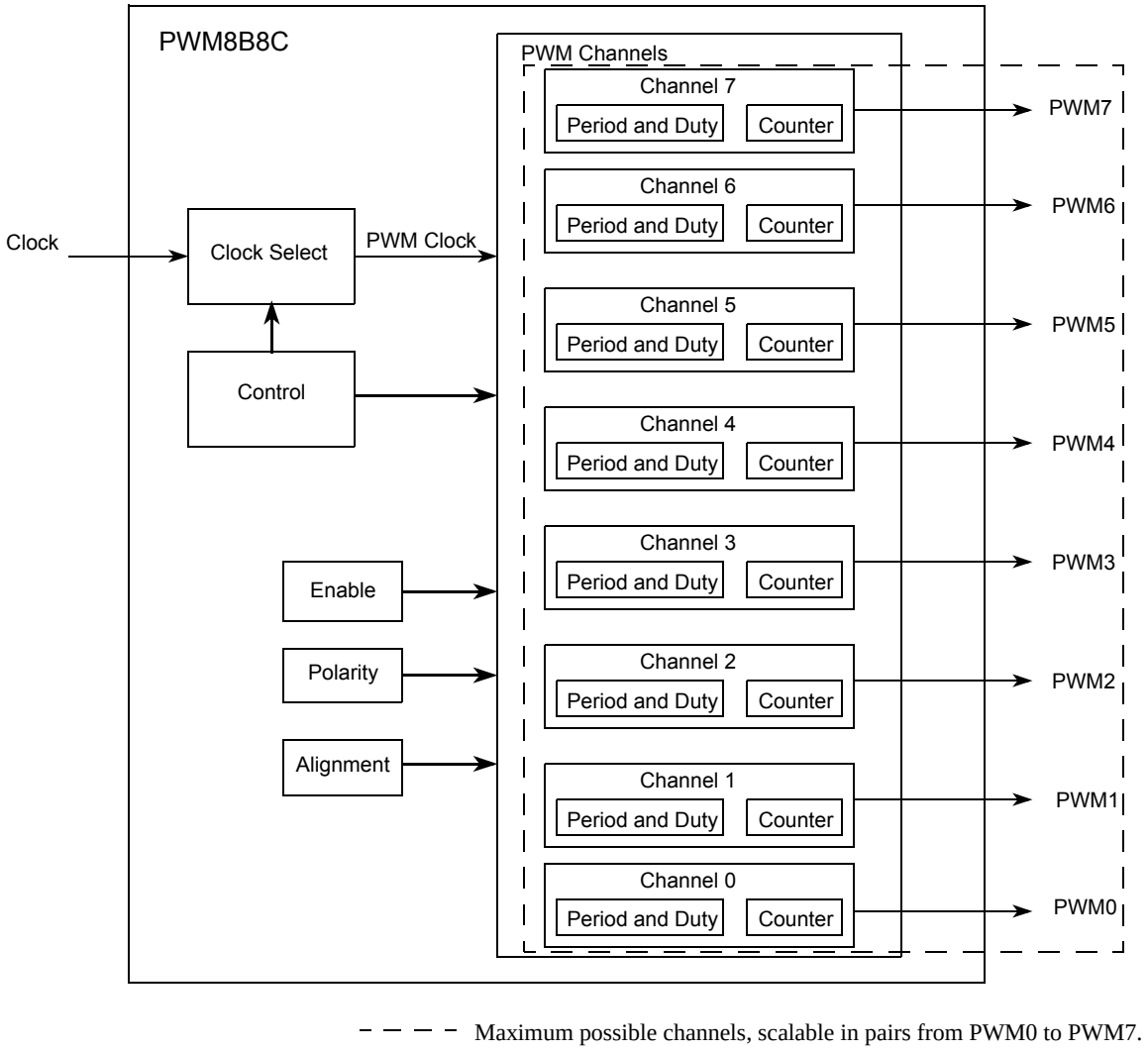


Figure 22-1. Scalable PWM Block Diagram

22.2 External Signal Description

The scalable PWM module has a selected number of external pins. Refer to device specification for exact number.