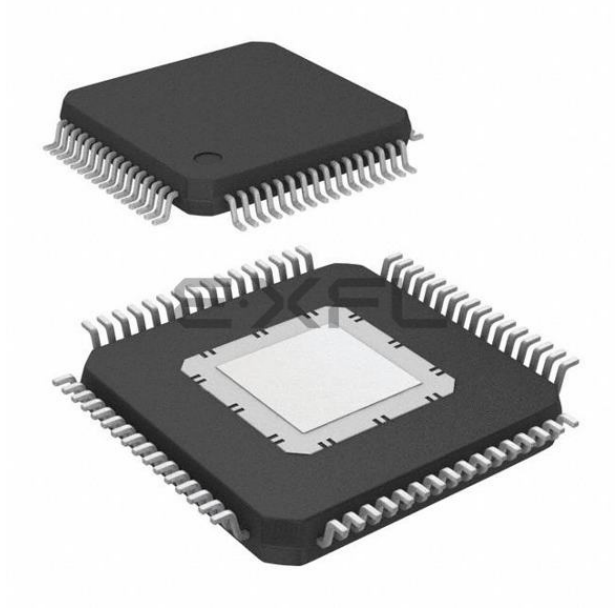

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Details	
Product Status	Obsolete
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Speed	50MHz
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Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f1mkhr

Table 1-8. Pin Summary For 64-Pin and 48-Pin Package Options (Sheet 2 of 4)

LQFP Option				Function (Priority and device dependencies specified in PIM chapter)					Power Supply	Internal Pull Resistor	
64 M/ ML	64 MC	48	Pin	1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
20	20	16	VDD	—	—	—	—	—	V_{DD}	—	—
21	21	17	PAD0	KWAD0	AN0_0	AMP0	—	—	V_{DDA}	PERADL /PPSADL	Off
22	22	18	PAD1	KWAD1	AN0_1	AMPM0	—	—	V_{DDA}	PERADL /PPSADL	Off
23	23	19	PAD2	KWAD2	AN0_2	AMPP0	—	—	V_{DDA}	PERADL /PPSADL	Off
24	24	—	PAD3	KWAD3	AN0_3	—	—	—	V_{DDA}	PERADL /PPSADL	Off
25	25	—	PAD4	KWAD4	AN0_4	—	—	—	V_{DDA}	PERADL /PPSADL	Off
26	26	—	PAD5	KWAD5	AN1_0	AMP1	—	—	V_{DDA}	PERADL /PPSADL	Off
27	27	—	PAD6	KWAD6	AN1_1	AMPM1	SS0	—	V_{DDA}	PERADL /PPSADL	Off
28	28	—	PAD7	KWAD7	AN1_2	AMPP1	—	—	V_{DDA}	PERADL /PPSADL	Off
29	29	20	PAD8	KWAD8	AN1_3	VRH0_0	VRH1_0	—	V_{DDA}	PERADH/PPSADH	Off
30	30	21	VDDA	VRH0_1	VRH1_1	—	—	—	V_{DDA}	—	—
31	31	22	VSSA	VRL0_ [1:0]	VRL1_ [1:0]	—	—	—	V_{DDA}	—	—
32	32	23	LS0	—	—	—	—	—	—	—	—
33	33	24	LG0	—	—	—	—	—	—	—	—
34	34	—	VLS0	—	—	—	—	—	—	—	—
35	35	25	VBS0	—	—	—	—	—	—	—	—

2.3.2.4 ECLK Control Register (ECLKCTL)

Address 0x0208 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	NECLK	0	0	0	0	0	0	0
W								
Reset:	1	0	0	0	0	0	0	0

Figure 2-6. ECLK Control Register (ECLKCTL)

1. Read: Anytime
   Write: Anytime

Table 2-14. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	**No ECLK** — Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. This clock has a fixed rate equivalent to the internal bus clock. 1 ECLK disabled 0 ECLK enabled

2.3.2.5 IRQ Control Register (IRQCR)

Address 0x0209 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	IRQE	IRQEN	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-7. IRQ Control Register (IRQCR)

1. Read: Anytime
   Write:
   IRQE: Once in normal mode, anytime in special mode
   IRQEN: Anytime

- Initialize the interrupt processing level configuration data registers (INT_CFADDR, INT_CFDATA0–7) for all interrupt vector requests with the desired priority levels. It might be a good idea to disable unused interrupt requests.
- Enable I-bit maskable interrupts by clearing the I-bit in the CCW.
- Enable the X-bit maskable interrupt by clearing the X-bit in the CCW (if required).

4.5.2 Interrupt Nesting

The interrupt request priority level scheme makes it possible to implement priority based interrupt request nesting for the I-bit maskable interrupt requests.

- I-bit maskable interrupt requests can be interrupted by an interrupt request with a higher priority, so that there can be up to seven nested I-bit maskable interrupt requests at a time (refer to Figure 4-14 for an example using up to three nested interrupt requests).

I-bit maskable interrupt requests cannot be interrupted by other I-bit maskable interrupt requests per default. In order to make an interrupt service routine (ISR) interruptible, the ISR must explicitly clear the I-bit in the CCW (CLI). After clearing the I-bit, I-bit maskable interrupt requests with higher priority can interrupt the current ISR.

An ISR of an interruptible I-bit maskable interrupt request could basically look like this:

- Service interrupt, e.g., clear interrupt flags, copy data, etc.
- Clear I-bit in the CCW by executing the CPU instruction CLI (thus allowing interrupt requests with higher priority)
- Process data
- Return from interrupt by executing the instruction RTI

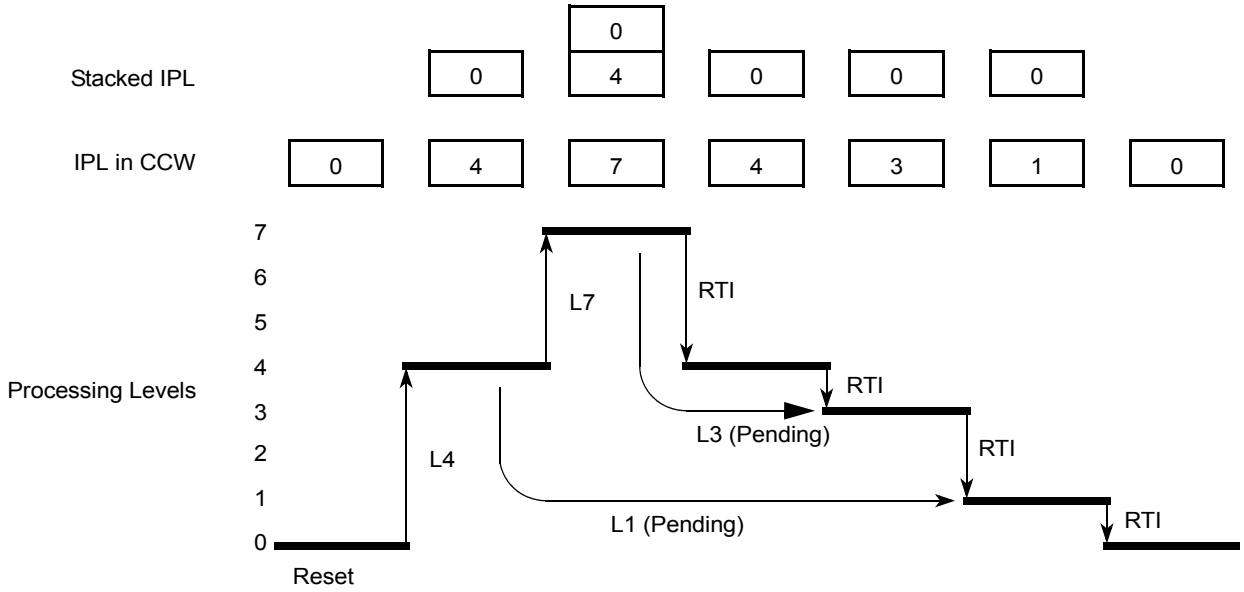


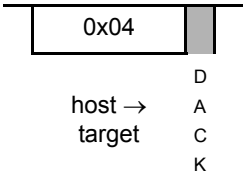
Figure 4-14. Interrupt Processing Example

Enables the hardware handshake protocol in the serial communication. The hardware handshake is implemented by an acknowledge (ACK) pulse issued by the target MCU in response to a host command. The ACK_ENABLE command is interpreted and executed in the BDC logic without the need to interface with the CPU. An ACK pulse is issued by the target device after this command is executed. This command can be used by the host to evaluate if the target supports the hardware handshake protocol. If the target supports the hardware handshake protocol, subsequent commands are enabled to execute the hardware handshake protocol, otherwise this command is ignored by the target. Table 5-8 indicates which commands support the ACK hardware handshake protocol.

For additional information about the hardware handshake protocol, refer to Section 5.4.7," and Section 5.4.8."

5.4.4.4 BACKGROUND

Enter active background mode (if enabled) **Non-intrusive**



Provided ENBDC is set, the BACKGROUND command causes the target MCU to enter active BDM as soon as the current CPU instruction finishes. If ENBDC is cleared, the BACKGROUND command is ignored.

A delay of 16 BDCSI clock cycles is required after the BACKGROUND command to allow the target MCU to finish its current CPU instruction and enter active background mode before a new BDC command can be accepted.

The host debugger must set ENBDC before attempting to send the BACKGROUND command the first time. Normally the host sets ENBDC once at the beginning of a debug session or after a target system reset. During debugging, the host uses GO commands to move from active BDM to application program execution and uses the BACKGROUND command or DBG breakpoints to return to active BDM.

A BACKGROUND command issued during stop or wait modes cannot immediately force active BDM because the WAI instruction does not end until an interrupt occurs. For the detailed mode dependency description refer to Section 5.1.3.3.

The host can recognize this pending BDM request condition because both NORESP and WAIT are set, but BDMACT is clear. Whilst in wait mode, with the pending BDM request, non-intrusive BDC commands are allowed.

Following a STOP or WAI instruction, if the BDC is enabled, the first ACK, following stop or wait mode entry is a long ACK to indicate an exception.

5.4.8 Hardware Handshake Abort Procedure

The abort procedure is based on the SYNC command. To abort a command that has not responded with an ACK pulse, the host controller generates a sync request (by driving BKGD low for at least 128 BDCSI clock cycles and then driving it high for one BDCSI clock cycle as a speedup pulse). By detecting this long low pulse in the BKGD pin, the target executes the SYNC protocol, see Section 5.4.4.1", and assumes that the pending command and therefore the related ACK pulse are being aborted. After the SYNC protocol has been completed the host is free to issue new BDC commands.

The host can issue a SYNC close to the 128 clock cycles length, providing a small overhead on the pulse length to assure the sync pulse is not misinterpreted by the target. See Section 5.4.4.1".

Figure 5-11 shows a SYNC command being issued after a READ_MEM, which aborts the READ_MEM command. Note that, after the command is aborted a new command is issued by the host.

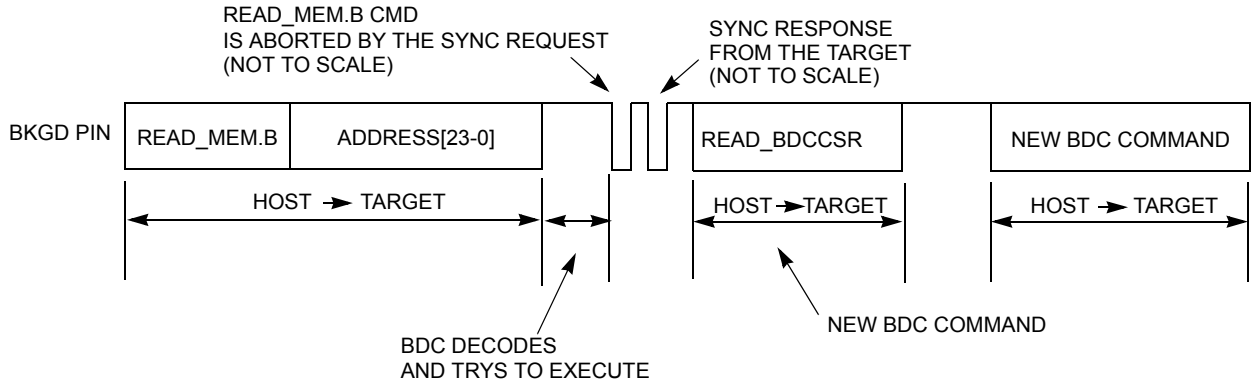


Figure 5-11. ACK Abort Procedure at the Command Level (Not To Scale)

Figure 5-12 shows a conflict between the ACK pulse and the SYNC request pulse. The target is executing a pending BDC command at the exact moment the host is being connected to the BKGD pin. In this case, an ACK pulse is issued simultaneously to the SYNC command. Thus there is an electrical conflict between the ACK speedup pulse and the SYNC pulse. As this is not a probable situation, the protocol does not prevent this conflict from happening.

7.2.2.7 ECC Debug Command (ECCDCMD)

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime, in special mode only

Figure 7-8. ECC Debug Command (ECCDCMD)

Table 7-8. ECCDCMD Field Description

Field	Description
7 ECCDRR	ECC Disable Read Repair Function— Writing one to this register bit will disable the automatic single bit ECC error repair function during read access; see also chapter 7.3.7, “ECC Debug Behavior”. 0 Automatic single ECC error repair function is enabled 1 Automatic single ECC error repair function is disabled
1 ECCDW	ECC Debug Write Command — Writing one to this register bit will perform a debug write access, to the system memory. During this access the debug data word (DDATA) and the debug ECC value (DECC) will be written to the system memory address defined by DPTR. If the debug write access is done, this bit is cleared. Writing 0 has no effect. It is not possible to set this bit if the previous debug access is ongoing (ECCDW or ECCDR bit set).
0 ECCDR	ECC Debug Read Command — Writing one to this register bit will perform a debug read access from the system memory address defined by DPTR. If the debug read access is done, this bit is cleared and the raw memory read data are available in register DDATA and the raw ECC value is available in register DECC. Writing 0 has no effect. If the ECCDW and ECCDR bit are set at the same time, then only the ECCDW bit is set and the Debug Write Command is performed. It is not possible to set this bit if the previous debug access is ongoing (ECCDW or ECCDR bit set).

7.3 Functional Description

The bus system allows 1, 2, 3 and 4 byte write access to a 4 byte aligned memory address, but the ECC value is generated based on an aligned 2 byte data word. Depending on the access type, the access is separated into different access cycles. Table 7-9 shows the different access types with the expected number of access cycles and the performed internal operations.

Table 7-9. Memory access cycles

Access type	ECC error	access cycle	Internal operation	Memory content	Error indication
2 and 4 byte aligned write access	—	1	write to memory	new data	—

8.3.2 Register Descriptions

This section describes all the S12CPMU_UHV_V10_V6 registers and their individual bits.

Address order is as listed in Figure 8-5

8.3.2.1 Reserved Register CPMUVREGTRIM0

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	U			
W								
Reset	0	0	0	0	F	F	F	F
Power on Reset	0	0	0	0	0	0	0	0

Note: After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 8-6. Reserved Register (CPMUVREGTRIM0)

Read: Anytime

Write: Only in Special Mode

8.3.2.2 Reserved Register CPMUVREGTRIM1

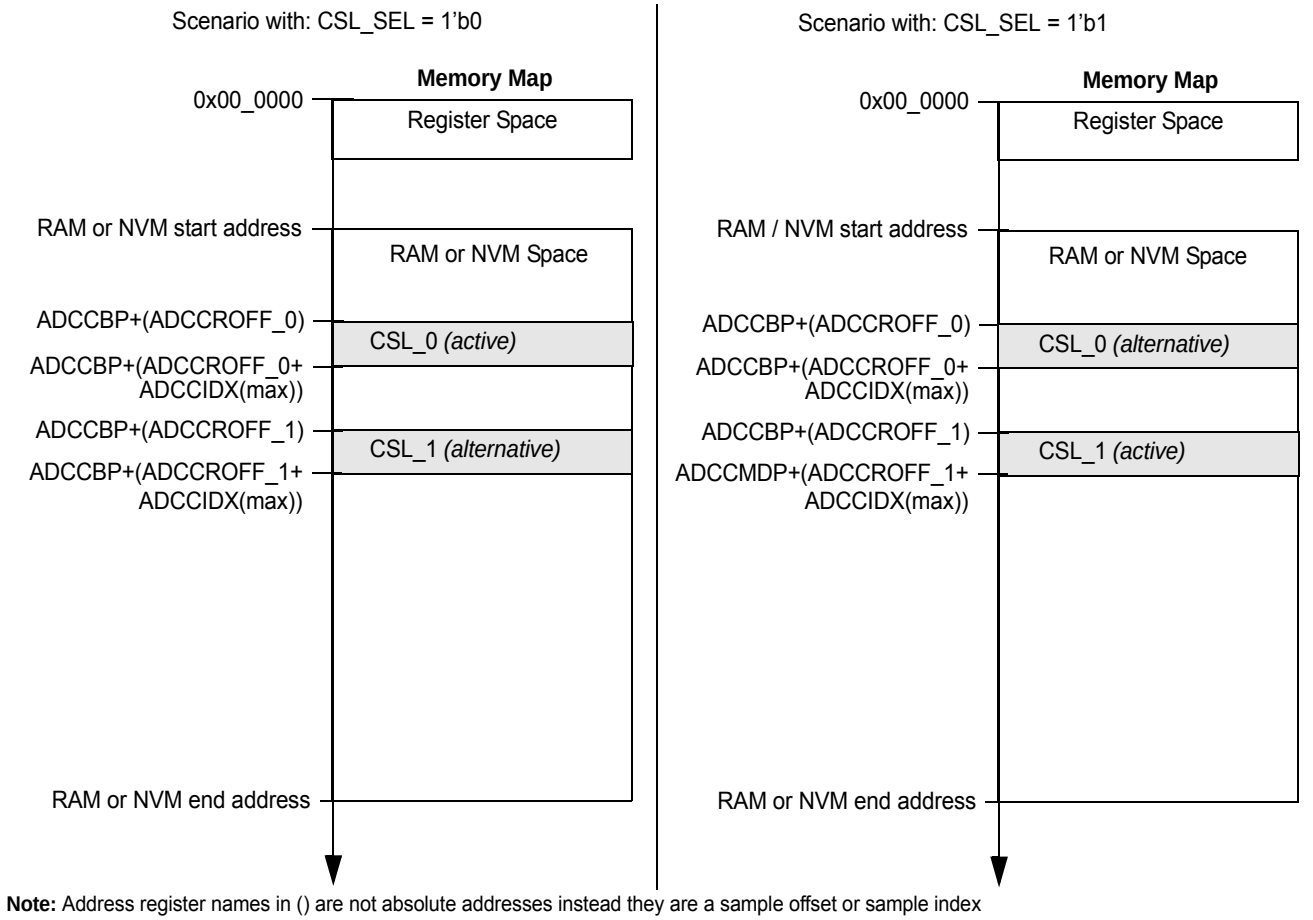
NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

.

9.6.3.2.2 Introduction of the two Command Sequence Lists (CSLs)

The two Command Sequence Lists (CSLs) can be referred to via the Command Base Pointer Register plus the Command and Result Offset Registers plus the Command Index Register (ADCCBP, ADCCROFF_0/1, ADCCIDX).
The final address for conversion command loading is calculated by the sum of these registers (e.g.: ADCCBP+ADCCROFF_0+ADCCIDX or ADCCBP+ADCCROFF_1+ADCCIDX).
Bit CSL_BMOD selects if the CSL is used in double buffer or single buffer mode. In double buffer mode, the CSL can be swapped by flow control bits LDOK and RSTA. For detailed information about when and how the CSL is swapped, please refer to Section 9.6.3.2.5, “The four ADC conversion flow control bits - description of Restart Event + CSL Swap, Section 9.9.7.1, “Initial Start of a Command Sequence List and Section 9.9.7.3, “Restart CSL execution with new/other CSL (alternative CSL becomes active CSL) — CSL swapping
Which list is actively used for ADC command loading is indicated by bit CSL_SEL. The register to define the CSL start addresses (ADCCBP) can be set to any even location of the system RAM or NVM area. It is the user’s responsibility to make sure that the different ADC lists do not overlap or exceed the system RAM or the NVM area, respectively. The error flag IA_EIF will be set for accesses to ranges outside system RAM area and cause an error interrupt if enabled.



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 9-31. Command Sequence List Schema in Double Buffer Mode

11.3.2.8 Timer Interrupt Enable Register (TIE)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 11-14. Timer Interrupt Enable Register (TIE)

Read: Anytime

Write: Anytime.

Table 11-10. TIE Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
3:0 C3I:C0I	**Input Capture/Output Compare "x" Interrupt Enable —** The bits in TIE correspond bit-for-bit with the bits in the TFLG1 status register. If cleared, the corresponding flag is disabled from causing a hardware interrupt. If set, the corresponding flag is enabled to cause a interrupt.

11.3.2.9 Timer System Control Register 2 (TSCR2)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R W	TOI	0	0	0	RESERVED	PR2	PR1	PR0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-15. Timer System Control Register 2 (TSCR2)

Read: Anytime

Write: Anytime.

Table 11-11. TSCR2 Field Descriptions

Field	Description
7 TOI	Timer Overflow Interrupt Enable 0 Interrupt inhibited. 1 Hardware interrupt requested when TOF flag set.
2:0 PR[2:0]	**Timer Prescaler Select** — These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 11-12.

Table 15-6. PMFCFG0 Field Descriptions (continued)

Field	Description
1 INDEPB	**Independent or Complementary Operation for Pair B**— This bit determines if the PWM channels 2 and 3 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are complementary PWM pair 1 PWM2 and PWM3 are independent PWMs
0 INDEPA	**Independent or Complementary Operation for Pair A**— This bit determines if the PWM channels 0 and 1 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM0 and PWM1 are complementary PWM pair 1 PWM0 and PWM1 are independent PWMs

15.3.2.2 PMF Configure 1 Register (PMFCFG1)

Address: Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	ENCE	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-4. PMF Configure 1 Register (PMFCFG1)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

A normal PWM output or positive polarity means that the PWM channel outputs high when the counter value is smaller than or equal to the pulse width value and outputs low otherwise. An inverted output or negative polarity means that the PWM channel outputs low when the counter value is smaller than or equal to the pulse width value and outputs high otherwise.

NOTE

The TOPNEGx and BOTNEGx are intended for adapting to the polarity of external predrivers on devices driving the PWM output directly to pins. If an integrated GDU is driven it must be made sure to keep the reset values of these bits in order not to violate the deadtime insertion.

Table 15-7. PMFCFG1 Field Descriptions

Field	Description
6 ENCE	**Enable Commutation Event —** This bit enables the commutation event input and activates buffering of registers PMFOUTC and PMFOUTB and MSKx bits.This bit cannot be modified after the WP bit is set.If set to zero the commutation event input is ignored and writes to the above registers and bits will take effect immediately. If set to one, the commutation event input is enabled and the value written to the above registers and bits does not take effect until the next commutation event occurs. 0 Commutation event input disabled and PMFOUTC, PMFOUTB and MSK*n* not buffered 1 Commutation event input enabled and PMFOUTC, PMFOUTB and MSK*n* buffered
5 BOTNEGC	**Pair C Bottom-Side PWM Polarity** — This bit determines the polarity for Pair C bottom-side PWM (PWM5). This bit cannot be modified after the WP bit is set. 0 Positive PWM5 polarity 1 Negative PWM5 polarity

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 16-18 summarizes the results of the data bit samples.

Table 16-18. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 16-19 summarizes the results of the stop bit samples.

Table 16-19. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

16.4.6.5.2 Fast Data Tolerance

Figure 16-29 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

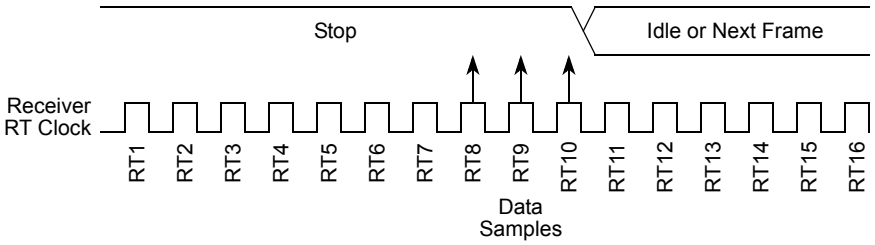


Figure 16-29. Fast Data

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles + 9 RTr cycles = 153 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 16-29, the receiver counts 153 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((160 – 153) / 160) x 100 = 4.375%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 9 RTr cycles = 169 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 16-29, the receiver counts 169 RTr cycles at the point when the count of the transmitting device is 11 bit times x 16 RTt cycles = 176 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((176 – 169) /176) x 100 = 3.98%

NOTE

Due to asynchronous sample and internal logic, there is maximal 2 bus cycles between startbit edge and 1st RT clock, and cause to additional tolerance loss at worst case. The loss should be 2/SBR/10*100%, it is small.For example, for highspeed baud=230400 with 25MHz bus, SBR should be 109, and the tolerance loss is 2/109/10*100=0.18%, and fast data tolerance is 4.375%-0.18%=4.195%.

16.4.6.6 Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCICR2) puts the receiver into standby state during which receiver interrupts are disabled.The SCI will still load the receive data into the SCIDRH/L registers, but it will not set the RDRF flag.

18.4 Functional Description

18.4.1 General

The PMF module provides the values to be driven onto the outputs of the low-side and high-side FET pre-drivers. If the FET pre-drivers are enabled, the PMF channels drive their corresponding high-side or low-side FET pre-drivers according Table 18-22.

Table 18-22. PMF Channel Assignment

PMF Channel	PMF Channel Assignment
0	High-Side Gate and Source Pins HG[0], HS[0]
1	Low-Side Gate and Source Pins LG[0], LS[0]
2	High-Side Gate and Source Pins HG[1], HS[1]
3	Low-Side Gate and Source Pins LG[1], LS[1]
4	High-Side Gate and Source Pins HG[2], HS[2]
5	Low-Side Gate and Source Pins LG[2], LS[2]

18.4.2 Low-Side FET Pre-Drivers

The three low-side FET pre-drivers turn on and off the external low-side power FETs. The energy required to charge the gate capacitance of the power FET C_G is drawn from the output of the voltage regulator VLS. See Figure 18-20. The register bits GSRCLS[2:0] in the GDUSRC Register (see Figure 18-8) control the slew rate of the low-side FET pre-drivers in order to control fast voltage changes dv/dt (see also Section 18.5.1, “FET Pre-Driver Details).

18.4.3 High-Side FET Pre-Driver

The three high-side FET pre-drivers turn on and off the external high-side power FETs. The required charge for the gate capacitance of the external power FET is delivered by the bootstrap capacitor. After the supply voltage is applied to the microcontroller or after exit from stop mode, the low-side FET pre-drivers should be activated for a short time in order to charge the bootstrap capacitor C_{BS}. Care must be taken after a long period of inactivity of the low-side FET pre-drivers to verify that the bootstrap capacitor C_{BS} is not discharged.

The register bits GSRCHS[2:0] in the GDUSRC Register (see Figure 18-8) control the slew rate of the high-side FET pre-driver in order to control fast voltage changes dv/dt (see also Section 18.5.1, “FET Pre-Driver Details).

NOTE

The minimum PWM pulse on & off time must be $t_{minpulse}$.

18.4.5 Desaturation Error

A desaturation error is generated if the output signal at HSx does not properly reflect the drive condition of the low-side and high-side FET pre-drivers. The GDU integrates three desaturation comparators for the low-side FET pre-drivers and three desaturation comparators for the high-side FET pre-drivers.

If the low-side power FET T2 (see Figure 18-23) is turned on and the drain source voltage V_{DS2} of T2 is greater than $V_{desatls}$ after the blanking time t_{BLANK} a desaturation error will be flagged. In this case the associated desaturation error flag GDLSIF[2:0] will be set (see Figure 18-6) and the low-side power FET T2 will be turned off. The level of the voltage $V_{desatls}$ can be adjusted in the range of 0.35V to 1.40V (see Figure 18-14).

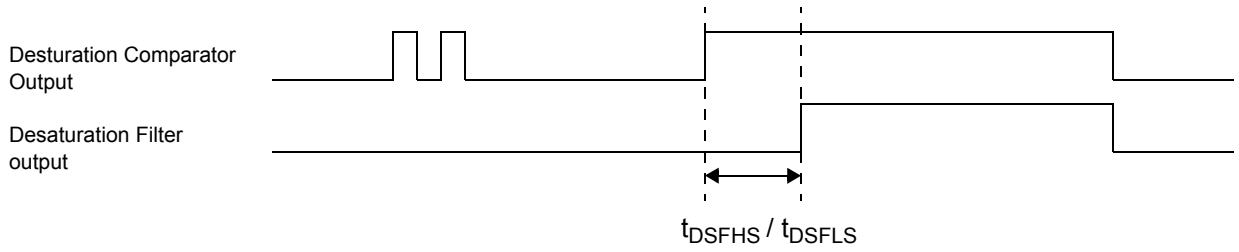
If the high-side power FET T1 (see Figure 18-23) is turned on and the drain source voltage V_{DS1} is greater than $V_{desaths}$ after the blanking time t_{BLANK} a desaturation error will be flagged.In this case the associated desaturation error flag GDHSIF[2:0] will be set (see Figure 18-6) and the high-side power FET T1 will be turned off. The level of the voltage $V_{desaths}$ can be adjusted in the range of 0.35 to 1.40V (see Figure 18-14).

NOTE

The filter on the output of desaturation comparators described below is only available on GDUV5 and V6.

The desaturation comparator outputs of the low-side and high-side drivers are filtered. The filter characteristic is controlled by the GDSFHS and GDSFLS bits as shown in Figure 18-22. A slow filter time constant can be selected by setting the corresponding GDSFHS or GDSFLS bit. If the bit is clear, then a fast time constant is selected. The time constant values, derived from simulation, are included in the device electrical specification, for both fast and slow filter time constants.

Figure 18-22. Filter Characteristic of Desaturation Comparator Output



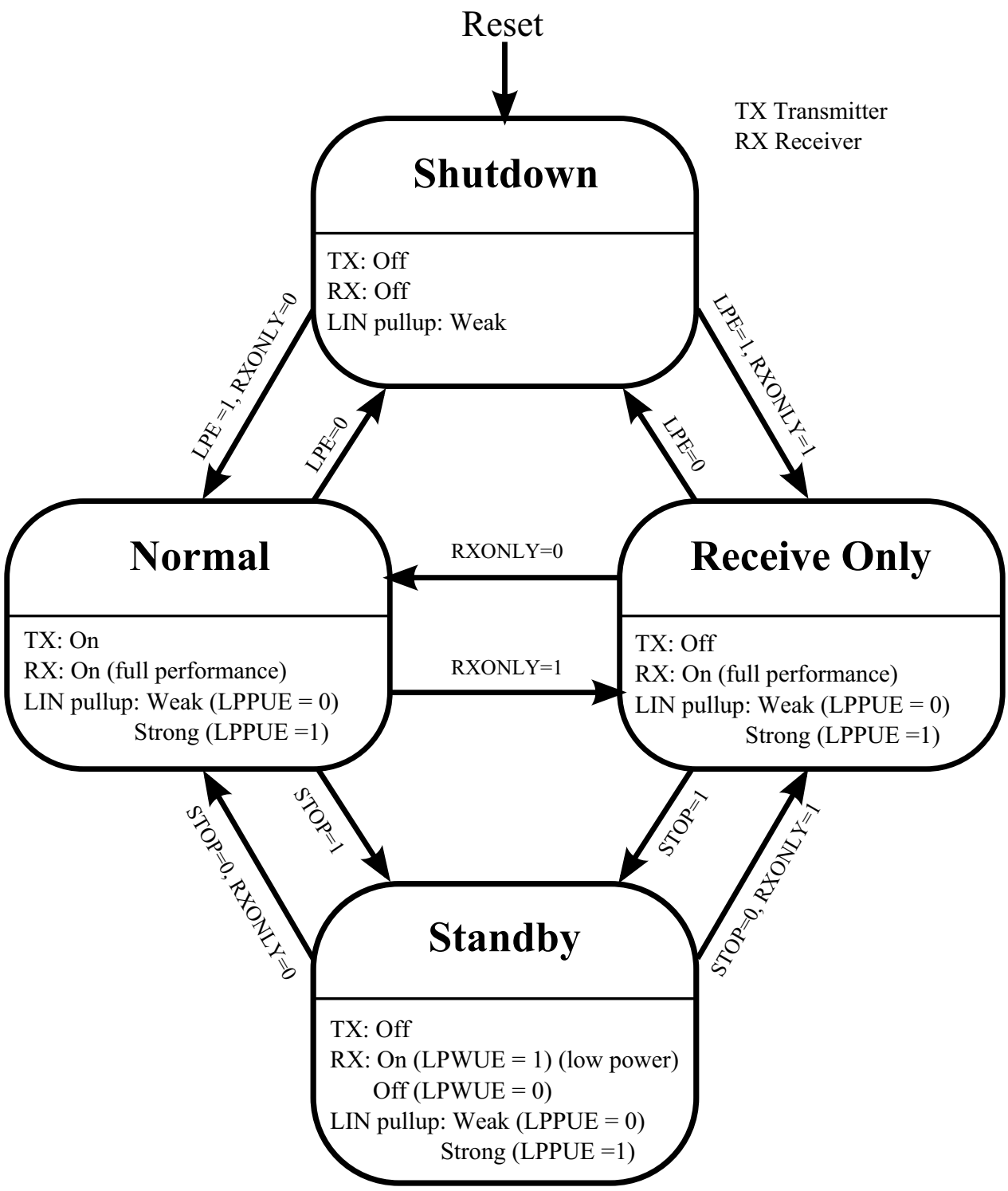


Figure 19-11. LIN/HV Physical Layer Mode Transitions

The number of DPS bits depends on the size of the implemented EEPROM. The whole implemented EEPROM range can always be protected. Each DPS value increment increases the size of the protected range by 32-bytes. Thus to protect a 1 KB range DPS[4:0] must be set (protected range of 32 x 32 bytes).

20.3.2.11 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F(1)	F1	F1	F1	F1	F1	F1	F1

= Unimplemented or Reserved

Figure 20-16. Flash Option Register (FOPT)

1. Loaded from Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but can only be written in special mode.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0xFF_FE0E located in P-Flash memory (see Table 20-4) as indicated by reset condition F in Figure 20-16. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 20-26. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device overview for proper use of the NV bits.

20.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-17. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

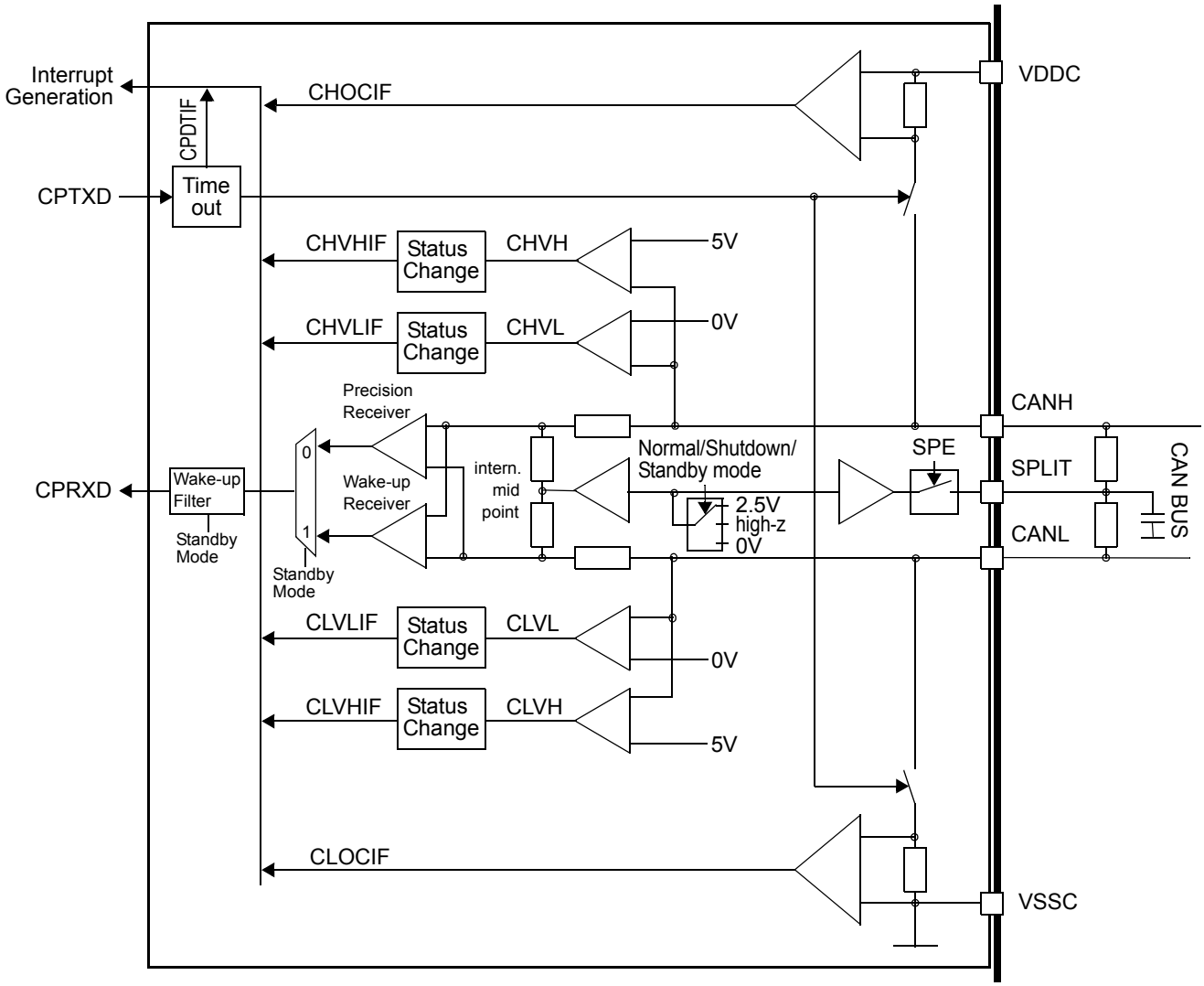


Figure 21-1. CAN Physical Layer Block Diagram

21.2 External Signal Description

Table 21-2 shows the external pins associated with the CAN Physical Layer.

Table 21-2. CAN Physical Layer Signal Properties

Name	Function
CANH	CAN Bus High Pin
SPLIT	2.5 V Termination Pin
CANL	CAN Bus Low Pin
VDDC	Supply Pin for CAN Physical Layer
VSSC	Ground Pin for CAN Physical Layer

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation P_D can be calculated from the equation below. Table A-7 below lists the power dissipation components. Figure A-2 provides an overview of power pin connectivity.

$$P_D = P_{VSUP} + P_{BCTL} + P_{INT} - P_{GPIO} + P_{LIN} - P_{EVDD1} + P_{GDU}$$

Table A-7. Power Dissipation Components

Power Component	Description
$P_{VSUP} = V_{SUP}\ I_{SUP}$	Internal Power through VSUP pin
$P_{BCTL} = V_{BCTL}\ I_{BCTL}$	Internal Power through BCTL pin
$P_{INT} = V_{DDX}\ I_{VDDX} + V_{DDA}\ I_{VDDA}$	Internal Power through VDDX/A pins.
$P_{GPIO} = V_{I/O}\ I_{I/O}$	Power dissipation of external load driven by GPIO Port. Assuming the load is connected between GPIO and ground. This power component is included in P_{INT} and is subtracted from overall MCU power dissipation P_D
$P_{LIN} = V_{LIN}\ I_{LIN}$	Power dissipation of LINPHY
P_{GDU}[1] = $(-V_{VLS\_OUT}\ I_{VLS\_OUT}) + (V_{VBS}\ I_{VBS}) + (V_{VCP}I_{VCP}) + (V_{VLSn}\ I_{VLSn})$	Power dissipation of FET-Predriver without the outputs switching

1. No switching. GDU power consumption is very load dependent.

H.3 Dynamic Electrical Characteristics

Table H-3. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 175°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL)						
1	Propagation Loop Delay TXD to RXD (Recessive to Dominant) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LRD}	 — 	 146 112 89 83 72 64	 (255)	ns
2	Propagation Delay TXD to CAN (Recessive to Dominant) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TRD}	 — 	 98 63 43 38 28 23	 — 	ns
3	Propagation Delay CAN to RXD (Recessive to Dominant, using slew rate 0)	t_{RRD}	—	42	—	ns
4	Propagation Loop Delay TXD to RXD (Dominant to Recessive) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LDR}	 — 	 366 224 153 139 114 102	 (255)	ns
5	Propagation Delay TXD to CAN (Dominant to Recessive) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TDR}	 — 	 280 152 90 81 56 46	 — 	ns
6	Propagation Delay CAN to RXD (Dominant to Recessive, using slew rate 0)	t_{RDR}	—	56	—	ns

M.18 0x0700-0x0707 SCI0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0706	SCI0DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0707	SCI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

M.19 0x0710-0x0717 SCI1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0710	SCI1BDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x0711	SCI1BDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x0712	SCI1CR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x0710	SCI1ASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		W								
0x0711	SCI1ACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		W								
0x0712	SCI1ACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
		W								
0x0713	SCI1CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x0714	SCI1SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x0715	SCI1SR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x0716	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0717	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.