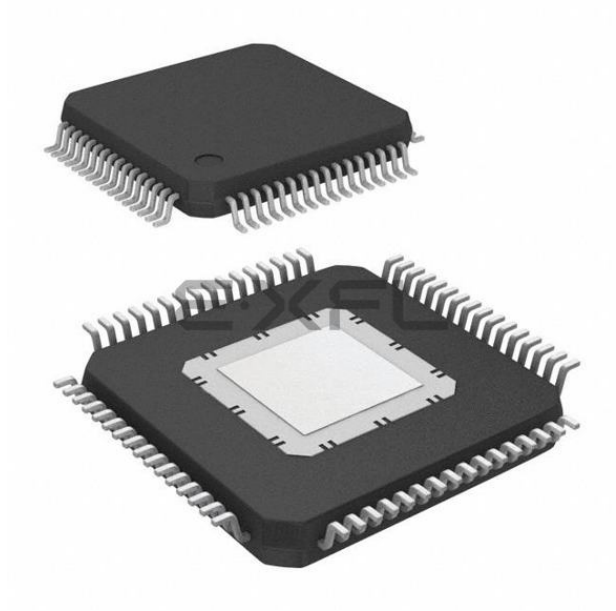

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f1wkhr

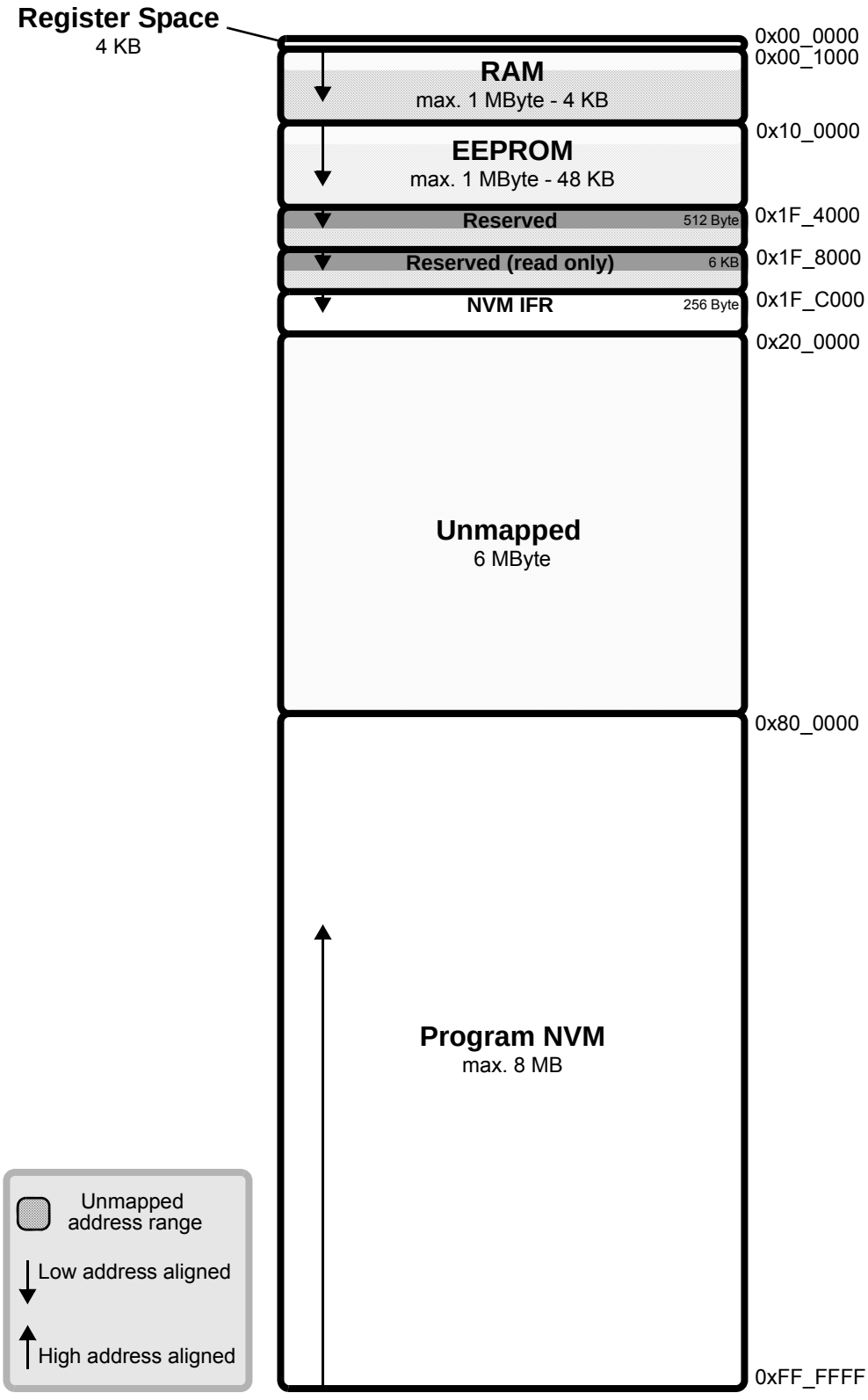
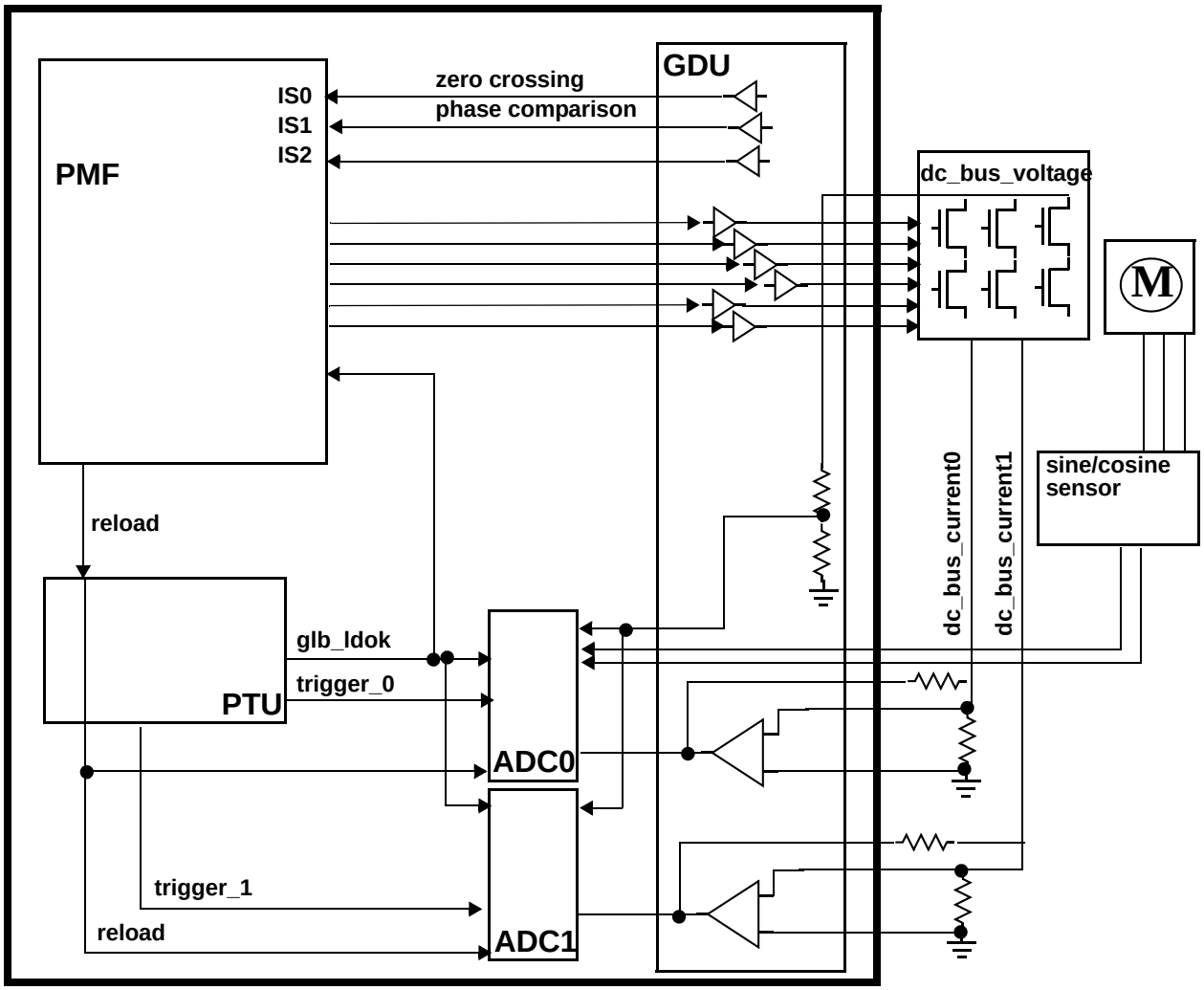


Figure 1-2. MC9S12ZVM-Family Global Memory Map. (See Table 1-3 for individual device details)

6. Map the sine/cosine input signals to ADC input channels.
7. Configure the EVDD1 pin as output.
8. Optionally use GDU phase comparators for zero crossing detection to correct dead time distortion.
9. Fetch targeted motor speed parameter from external source (e.g. SCI)
10. Configure PMF period and duty cycle.
11. Start motor by applying startup algorithm.
12. Sample the sine/cosine voltages periodically based on PWM cycle to determine motor position.
13. Use FOC algorithm to determine back EMF and motor speed.

Figure 1-17. PMSM Sine/Cosine Control Loop Configuration



The device supports the use of an external PNP to supplement the VDDX supply, for reducing on chip power dissipation. In this configuration, most of the current flowing from VRBATP to VDDX, flows through the external PNP, using the BCTL pin for PNP base current control. The configuration can be selected by register bits EXTXON and INTXON.

The maximum current that can be sourced by the voltage regulator without the external PNP is specified as IDDX, for different VSUP ranges, in the electrical parameter appendices. Depending on activity and external loading, an application current may exceed this specification limit. In such cases the external PNP configuration must be used.

A supply for the internal CANPHY is offered via device pins BCTLC and VDDC, whereby BCTLC provides the base current of an external PNP and VDDC is the CANPHY supply (output voltage of the external PNP). This configuration can be enabled by the register bit EXTCON.

Two separate 5V range supplies (VDDS1 and VDDS2) are provided for external (sensor) components. These supplies also use external PNP configurations, whereby the PNP base current is controlled by BCTLS1 and BCTLS2 for VDDS1 and VDDS2 respectively.

The VDDS1 and VDDS2 supplies feature sense inputs SNPS1 and SNPS2, to detect a short circuit or over current condition and subsequently limit the current to avoid damage.

For each ADC instantiation, the ADC register bit VRH_SEL maps the ADC reference VRH to VDDA or to a VDDS of a tracker regulator. The Figure 1-19 example only shows one ADC to VDDS connection.

1.13.8.1 Voltage Domain Monitoring

The BATS module monitors the voltage on the VSUP pin, providing status and flag bits, an interrupt and a connection to the ADC, for accurate measurement of the scaled VSUP level.

The POR circuit monitors the VDD and VDDA domains, ensuring a reset assertion until an adequate voltage level is attained. The LVR circuit monitors the VDD, VDDF and VDDX domains, generating a reset when the voltage in any of these domains drops below the specified assert level. The VDDX LVR monitor is disabled when the VREG is in reduced power mode. A low voltage interrupt circuit monitors the VDDA domain.

The GDU high side drain voltage, pin HD, is monitored within the GDU and mapped to an interrupt. A connection to the ADC is provided for accurate measurement of a scaled HD level.

1.13.8.2 FET-Predriver (GDU) Supplies

A dedicated low drop regulator is used to generate the VLS_OUT voltage from VSUP. The VLS_OUT voltage is used to supply the low side drivers and can be directly connected to the VLS inputs of each low side driver. For FET-predriver operation at lower VSUP levels, a boost circuit can be enabled by the GBOE register bit. The boost circuit requires Shottky diodes, a coil and capacitors, as shown in Figure 1-18. More detailed information is included in the GDU module description.

1.13.8.2.1 Bootstrap Precharge

The FET-predriver high side driver must provide a sufficient gate-source voltage and sufficient charge for the gate capacitance of the external FETs. A bootstrap circuit is used to provide sufficient charge, whereby

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F8–0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	RDRP	R	0	0	0	0	0	0	0	RDRP0
		W								
0x02FE–0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL[2]	R	0	0	0	0	0	0	0	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL[2]	R	0	0	0	0	0	0	0	PTPSL0
		W								
0x0334	PPSL[2]	R	0	0	0	0	0	0	0	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL[2]	R	0	0	0	0	0	0	0	PIEL0
		W								
0x0337	PIFL[2]	R	0	0	0	0	0	0	0	PIFL0
		W								

Table 5-8. BDC Command Summary (continued)

Command Mnemonic	Command Classification	ACK	Command Structure	Description
DUMP_MEM.sz	Non-Intrusive	Yes	(0x32+4 x sz)/dack/rd.sz	Dump (read) memory based on operand size (sz). Used with READ_MEM to dump large blocks of memory. An initial READ_MEM is executed to set up the starting address of the block and to retrieve the first result. Subsequent DUMP_MEM commands retrieve sequential operands.
DUMP_MEM.sz_WS	Non-Intrusive	No	(0x33+4 x sz)/d/ss/rd.sz	Dump (read) memory based on operand size (sz) and report status. Used with READ_MEM{_WS} to dump large blocks of memory. An initial READ_MEM{_WS} is executed to set up the starting address of the block and to retrieve the first result. Subsequent DUMP_MEM{_WS} commands retrieve sequential operands.
FILL_MEM.sz	Non-Intrusive	Yes	(0x12+4 x sz)/wd.sz/dack	Fill (write) memory based on operand size (sz). Used with WRITE_MEM to fill large blocks of memory. An initial WRITE_MEM is executed to set up the starting address of the block and to write the first operand. Subsequent FILL_MEM commands write sequential operands.
FILL_MEM.sz_WS	Non-Intrusive	No	(0x13+4 x sz)/wd.sz/d/ss	Fill (write) memory based on operand size (sz) and report status. Used with WRITE_MEM{_WS} to fill large blocks of memory. An initial WRITE_MEM{_WS} is executed to set up the starting address of the block and to write the first operand. Subsequent FILL_MEM{_WS} commands write sequential operands.
GO	Active Background	Yes	0x08/dack	Resume CPU user code execution
GO_UNTIL[(2)]	Active Background	Yes	0x0C/dack	Go to user program. ACK is driven upon returning to active background mode.
NOP	Non-Intrusive	Yes	0x00/dack	No operation
READ_Rn	Active Background	Yes	(0x60+CRN)/dack/rd32	Read the requested CPU register
READ_MEM.sz	Non-Intrusive	Yes	(0x30+4 x sz)/ad24/dack/rd.sz	Read the appropriately-sized (sz) memory value from the location specified by the 24-bit address
READ_MEM.sz_WS	Non-Intrusive	No	(0x31+4 x sz)/ad24/d/ss/rd.sz	Read the appropriately-sized (sz) memory value from the location specified by the 24-bit address and report status
READ_DBGTB	Non-Intrusive	Yes	(0x07)/dack/rd32/dack/rd32	Read 64-bits of DBG trace buffer

5. Listens to the BKGD pin for the sync response pulse.

Upon detecting the sync request from the host (which is a much longer low time than would ever occur during normal BDC communications), the target:

1. Discards any incomplete command
2. Waits for BKGD to return to a logic high.
3. Delays 16 cycles to allow the host to stop driving the high speed-up pulse.
4. Drives BKGD low for 128 BDCSI clock cycles.
5. Drives a 1-cycle high speed-up pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high impedance.
7. Clears the OVRRUN flag (if set).

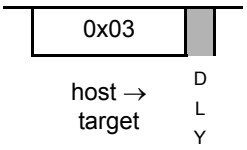
The host measures the low time of this 128-cycle SYNC response pulse and determines the correct speed for subsequent BDC communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the serial protocol can easily tolerate this speed error.

If the SYNC request is detected by the target, any partially executed command is discarded. This is referred to as a soft-reset, equivalent to a timeout in the serial communication. After the SYNC response, the target interprets the next negative edge (issued by the host) as the start of a new BDC command or the start of new SYNC request.

A SYNC command can also be used to abort a pending ACK pulse. This is explained in Section 5.4.8.

5.4.4.2 ACK_DISABLE

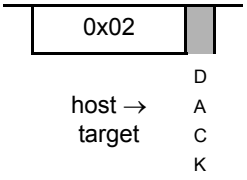
Disable host/target handshake protocol **Always Available**



Disables the serial communication handshake protocol. The subsequent commands, issued after the ACK_DISABLE command, do not execute the hardware handshake protocol. This command is not followed by an ACK pulse.

5.4.4.3 ACK_ENABLE

Enable host/target handshake protocol **Always Available**



6.2.2 Profiling Output

The DBG module features a profiling data output signal PDO. The mapping of this signal to a device pin is specified in the device specific documentation. The device pin is enabled for profiling by setting the PDOE bit. The profiling function can be enabled by the PROFILE bit in the DBGTCRL control register. This signal is output only and provides a serial, encoded data stream that can be used by external development tools to reconstruct the internal CPU code flow, as specified in Section 6.4.6. During code profiling the device PDOCLK output is used as a clock signal.

6.3 Memory Map and Registers

6.3.1 Module Memory Map

A summary of the registers associated with the DBG module is shown in Figure 6-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0100	DBGC1	R	ARM	0	reserved	BDMBP	BRKCPU	reserved	EEVE	
		W		TRIG						
0x0101	DBGC2	R	0	0	0	0	CDCM		ABCM	
		W								
0x0102	DBGTCRH	R	reserved	TSOURCE	TRANGE		TRCMOD		TALIGN	
		W								
0x0103	DBGTCRL	R	0	0	0	PREND	DSTAMP	PDOE	PROFILE	STAMP
		W								
0x0104	DBGTB	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0105	DBGTB	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0106	DBGCNT	R	0	CNT						
		W								
0x0107	DBGSCR1	R	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
		W								
0x0108	DBGSCR2	R	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
		W								
0x0109	DBGSCR3	R	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
		W								
0x010A	DBGEFR	R	PTBOVF	TRIGF	0	EEVF	ME3	ME2	ME1	ME0
		W								
0x010B	DBGSR	R	TBF	0	0	PTACT	0	SSF2	SSF1	SSF0
		W								

Figure 6-2. Quick Reference to DBG Registers

8.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV_V10_V6.

8.3.1 Module Memory Map

The S12CPMU_UHV_V10_V6 registers are shown in Figure 8-5.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	CPMU RESERVED00	R	0	0	0	0	0	0	0	0
		W								
0x0001	RESERVED	R	0	0	0	0	U	U	U	U
	CPMU VREGTRIM0	W								
0x0002	RESERVED	R	0	0	U	U	U	0	0	0
	CPMU VREGTRIM1	W								
0x0003	CPMURFLG	R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
		W								
0x0004	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0005	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0006	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0007	CPMUIFLG	R	RTIF	0	0	LOCKIF	LOCK	0	OSCIF	UPOSC
		W								
0x0008	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0009	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x000A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x000B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x000C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x000D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
			= Unimplemented or Reserved							

Figure 8-5. CPMU Register Summary

Table 8-16. COP Watchdog Rates if COPOSCSEL1=1.

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is ACLK divided by 2)
0	0	0	COP disabled
0	0	1	2^{7}
0	1	0	2^{9}
0	1	1	2^{11}
1	0	0	2^{13}
1	0	1	2^{15}
1	1	0	2^{16}
1	1	1	2^{17}

8.3.2.13 Reserved Register CPMUTEST0

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-18. Reserved Register (CPMUTEST0)

Read: Anytime

Write: Only in Special Mode

8.3.2.14 Reserved Register CPMUTEST1

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V10_V6's functionality.

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-19. Reserved Register (CPMUTEST1)

Read: Anytime

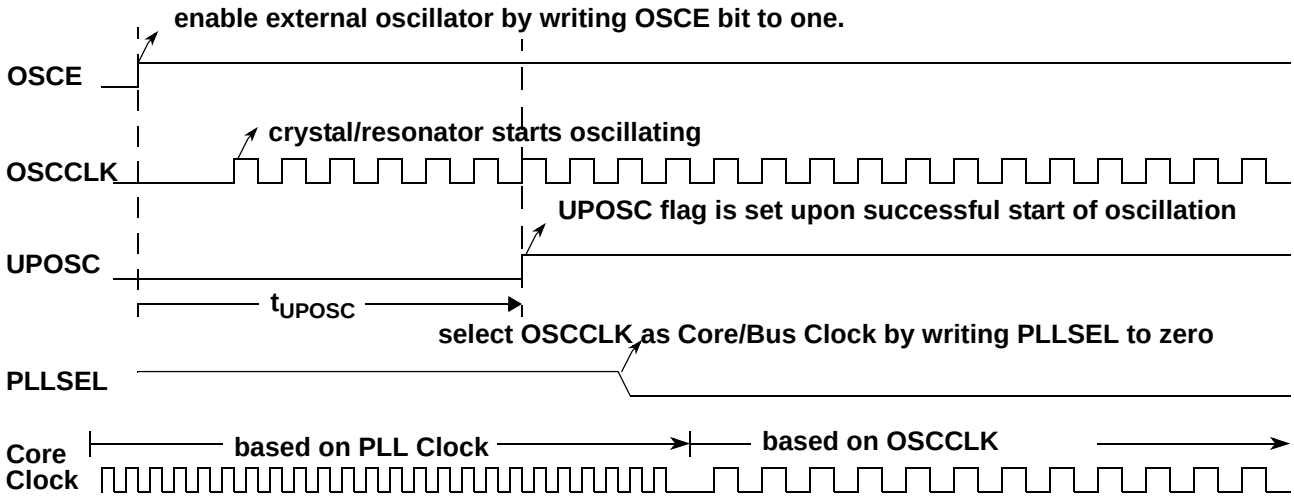
Write: Only in Special Mode

8.4.5 External Oscillator

8.4.5.1 Enabling the External Oscillator

An example of how to use the oscillator as source of the Bus Clock is shown in Figure 8-44.

Figure 8-44. Enabling the external oscillator



Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ADCEOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0011	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	Reserved	Reserved					0	0
		W								
0x0014	ADCCMD_0 (V1)	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0014	ADCCMD_0 (V2, V3)	R	CMD_SEL		OPT[1:0]		INTFLG_SEL[3:0]			
		W								
0x0015	ADCCMD_1 (V1, V2)	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0015	ADCCMD_1 (V3)	R	VRH_SEL[1:0]		CH_SEL[5:0]					
		W								
0x0016	ADCCMD_2 (V1)	R	SMP[4:0]					0	0	Reserved
		W								
0x0016	ADCCMD_2 (V2, V3)	R	SMP[4:0]					OPT[3:2]		Reserved
		W								
0x0017	ADCCMD_3	R	Reserved	Reserved	Reserved					
		W								
0x0018	Reserved	R	Reserved							
		W								
0x0019	Reserved	R	Reserved							
		W								
0x001A	Reserved	R	Reserved							
		W								
0x001B	Reserved	R	Reserved							
		W								
0x001C	ADCCIDX	R	0	0	CMD_IDX[5:0]					
		W								
0x001D	ADCCBP_0	R	CMD_PTR[23:16]							
		W								
0x001E	ADCCBP_1	R	CMD_PTR[15:8]							
		W								
0x001F	ADCCBP_2	R	CMD_PTR[7:2]						0	0
		W								
0x0020	ADCRIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0021	ADCRBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0022	ADCRBP_1	R	RES_PTR[15:8]							
		W								
0x0023	ADCRBP_2	R	RES_PTR[7:2]						0	0
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 2 of 3)

9.6.3.2.4 The two conversion flow control Mode Configurations

The ADC provides two modes (“Trigger Mode” and “Restart Mode”) which are different in the conversion control flow. The “Restart Mode” provides precise timing control about the sample start point but is more complex from the flow control perspective, while the “Trigger Mode” is more simple from flow control point of view but is less controllable regarding conversion sample start.

Following are the key differences:

In “Trigger Mode” configuration, when conversion flow control bit RSTA gets set the bit TRIG gets set automatically. Hence in “Trigger Mode” the applications should not set the bit TRIG and bit RSTA simultaneously (via data bus or internal interface), because it is a flow control failure and the ADC will cease operation.

In “Trigger Mode” configuration, after the execution of the initial Restart Event the current CSL can be executed and controlled via Trigger Events only. Hence, if the “End Of List” command is reached a restart of conversion flow from top of current CSL does not require to set bit RSTA because returning to the top of current CSL is done automatically. Therefore the current CSL can be executed again after the “End Of List” command type is executed by a Trigger Event only.

In “Restart Mode” configuration, the execution of a CSL is controlled via Trigger Events and Restart Events. After execution of the “End Of List” command the conversion flow must be continued by a Restart Event followed by a Trigger Event and the Trigger Event must not occur before the Restart Event has finished.

For more details and examples regarding flow control and application use cases please see following section and Section 9.9.7, “Conversion flow control application information.

9.6.3.2.5 The four ADC conversion flow control bits

There are four bits to control conversion flow (execution of a CSL and CSL exchange in double buffer mode). Each bit is controllable via the data bus and internal interface depending on the setting of ACC_CFG[1:0] bits (see also Figure 9-2). In the following the conversion control event to control the conversion flow is given with the related internal interface signal and corresponding register bit name together with information regarding:

- Function of the conversion control event
- How to request the event
- When is the event finished
- Mandatory requirements to executed the event

A summary of all event combinations is provided by Table 9-11.

- **Trigger Event**
  Internal Interface Signal: Trigger
  Corresponding Bit Name: TRIG

Table 11-2. TIOS Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 IOS[3:0]	Input Capture or Output Compare Channel Configuration 0 The corresponding implemented channel acts as an input capture. 1 The corresponding implemented channel acts as an output compare.

11.3.2.2 Timer Compare Force Register (CFORC)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	RESERVED	RESERVED	RESERVED	RESERVED	FOC3	FOC2	FOC1	FOC0
Reset	0	0	0	0	0	0	0	0

Figure 11-5. Timer Compare Force Register (CFORC)

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 11-3. CFORC Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 FOC[3:0]	**Note: Force Output Compare Action for Channel 3:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

11.3.2.3 Timer Count Register (TCNT)

Module Base + 0x0004

	15	14	13	12	11	10	9	9
R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
Reset	0	0	0	0	0	0	0	0

Figure 11-6. Timer Count Register High (TCNTH)

Module Base + 0x00XF

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
W								
Reset:	x	x	x	x	x	x	x	x

Figure 13-38. Time Stamp Register — Low Byte (TSRL)

1. Read: or transmit buffers: Anytime when TXEx flag is set (see Section 13.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”) and the corresponding transmit buffer is selected in CANTBSEL (see Section 13.3.2.11, “MSCAN Transmit Buffer Selection Register (CANTBSEL)”). For receive buffers: Anytime when RXF is set.
   Write: Unimplemented

Table 17-7. Example SPI Baud Rate Selection (25 MHz Bus Clock) (Sheet 3 of 3)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
1	1	0	1	0	1	448	55.80 kbit/s
1	1	0	1	1	0	896	27.90 kbit/s
1	1	0	1	1	1	1792	13.95 kbit/s
1	1	1	0	0	0	16	1.5625 Mbit/s
1	1	1	0	0	1	32	781.25 kbit/s
1	1	1	0	1	0	64	390.63 kbit/s
1	1	1	0	1	1	128	195.31 kbit/s
1	1	1	1	0	0	256	97.66 kbit/s
1	1	1	1	0	1	512	48.83 kbit/s
1	1	1	1	1	0	1024	24.41 kbit/s
1	1	1	1	1	1	2048	12.21 kbit/s

17.3.2.4 SPI Status Register (SPISR)

Module Base +0x0003

	7	6	5	4	3	2	1	0
R	SPIF	0	SPTEF	MODF	0	0	0	0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-6. SPI Status Register (SPISR)

Read: Anytime

Write: Has no effect

Table 17-8. SPISR Field Descriptions

Field	Description
7 SPIF	**SPIF Interrupt Flag** — This bit is set after received data has been transferred into the SPI data register. For information about clearing SPIF Flag, please refer to Table 17-9. 0 Transfer not yet complete. 1 New data copied to SPIDR.
5 SPTEF	**SPI Transmit Empty Interrupt Flag** — If set, this bit indicates that the transmit data register is empty. For information about clearing this bit and placing data into the transmit data register, please refer to Table 17-10. 0 SPI data register not empty. 1 SPI data register empty.
4 MODF	**Mode Fault Flag** — This bit is set if the $\overline{SS}$ input becomes low while the SPI is configured as a master and mode fault detection is enabled, MODFEN bit of SPICR2 register is set. Refer to MODFEN bit description in Section 17.3.2.2, “SPI Control Register 2 (SPICR2)”. The flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to the SPI control register 1. 0 Mode fault has not occurred. 1 Mode fault has occurred.

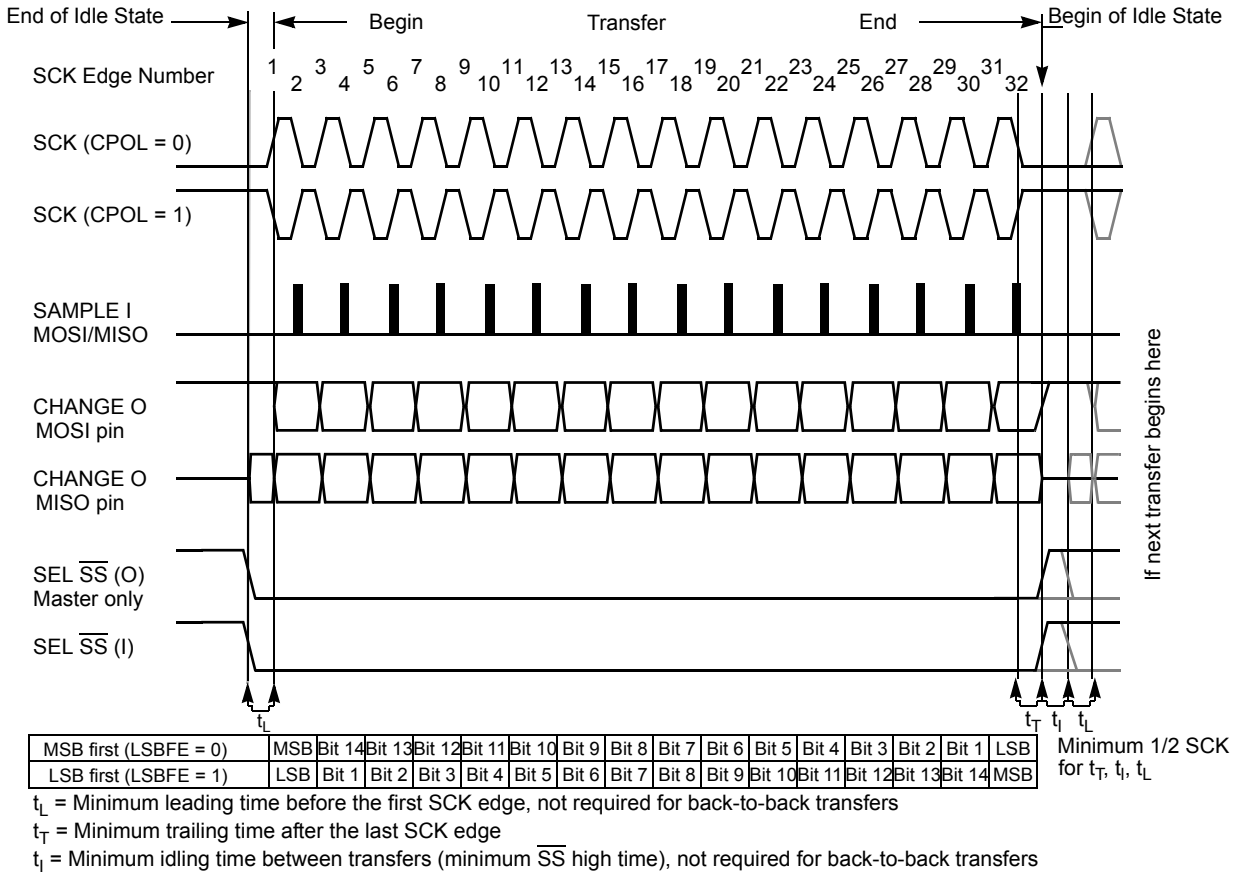


Figure 17-15. SPI Clock Format 1 (CPHA = 1), with 16-Bit Transfer Width selected (XFRW = 1)

The $\overline{SS}$ line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

- Back-to-back transfers in master mode

  In master mode, if a transmission has completed and new data is available in the SPI data register, this data is sent out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.

17.4.4 SPI Baud Rate Generation

Baud rate generation consists of a series of divider stages. Six bits in the SPI baud rate register (SPPR2, SPPR1, SPPR0, SPR2, SPR1, and SPR0) determine the divisor to the SPI module clock which results in the SPI baud rate.

The SPI clock rate is determined by the product of the value in the baud rate preselection bits (SPPR2–SPPR0) and the value in the baud rate selection bits (SPR2–SPR0). The module clock divisor equation is shown in Equation 17-3.

Figure 20-1. FTMRZ Block Diagram (Single P-Flash Block plus EEPROM block)

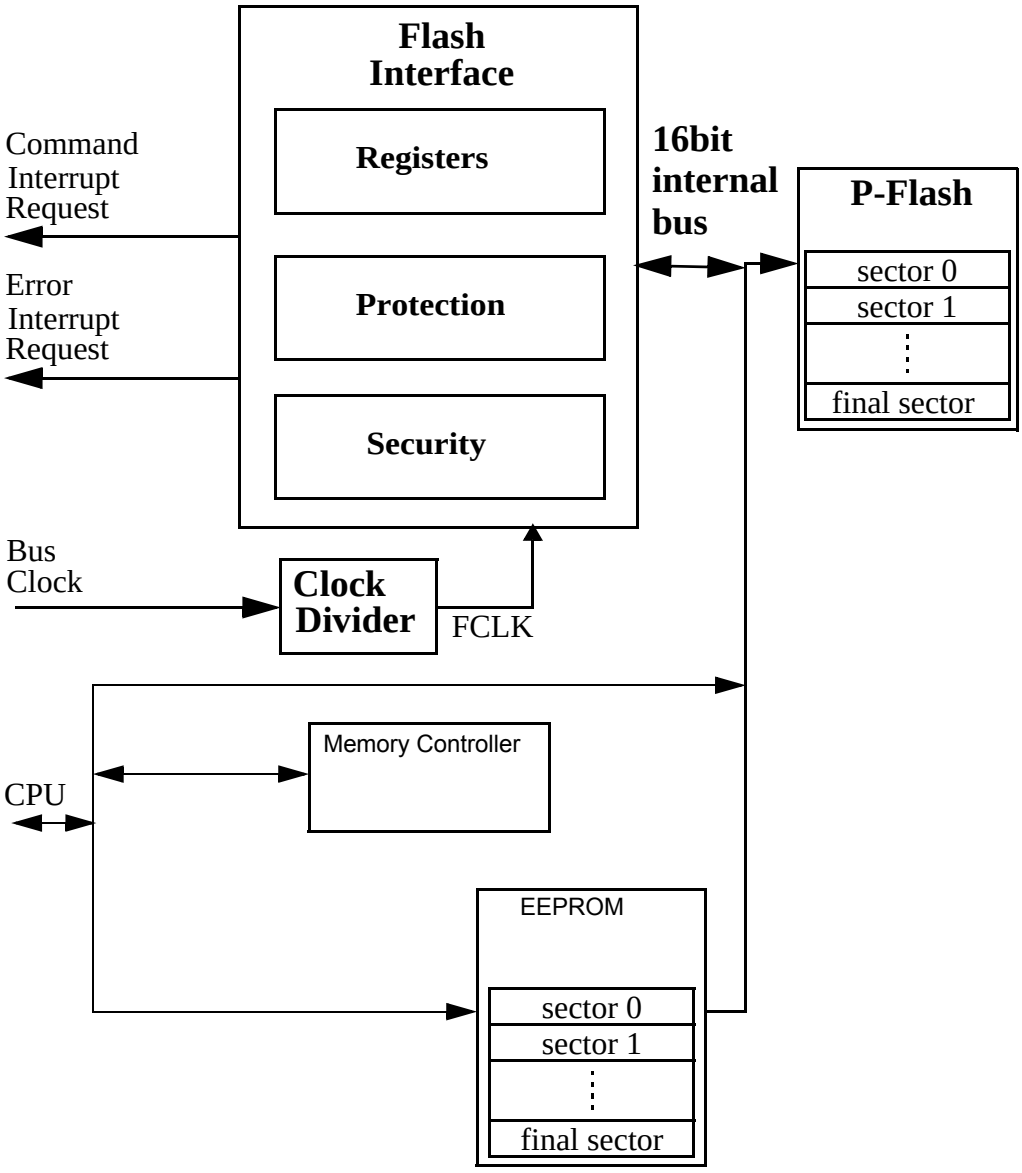


Table 22-4. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7-0 PCLK[7:0]	Pulse Width Channel 7-0 Clock Select 0 Clock A or B is the clock source for PWM channel 7-0, as shown in Table 22-5 and Table 22-6. 1 Clock SA or SB is the clock source for PWM channel 7-0, as shown in Table 22-5 and Table 22-6.

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK and PCLKABx bits in PWMCLKAB (see Section 22.3.2.7, “PWM Clock A/B Select Register (PWMCLKAB)). For Channel 0, 1, 4, 5, the selection is shown in Table 22-5; For Channel 2, 3, 6, 7, the selection is shown in Table 22-6.

Table 22-5. PWM Channel 0, 1, 4, 5 Clock Source Selection

PCLKAB[0,1,4,5]	PCLK[0,1,4,5]	Clock Source Selection
0	0	Clock A
0	1	Clock SA
1	0	Clock B
1	1	Clock SB

Table 22-6. PWM Channel 2, 3, 6, 7 Clock Source Selection

PCLKAB[2,3,6,7]	PCLK[2,3,6,7]	Clock Source Selection
0	0	Clock B
0	1	Clock SB
1	0	Clock A
1	1	Clock SA

22.3.2.4 PWM Prescale Clock Select Register (PWMPRCLK)

This register selects the prescale clock source for clocks A and B independently.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 22-6. PWM Prescale Clock Select Register (PWMPRCLK)

Read: Anytime

Write: Anytime

NOTE

PCKB2–0 and PCKA2–0 register bits can be written anytime. If the clock pre-scale is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

4. At temperatures above 25°C the current may be naturally limited by the driver, in this case the limitation circuit is not engaged and the flag is not set.

D.2 Dynamic Electrical Characteristics

Table D-2. Dynamic electrical characteristics of the LIN/HV PHY

Characteristics noted under conditions 5.5V ≤ V_{LINSUP} ≤ 18 V unless otherwise noted(1) (2) (3). Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.							
Num	**C**	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Minimum duration of wake-up pulse generating a wake-up interrupt	t_{WUFR}	56	72	120	µs
2		TxD-dominant timeout (in IRC clock periods) (4)	t_{DTLIM}	16388	—	16389	t_{IRC}
3		Propagation delay of receiver	t_{rx_pd}	—	—	6	µs
4		Symmetry of receiver propagation delay rising edge w.r.t. falling edge	t_{rx_sym}	-2	—	2	µs
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NOMINAL SLEW RATE - 20.0KBIT/S							
5		Rising/falling edge time (min to max / max to min)	t_{rise}	—	6.5	—	µs
6		Over-current masking window (IRC trimmed at 1MHz)	t_{OCLIM}	15	—	16	µs
7	M	Duty cycle 1 $T_{HRec(max)} = 0.744 \times V_{LINSUP}$ $T_{HDom(max)} = 0.581 \times V_{LINSUP}$ V_{LINSUP} = 5.5V...18V t_{Bit} = 50us $D1 = t_{Bus\_rec(min)} / (2 \times t_{Bit})$	D1	0.396 (5)	—	—	
8	M	Duty cycle 2 $T_{HRec(min)} = 0.422 \times V_{LINSUP}$ $T_{HDom(min)} = 0.284 \times V_{LINSUP}$ V_{LINSUP} = 5.5V...18V t_{Bit} = 50us $D2 = t_{Bus\_rec(max)} / (2 \times t_{Bit})$	D2	—	—	0.581[5]	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4KBIT/S							
9		Rising/falling edge time (min to max / max to min)	t_{rise}	—	13	—	µs
10		Over-current masking window (IRC trimmed at 1MHz)	t_{OCLIM}	31	—	32	µs
11	M	Duty cycle 3 $T_{HRec(max)} = 0.778 \times V_{LINSUP}$ $T_{HDom(max)} = 0.616 \times V_{LINSUP}$ V_{LINSUP} = 5.5V...18V t_{Bit} = 96us $D3 = t_{Bus\_rec(min)} / (2 \times t_{Bit})$	D3	0.417[5]	—	—	