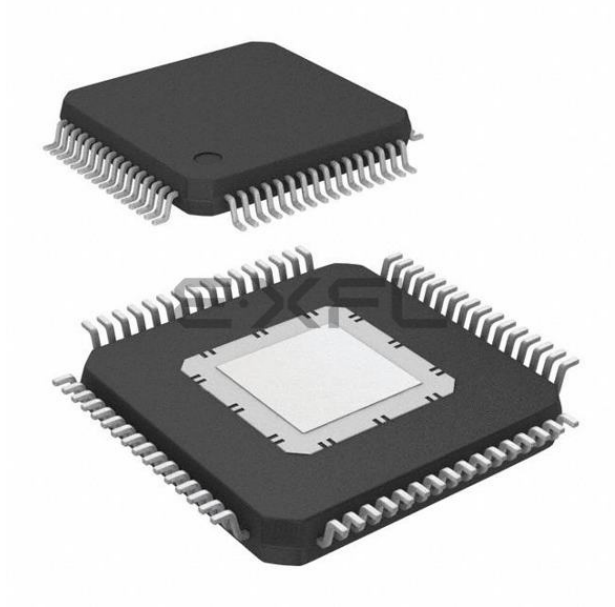


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f2mkh

Table 2-27. Port P Polarity Select Register Field Descriptions

Field	Description
2-1 PPSP	**See Section 2.3.3.5, “Polarity Select Register”**
0 PPSP	**Pull Polarity Select** — Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. This bit also selects the polarity of the active interrupt edge. This bit selects if a high or a low level on FAULT5 generates a fault event in PMF. 1 Pulldown device selected; rising edge selected; active-high level selected on FAULT5 input 0 Pullup device selected; falling edge selected; active-low level selected on FAULT5 input

2.3.4.2 Port P Interrupt Enable Register (PIEP)

Read: Anytime

Address 0x02F6 PIEP — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIE1	0	0	0	0	PIEP2	PIEP1	PIEP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-24. Port P Interrupt Enable Register

1. Read: Anytime
   Write: Anytime

Table 2-28. Port P Interrupt Enable Register Field Descriptions

Field	Description
7 OCIE1	**Over-Current Interrupt Enable register** — This bit enables or disables the over-current interrupt on PP0. 1 PP0 over-current interrupt enabled 0 PP0 over-current interrupt disabled (interrupt flag masked)
2-0 PIEP2-0	**See Section 2.3.3.6, “Port Interrupt Enable Register”**

Chapter 3
Memory Mapping Control (S12ZMMCV1)

Table 3-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	27 Jul 2012		Corrected Table 3-9
V01.04	27 Jul 2012		Added feature tags
V01.05	6 Aug 2012		Fixed wording
V01.06	12 Feb 2013	Figure 3-8 3.3.2.2/3-162	• Changed “KByte:to “KB” • Corrected the description of the MMCECH/L register

3.1 Introduction

The S12ZMMC module controls the access to all internal memories and peripherals for the S12ZCPU, and the S12ZBDC module. It also provides access to the RAM for ADCs and the PTU module. The S12ZMMC determines the address mapping of the on-chip resources, regulates access priorities and enforces memory protection. Figure 3-1 shows a block diagram of the S12ZMMC module.

Table 5-9. CPU Register Number (CRN) Mapping

CPU Register	Valid Data Bits	Command	Opcode	Command	Opcode
D7	[31:0]	WRITE_D7	0x47	READ_D7	0x67
X	[23:0]	WRITE_X	0x48	READ_X	0x68
Y	[23:0]	WRITE_Y	0x49	READ_Y	0x69
SP	[23:0]	WRITE_SP	0x4A	READ_SP	0x6A
PC	[23:0]	WRITE_PC	0x4B	READ_PC	0x6B
CCR	[15:0]	WRITE_CCR	0x4C	READ_CCR	0x6C

5.4.5.2 BDC Access Of Device Memory Mapped Resources

The device memory map is accessed using READ_MEM, DUMP_MEM, WRITE_MEM, FILL_MEM and READ_SAME, which support different access sizes, as explained in the command descriptions.

When an unimplemented command occurs during a DUMP_MEM, FILL_MEM or READ_SAME sequence, then that sequence is ended.

Illegal read accesses return a value of 0xEE for each byte. After an illegal access FILL_MEM and READ_SAME commands are not valid, and it is necessary to restart the internal access sequence with READ_MEM or WRITE_MEM. An illegal access does not break a DUMP_MEM sequence. After read accesses that cause the RDINV bit to be set, DUMP_MEM and READ_SAME commands are valid, it is not necessary to restart the access sequence with a READ_MEM.

The hardware forces low-order address bits to zero for longword accesses to ensure these accesses are realigned to 0-modulo-size alignments.

Word accesses map to 2-bytes from within a 4-byte field as shown in Table 5-10. Thus if address bits [1:0] are both logic “1” the access is realigned so that it does not straddle the 4-byte boundary but accesses data from within the addressed 4-byte field.

Table 5-10. Field Location to Byte Access Mapping

Address[1:0]	Access Size	00	01	10	11	Note
00	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	
01	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
10	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
11	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
00	16-bit	Data [15:8]	Data [7:0]			
01	16-bit		Data [15:8]	Data [7:0]		
10	16-bit			Data [15:8]	Data [7:0]	
11	16-bit			Data [15:8]	Data [7:0]	Realigned
00	8-bit	Data [7:0]				
01	8-bit		Data [7:0]			
10	8-bit			Data [7:0]		
11	8-bit				Data [7:0]	
			Denotes byte that is not transmitted			

Table 6-27. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

6.3.2.13 Debug Comparator A Address Register (DBGAAH, DBGAAM, DBGAAL)

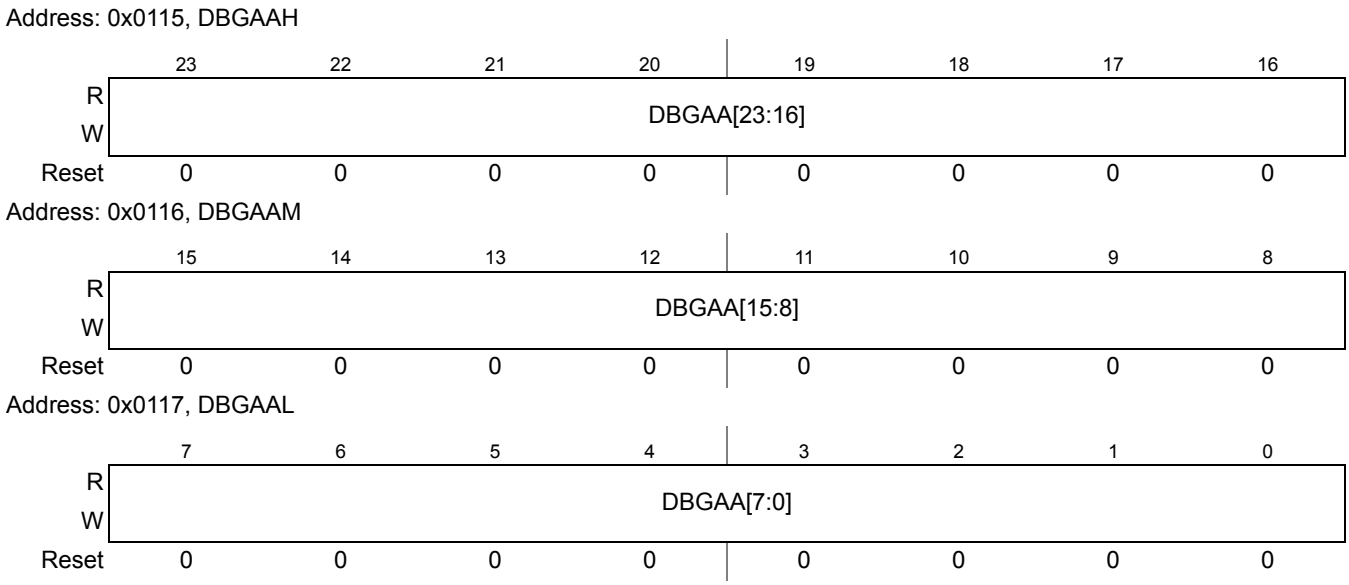


Figure 6-15. Debug Comparator A Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-28. DBGAAH, DBGAAM, DBGAAL Field Descriptions

Field	Description
23–16 DBGAA [23:16]	**Comparator Address Bits [23:16]—** These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one
15–0 DBGAA [15:0]	**Comparator Address Bits [15:0]—** These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

pointer is initialized by each aligned write to DBGTB to point to the oldest data again. This enables an interrupted trace buffer read sequence to be easily restarted from the oldest data entry. After reading all trace buffer lines, the next read wraps around and returns the contents of line0.

The least significant word of each 64-bit wide array line is read out first. All bytes, including those containing invalid information are read out.

6.4.5.5 Trace Buffer Reset State

The trace buffer contents are not initialized by a system reset. Thus should a system reset occur, the trace session information from immediately before the reset occurred can be read out. The DBGCNT bits are not cleared by a system reset. Thus should a reset occur, the number of valid lines in the trace buffer is indicated by DBGCNT. The internal pointer is cleared by a system reset. It can be initialized by an aligned word write to DBGTB following a reset during debugging, so that it points to the oldest valid data again. Debugging occurrences of system resets is best handled using mid or end trigger alignment since the reset may occur before the trace trigger, which in the begin trigger alignment case means no information would be stored in the trace buffer.

6.4.6 Code Profiling

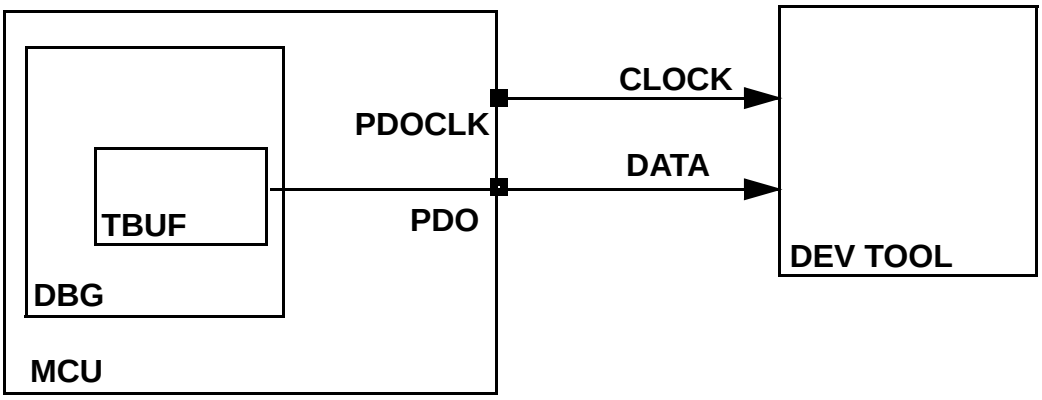
6.4.6.1 Code Profiling Overview

Code profiling supplies encoded COF information on the PDO pin and the reference clock on the PDOCLK pin. If the TSOURCE bit is set then code profiling is enabled by setting the PROFILE bit. The associated device pin is configured for code profiling by setting the PDOE bit. Once enabled, code profiling is activated by arming the DBG. During profiling, if PDOE is set, the PDO operates as an output pin at a half the internal bus frequency, driving both high and low.

Independent of PDOE status, profiling data is stored to the trace buffer and can be read out in the usual manner when the debug session ends and the PTACT bit has been cleared.

The external debugger uses both edges of the clock output to strobe the data on PDO. The first PDOCLK edge is used to sample the first data bit on PDO.

Figure 6-30. Profiling Output Interface



8.1.1 Differences between S12CPMU_UHV_V10 and S12CPMU_UHV_V6

- The following device pins exist only in V10:
  VDDS1, VDDS2, BCTLS1, BCTLS2, SNPS1, SNPS2,
- The feature of switching VDDS1/2 to VRH1/2 (which connects to ADC) exists only in V10
- The following register and bits exist only in V10:
  CPMUVREGCTL register: Bits VRH2EN, VRH1EN, EXTS1ON, EXTS2ON
  CPMULVCTL register: Bit VDDSIE
  CPMUVDDS register
- The VDDS Integrity Interrupt only exists in V10

Be aware that the output frequency varies with the TC trimming. A frequency trimming correction is therefore necessary. The values provided in Table 8-28 are typical values at ambient temperature which can vary from device to device.

8.3.2.24 S12CPMU_UHV_V10_V6 Oscillator Register (CPMUOSC)

This registers configures the external oscillator (XOSCLCP).

Module Base + 0x001A

	7	6	5	4	3	2	1	0
R	OSCE	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-35. S12CPMU_UHV_V10_V6 Oscillator Register (CPMUOSC)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

Table 8-29. CPMUOSC Field Descriptions

Field	Description
7 OSCE	**Oscillator Enable Bit** — This bit enables the external oscillator (XOSCLCP). The UPOSC status bit in the CPMIUFLG register indicates when the oscillation is stable and when OSCCLK can be selected as source of the Bus Clock or source of the COP or RTI.**If the oscillator clock monitor reset is enabled (OMRE = 1 in CPMUOSC2 register), then a loss of oscillation will lead to an oscillator clock monitor reset.** 0 External oscillator is disabled. REFCLK for PLL is IRCCLK. 1 External oscillator is enabled. Oscillator clock monitor is enabled. External oscillator is qualified by PLLCLK. REFCLK for PLL is the external oscillator clock divided by REFDIV. If OSCE bit has been set (write “1”) the EXTAL and XTAL pins are exclusively reserved for the oscillator and they can not be used anymore as general purpose I/O until the next system reset. **Note:** When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.

9.5.2.22 ADC Result Base Pointer Register (ADCRBP)

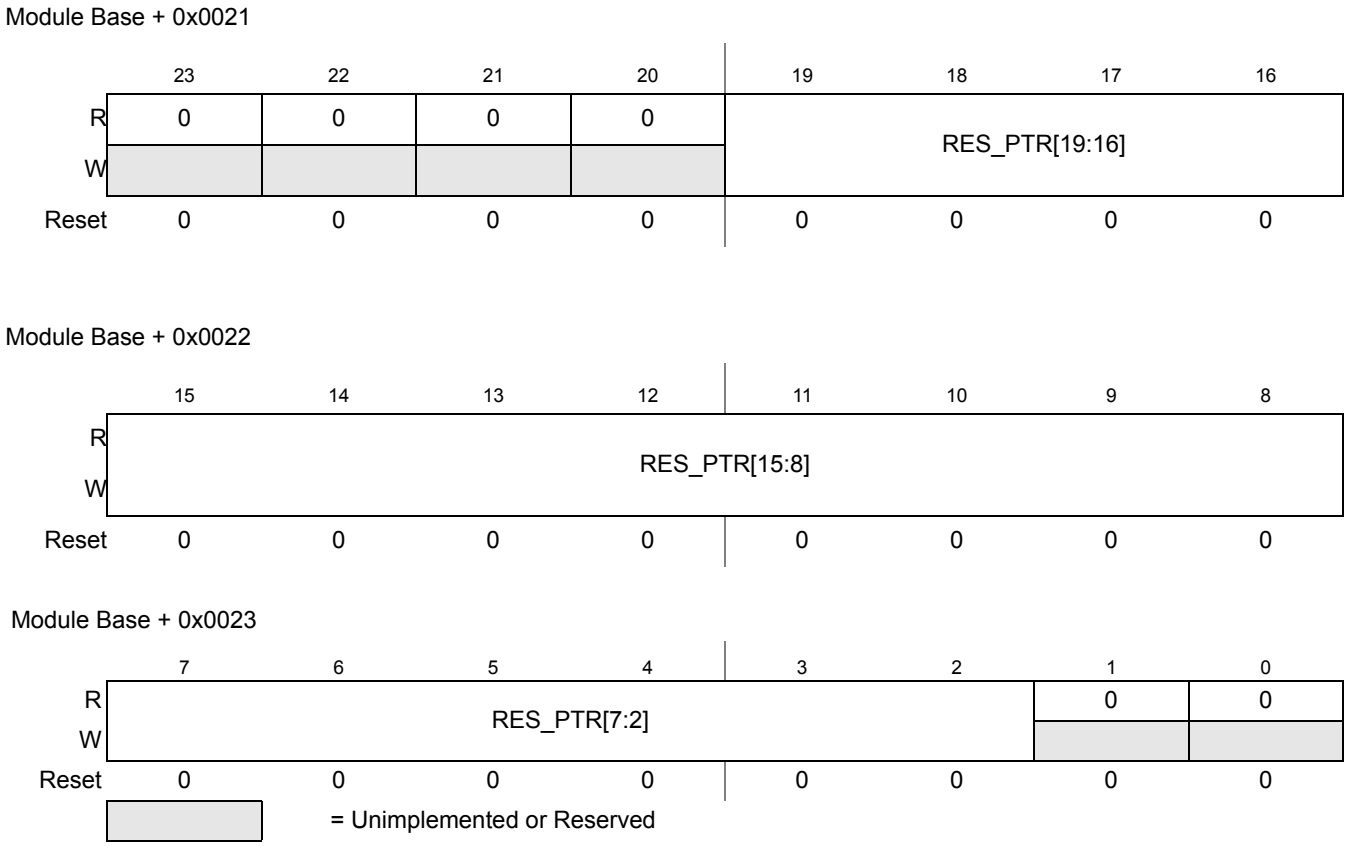


Figure 9-25. ADC Result Base Pointer Registers (ADCRBP_0, ADCRBP_1, ADCRBP_2))

Read: Anytime

Write: Bits RES_PTR[19:2] writeable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-30. ADCRBP Field Descriptions

Field	Description
19-2 RES_PTR[19:2]	**ADC Result Base Pointer Address** — These bits define the base address of the list areas inside the system RAM of the memory map to which conversion results will be stored to at the end of a conversion. These bits can only be written if bit ADC_EN is clear. See also Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs).

9.6 Functional Description

9.6.1 Overview

The ADC12B_LBA consists of an analog sub-block and a digital sub-block. It is a successive approximation analog-to-digital converter including a sample-and-hold mechanism and an internal charge scaled C-DAC (switched capacitor scaled digital-to-analog converter) with a comparator to realize the successive approximation algorithm.

9.6.2 Analog Sub-Block

The analog sub-block contains all analog circuits (sample and hold, C-DAC, analog Comparator, and so on) required to perform a single conversion. Separate power supplies VDDA and VSSA allow noise from the MCU circuitry to be isolated from the analog sub-block for improved accuracy.

9.6.2.1 Analog Input Multiplexer

The analog input multiplexers connect one of the external or internal analog input channels to the sample and hold storage node.

9.6.2.2 Sample and Hold Machine with Sample Buffer Amplifier

The Sample and Hold Machine controls the storage and charge of the storage node (sample capacitor) to the voltage level of the analog signal at the selected ADC input channel. This architecture employs the advantage of reduced crosstalk between channels.

The sample buffer amplifier is used to raise the effective input impedance of the A/D machine, so that external components (higher bandwidth or higher impedance connected as specified) are less significant to accuracy degradation.

During the sample phase, the analog input connects first via a sample buffer amplifier with the storage node always for two ADC clock cycles (“Buffer” sample time). For the remaining sample time (“Final” sample time) the storage node is directly connected to the analog input source. Please see also Figure 9-28 for illustration and the Appendix of the device reference manual for more details.
The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.
During the hold process, the analog input is disconnected from the storage node.

If signal Restart is asserted before signal LoadOK is set the conversion starts from top of currently active CSL at the next Trigger Event (no exchange of CSL list).
If signal Restart is asserted after or simultaneously with signal LoadOK the conversion starts from top of the other CSL at the next Trigger Event (CSL is switched) if CSL is configured for double buffer mode.

- **Sequence Abort Event**
  Internal Interface Signal: Seq_Abort
  Corresponding Bit Name: SEQA
  - *Function:*
    Abort any possible ongoing conversion at next conversion boundary and abort current conversion sequence and active CSL
  - *Requested by:*
    - Positive edge of internal interface signal Seq_Abort
    - Write Access via data bus to set control bit SEQA
  - *When finished:*
    This bit gets cleared when an ongoing conversion is finished and the result is stored and/or an ongoing conversion sequence is aborted and current active CSL is aborted (ADC idle, RVL done)
  - *Mandatory Requirement:*
    - In all ADC conversion flow control modes bit SEQA can only be set if:
    * ADC not idle (a conversion or conversion sequence is ongoing)
    * ADC idle but RVL done condition not reached
    The RVL done condition is not reached if:
    * An “End Of List” command type has not been executed
    * A Sequence Abort Event has not been executed (bit SEQA not already set)
    - In all ADC conversion flow control modes a Sequence Abort Event can be issued at any time
    - In ADC conversion flow control mode “Restart Mode” after a conversion sequence abort request has been executed it is mandatory to set bit RSTA. If a Trigger Event occurs before a Restart Event is executed (bit RSTA set and cleared by hardware), bit TRIG is set, error flag TRIG_EIF is set, and the ADC can only be continued by a Soft-Reset. After the Restart Event the ADC accepts new Trigger Events (bit TRIG set) and begins conversion from top of the currently active CSL.
    - In ADC conversion flow control mode “Restart Mode” after a Sequence Abort Event has been executed, a Restart Event causes only the RSTA bit being set. The ADC executes a Restart Event only.
  - In both conversion flow control modes (“Restart Mode” and “Trigger Mode”) when conversion flow control bit RSTA gets set automatically bit SEQA gets set when the ADC has not reached one of the following scenarios:
    * An “End Of List” command type has been executed or is about to be executed
    * A Sequence Abort request is about to be executed or has been executed.
    In case bit SEQA is set automatically the Restart error flag RSTA_EIF is set to indicate an unexpected Restart Request.

Table 11-16. PTPSR Field Descriptions

Field	Description
7:0 PTPS[7:0]	**Precision Timer Prescaler Select Bits** — These eight bits specify the division rate of the main Timer prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. Table 11-17 shows some selection examples in this case. The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

The Prescaler can be calculated as follows depending on logical value of the PTPS[7:0] and PRNT bit:

PRNT = 1 : Prescaler = PTPS[7:0] + 1

Table 11-17. Precision Timer Prescaler Selection Examples when PRNT = 1

PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0	Prescale Factor
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
0	0	0	1	0	0	1	1	20
0	0	0	1	0	1	0	0	21
0	0	0	1	0	1	0	1	22
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	253
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

11.4 Functional Description

This section provides a complete functional description of the timer TIM16B4CV3 block. Please refer to the detailed timer block diagram in Figure 11-22 as necessary.

Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-11. MSCAN Transmitter Interrupt Enable Register (CANTIER)

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANTIER register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-13. CANTIER Register Field Descriptions

Field	Description
2-0 TXEIE[2:0]	**Transmitter Empty Interrupt Enable** 0 No interrupt request is generated from this event. 1 A transmitter empty (transmit buffer available for transmission) event causes a transmitter empty interrupt request.

13.3.2.9 MSCAN Transmitter Message Abort Request Register (CANTARQ)

The CANTARQ register allows abort request of queued messages as described below.

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-12. MSCAN Transmitter Message Abort Request Register (CANTARQ)

1. Read: Anytime
   Write: Anytime when not in initialization mode

NOTE

The CANTARQ register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

14.3.2.11 Trigger Generator 1 Trigger Number Register (TG1TNUM)

Module Base + 0x000B — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	TG1TNUM[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-13. Trigger Generator 1 Trigger Number Register (TG1TNUM)

1. Read: Anytime
   Write: Never

Table 14-13. TG1TNUM Register Field Descriptions

Field	Description
4:0 TG1TNUM[4:0]	Trigger Generator 1 Trigger Number — This register shows the number of generated triggers since the last reload event. After the generation of 32 triggers this register shows zero. The next reload event clears this register. See also Figure 14-22.

14.3.2.12 Trigger Generator 1 Trigger Value (TG1TVH, TG1TVL)

Module Base + 0x000C — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	TG1TV[15:8]							
W								
Reset	0	0	0	0	0	0	0	0

Module Base + 0x000D — Access: User read only

	7	6	5	4	3	2	1	0
R	TG1TV[7:0]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-14. Trigger Generator 1 Trigger Value Register (TG1TVH, TG1TVL)

1. Read: Anytime
   Write: Never

Table 14-14. TG1TV Register Field Descriptions

Field	Description
TG1TV[15:0]	Trigger Generator 1 Next Trigger Value — This register contains the currently used trigger value to generate the next trigger. If the time base counter reach this value the next trigger event is generated. If the trigger generator reached the end of list (EOL) symbol then this value is visible inside this register. If the last generated trigger was trigger number 32 then the last used trigger value is visible inside this register. See also Figure 14-22.

14.3.2.15 Trigger Generator 0 List 0 Index (TG0L0IDX)

Module Base + 0x0014 Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	TG0L0IDX[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-17. Trigger Generator 0 List 0 Index (TG0L0IDX)

1. Read: Anytime
   Write: Never

Table 14-17. TG0L0IDX Register Field Descriptions

Field	Description
6:0 TG0L0IDX [6:0]	Trigger Generator 0 List 0 Index Register — This register defines offset of the start point for the trigger event list 0 used by trigger generator 0. This register is read only, so the list 0 for trigger generator 0 will start at the PTUPTR address. For more information see Section 14.4.2, “Memory based trigger event list”.

14.3.2.16 Trigger Generator 0 List 1 Index (TG0L1IDX)

Module Base + 0x0015 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	TG0L1IDX[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-18. Trigger Generator 0 List 1 Index (TG0L1IDX)

1. Read: Anytime
   Write: Anytime, if TG0EN bit is cleared

Table 14-18. TG0L1IDX Register Field Descriptions

Field	Description
6:0 TG0L1IDX [6:0]	Trigger Generator 0 List 1 Index Register — This register cannot be modified after the TG0EN bit is set. This register defines offset of the start point for the trigger event list 1 used by trigger generator 0. For more information see Section 14.4.2, “Memory based trigger event list”.

The Protection Override command can be called multiple times and every time it is launched it will preserve the current values of registers FPROT and DFPROT in a single-entry buffer to be restored later; when the Protection Override command is launched to restore FPROT and DFPROT these registers will assume the values they had before executing the Protection Override command on the last time. If contents of FPROT and/or DFPROT registers were modified by direct register writes while protection is overridden these modifications will be lost. Running Protection Override command to restore the contents of registers FPROT and DFPROT will not force them to the reset values.

Table 20-70. Protection Override Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != (001, 010 or 011) at command launch.
		Set if command not available in current mode (see Table 20-29).
		Set if protection is supposed to be restored (if key does not match or is invalid) and Protection Override command was not run previously (bit FPSTAT FPOVRD is 0), so there are no previous valid values of FPROT and DFPROT to be re-loaded.
		Set if Protection Update Selection[1:0] = 00 (in case of CCOBIX[2:0] = 010 or 011)
		Set if Protection Update Selection[1:0] = 00, CCOBIX[2:0] = 001 and a valid comparison key is loaded as a command parameter.
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

20.4.8 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 20-71. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

21.1.2 Modes of Operation

There are five modes the CAN Physical Layer can take (refer to 21.5.2 for details):

1. Shutdown mode

   In shutdown mode the CAN Physical Layer is fully de-biased including the wake-up receiver.
2. Normal mode

   In normal mode the transceiver is fully biased and functional. The SPLIT pin drives 2.5 V if enabled.
3. Pseudo-normal mode
   Same as normal mode with CANL driver disabled.
4. Listen-only mode
   Same as normal mode with transmitter de-biased.
5. Standby mode with configurable wake-up feature

   In standby mode the transceiver is fully de-biased. The wake-up receiver is enabled out of reset.

- CPU Run Mode
  The CAN Physical Layer is able to operate normally in modes 1 to 4.
- CPU Wait Mode
  The CAN Physical Layer operation is the same as in CPU run mode.
- CPU Stop Mode
  The CAN Physical Layer enters standby mode when the device voltage regulator switches to reduced performance mode (“RPM”) after a CPU stop mode request.
  If enabled, the wake-up pulse filtering mechanism is activated immediately at CPU stop mode entry.

21.1.3 Block Diagram

Figure 21-1 shows a block diagram of the CAN Physical Layer. The module consists of a precision receiver, a low-power wake-up receiver, an output driver and diagnostics.

condition instantaneously disappears as soon as the transmit driver is automatically being turned off. This state is locked and the application software must account for re-enabling the driver.

The recommended procedure to handle an over-current related bus error is:

1. On interrupt abort any scheduled transmissions
2. Read interrupt flag register to determine over-current source(s)
3. Clear related interrupt flag(s)
4. Retry CAN transmission
5. On interrupt abort any scheduled transmissions
6. Read interrupt flag register to determine over-current source(s)
7. If the same over-current error persists do not retry and run appropriate custom diagnostics

21.6.4 CPTXD-Dominant Timeout Recovery

Recovery from a CPTXD-dominant timeout error is attempted with the following sequence:

1. On CPTXD-dominant timeout interrupt set CPTXD input to recessive state
2. Wait until CPDT clear; exit loop if waiting for longer than 3 μs and report malfunction
3. Clear CPDTIF
4. Wait for min. 2 μs before attempting new transmission

Appendix B
CPMU Electrical Specifications (VREG, OSC, IRC, PLL)

B.1 VREG Electrical Specifications

Table B-1. Voltage Regulator Electrical Characteristics
(Junction Temperature From –40°C To +175°C unless otherwise stated)

Note: VDDA and VDDX must be shorted on the application board.							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
1		Input Voltages	V_{SUP}	3.5	—	40	V
2		Output Voltage Core Full Performance Mode Reduced Power Mode (stop mode)	V_{DD}	 1.72 —	 1.84 1.6	 1.98 —	 V V
3		Output Voltage Flash Full Performance Mode Reduced Power Mode (stop mode)	V_{DDF}	 2.6 —	 2.82 1.6	 2.9 —	 V V
4a		Output Voltage VDDX (with external PNP, ZVMC256) Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDX}	 4.90 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.10 5.10 5.10 5.75	 V V V V
4b		Output Voltage VDDX (with external PNP, other parts) Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDX}	 4.85 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.15 5.15 5.15 5.75	 V V V V
4c		Output Voltage VDDX (without external PNP)[1] Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDX}	 4.80 4.50 3.13 2.5	 4.95 4.95 — 5.5	 5.10 5.10 5.10 5.75	 V V V V
4d		VDDX dependence on temperature and VSUP input V_{SUP} > 6V. No external PNP.	V_{DDX}	—	50	80	mV
5a		Load Current VDDX[2][3] without external PNP Full Performance Mode, V_{SUP} > 6V, -40°C < T_J < 150°C	I_{DDX}	0	—	70	mA
5b		Load Current VDDX[2][3] without external PNP Full Performance Mode V_{SUP} > 6V Full Performance Mode 3.5V <= V_{SUP} <=6V Reduced Performance Mode (stop) V_{SUP} > =3.5V	I_{DDX}	 0 0 0	 — — —	 55 20 5	 mA mA mA