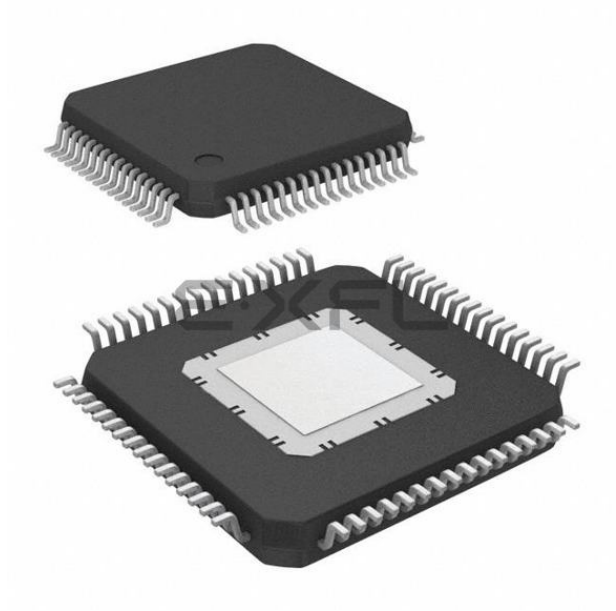

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f2vkh

1.6 Device Memory Map

Table 1-5 shows the device register memory map. All modules that can be instantiated more than once on S12 devices are listed with an index number, even if they are only instantiated once on this device family.

Table 1-5. Module Register Address Ranges

Address	Module	Size (Bytes)
0x0000–0x0003	Part ID Register Section 1.6.2	4
0x0004–0x000F	Reserved	12
0x0010–0x001F	INT	16
0x0020–0x006F	Reserved	80
0x0070–0x008F	MMC	32
0x0090–0x00FF	MMC Reserved	112
0x0100–0x017F	DBG	128
0x0180–0x01FF	Reserved	128
0x0200–0x033F	PIM	320
0x0340–0x037F	Reserved	64
0x0380–0x039F	FTMRZ	32
0x03A0–0x03BF	Reserved	32
0x03C0–0x03CF	RAM ECC	16
0x03D0–0x03FF	Reserved	48
0x0400–0x043F	TIM1 (ZVMC256 only)	64
0x0440–0x047F	Reserved	64
0x0480–0x04AF	PWM0 (ZVMC256 only)	48
0x04B0–0x04FF	Reserved[1]	80
0x0500–0x053F	PMF	64
0x0540–0x057F	Reserved	64
0x0580–0x059F	PTU	32
0x05A0–0x05BF	Reserved	32
0x05C0–0x05EF	TIM0	48
0x05F0–0x05FF	Reserved	16
0x0600–0x063F	ADC0	64
0x0640–0x067F	ADC1	64
0x0680–0x069F	Reserved	32
[2]0x06A0–0x06BF	GDU	32
0x06C0–0x06DF	CPMU	32

The exposed pad on the package bottom must be connected to a grounded contact pad on the PCB.

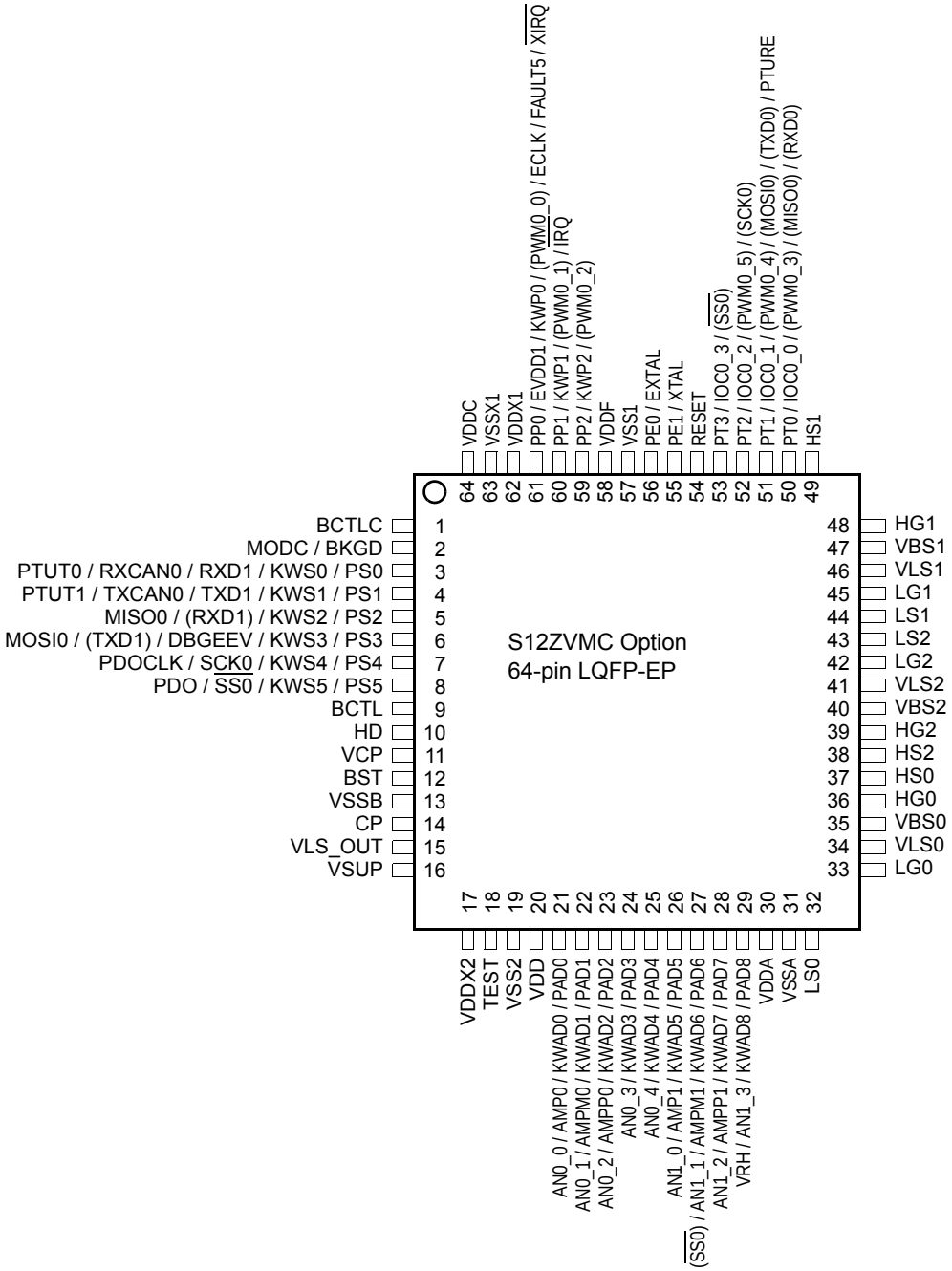

Figure 1-5. S12ZVMC Option 64-pin LQFP pin out

Chapter 2
Port Integration Module (S12ZVMPIMV3)

Table 2-1. Revision History

Rev. No. (Item No.)	Date	Sections Affected	Substantial Change(s)
V03.08	9 Jan 2015	Table 2-5 Table 2-6 Table 2-7 2.3.1/116 Table 2-9 Table 2-11	• Corrections
V03.09	22 Jan 2015		• Minor changes in wording
V03.10	23 Jan 2015	Figure 2-5 Table 2-13	• Corrected T0IC3RR1-0 description
V03.11	27 Jan 2015	2.3.1/116 2.3.2.3/128	• Changed T0C2RR1-0 specification
V03.12	10 Feb 2015	2.1.1/104 Table 2-5 Table 2-6	• Added TIM1 • Changed PWM0 routing
V03.13	16 Feb 2015	2.1.1/104	• Fixed typos and formatting
V03.14	19 Feb 2015	2.1.1/104 2.1.2/107 2.2/108 Table 2-39 Table 2-41	• Fixed typos and formatting
V03.15	16 Mar 2015	2.1.1/104 2.2/108	• Format updates
V03.16	22 Apr 2015	2.1.1/104	• Fixed typos and formatting
V03.17	12 Oct 2015	2.3.4/140	• Fixed typos and formatting
V03.18	12 Dec 2015	2.3.2.3/128	• Added bit description for T1IC0RR (MODRR2 register)

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02D6	PIES	R	0	0	PIES5[5]	PIES4[5]	PIES3	PIES2	PIES1	PIES0
		W								
0x02D7	PIFS	R	0	0	PIFS5[5]	PIFS4[5]	PIFS3	PIFS2	PIFS1	PIFS0
		W								
0x02D8–0x02DE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02DF	WOMS	R	0	0	WOMS5[5]	WOMS4[5]	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x02E0–0x02EF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F0	PTP	R	0	0	0	0	0	PTP2[5]	PTP1	PTP0
		W								
0x02F1	PTIP	R	0	0	0	0	0	PTIP2[5]	PTIP1	PTIP0
		W								
0x02F2	DDRP	R	0	0	0	0	0	DDRP2[5]	DDRP1	DDRP0
		W								
0x02F3	PERP	R	0	0	0	0	0	PERP2[5]	PERP1	PERP0
		W								
0x02F4	PPSP	R	0	0	0	0	0	PPSP2[5]	PPSP1	PPSP0
		W								
0x02F5	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F6	PIEP	R	OCIE1	0	0	0	0	PIEP2[5]	PIEP1	PIEP0
		W								
0x02F7	PIFP	R	OCIF1	0	0	0	0	PIFP2[5]	PIFP1	PIFP0
		W								

External pulldown device (Figure 2-38):

1. Enable analog function on HVI in non-direct mode (PTAENL[PTAENL0]=1, PTAENL[PTADIRL0]=0)
2. Select internal pullup device on HVI (PTPSL[PTPSL0]=1)
3. Enable function to force input buffer active on HVI in analog mode (PTTEL[PTTEL0]=1)
4. Verify PTIL=0 for a connected external pulldown device; read PTIL=1 for an open input

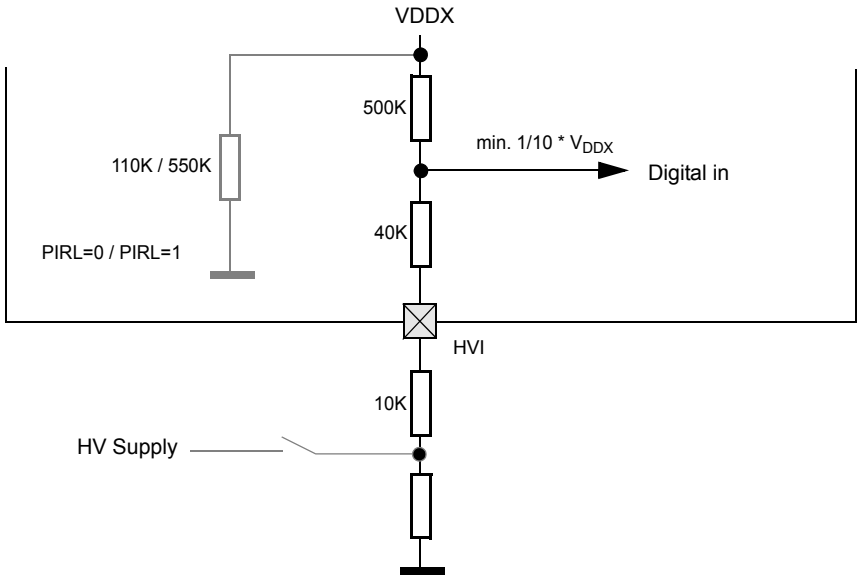

Figure 2-38. Digital Input Read with Pullup Enabled

External pullup device (Figure 2-39):

1. Enable analog function on HVI in non-direct mode (PTAENL[PTAENL0]=1, PTADIRL[PTADIRL0]=0)
2. Select internal pulldown device on HVI (PTPSL[PTPSL0]=0)
3. Enable function to force input buffer active on HVI in analog mode (PTTEL[PTTEL0]=1)
4. Verify PTIL0=1 for a connected external pullup device; read PTIL0=0 for an open input

3.4.2 Illegal Accesses

The S12ZMMC module monitors all memory traffic for illegal accesses. See Table 3-9 for a complete list of all illegal accesses.

Table 3-9. Illegal memory accesses

		S12ZCPU	S12ZBDC	ADCs and PTU
Register space	Read access	ok	ok	illegal access
	Write access	ok	ok	illegal access
	Code execution	illegal access		
RAM	Read access	ok	ok	ok
	Write access	ok	ok	ok
	Code execution	ok		
EEPROM	Read access	ok(1)	ok[1]	ok[1]
	Write access	illegal access	illegal access	illegal access
	Code execution	ok[1]		
Reserved Space	Read access	ok	ok	illegal access
	Write access	only permitted in SS mode	ok	illegal access
	Code execution	illegal access		
Reserved Read-only Space	Read access	ok	ok	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		
NVM IFR	Read access	ok[1]	ok[1]	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		
Program NVM	Read access	ok[1]	ok[1]	ok[1]
	Write access	illegal access	illegal access	illegal access
	Code execution	ok[1]		
Unmapped Space	Read access	illegal access	illegal access	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		

1. Unsupported NVM accesses during NVM command execution (“collisions”), are treated as illegal accesses.

Illegal accesses are reported in several ways:

- All illegal accesses performed by the S12ZCPU trigger machine exceptions.
- All illegal accesses performed through the S12ZBDC interface, are captured in the ILLACC bit of the BDCCSRL register.

Table 6-9. DBGTCRH Field Descriptions

Field	Description
6 TSOURCE	**Trace Control Bits** — The TSOURCE enables the tracing session. 0 No CPU tracing/profiling selected 1 CPU tracing/profiling selected
5–4 TRANGE	**Trace Range Bits** — The TRANGE bits allow filtering of trace information from a selected address range when tracing from the CPU in Detail mode. These bits have no effect in other tracing modes. To use a comparator for range filtering, the corresponding COMPE bit must remain cleared. If the COMPE bit is set then the comparator is used to generate events and the TRANGE bits have no effect. See Table 6-10 for range boundary definition.
3–2 TRCMOD	**Trace Mode Bits** — See Section 6.4.5.2 for detailed Trace Mode descriptions. In Normal Mode, change of flow information is stored. In Loop1 Mode, change of flow information is stored but redundant entries into trace memory are inhibited. In Detail Mode, address and data for all memory and register accesses is stored. See Table 6-11.
1–0 TALIGN	**Trigger Align Bits** — These bits control whether the trigger is aligned to the beginning, end or the middle of a tracing or profiling session. See Table 6-12.

Table 6-10. TRANGE Trace Range Encoding

TRANGE	Tracing Range
00	Trace from all addresses (No filter)
01	Trace only in address range from $00000 to Comparator D
10	Trace only in address range from Comparator C to $FFFFFF
11	Trace only in range from Comparator C to Comparator D

Table 6-11. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	Normal
01	Loop1
10	Detail
11	Pure PC

Table 6-12. TALIGN Trace Alignment Encoding

TALIGN	Description
00	Trigger ends data trace
01	Trigger starts data trace
10	32 lines of data trace follow trigger
11[1]	Reserved

1. Tracing/Profiling disabled.

6.3.2.14 Debug Comparator A Data Register (DBGAD)

Address: 0x0118, 0x0119, 0x011A, 0x011B

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-16. Debug Comparator A Data Register (DBGAD)

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

This register can be accessed with a byte resolution, whereby DBGAD0, DBGAD1, DBGAD2, DBGAD3 map to DBGAD[31:0] respectively.

Table 6-29. DBGAD Field Descriptions

Field	Description
31–16 Bits[31:16] (DBGAD0, DBGAD1)	**Comparator Data Bits** — These bits control whether the comparator compares the data bus bits to a logic one or logic zero. The comparator data bits are only used in comparison if the corresponding data mask bit is logic 1. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one
15–0 Bits[15:0] (DBGAD2, DBGAD3)	**Comparator Data Bits** — These bits control whether the comparator compares the data bus bits to a logic one or logic zero. The comparator data bits are only used in comparison if the corresponding data mask bit is logic 1. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

6.3.2.15 Debug Comparator A Data Mask Register (DBGADM)

Address: 0x011C, 0x011D, 0x011E, 0x011F

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-17. Debug Comparator A Data Mask Register (DBGADM)

Read: Anytime.

Table 6-35. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
1	1	1	Read match

6.3.2.19 Debug Comparator C Address Register (DBGCAH, DBGCAM, DBGCAL)

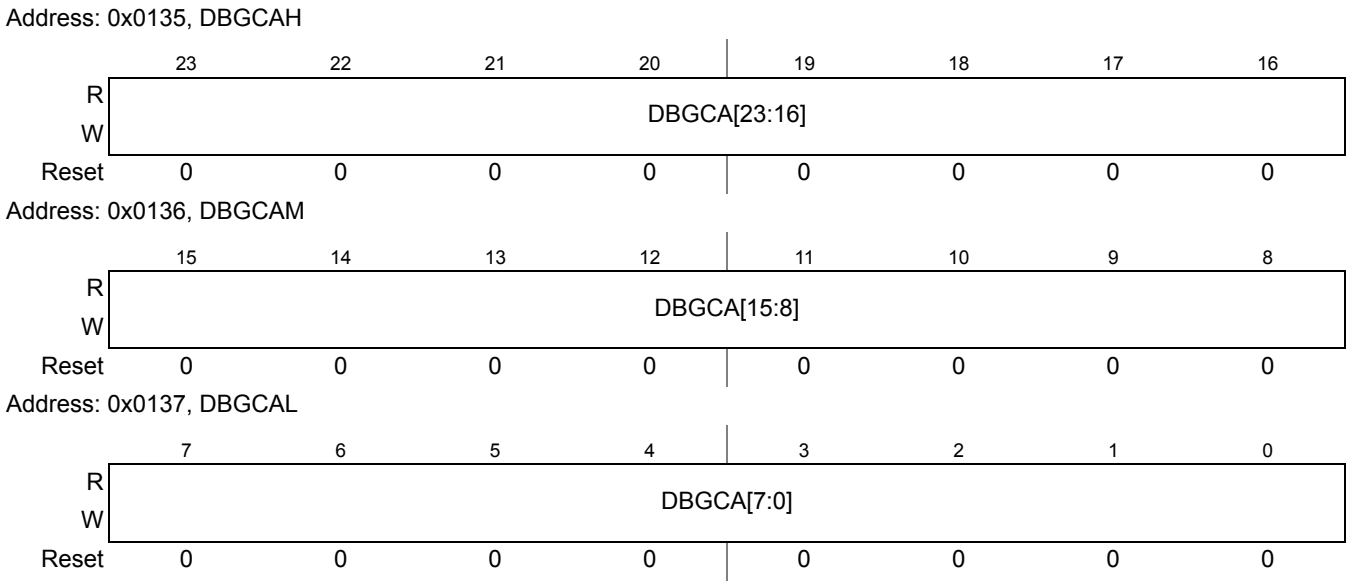

Figure 6-21. Debug Comparator C Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-36. DBGCAH, DBGCAM, DBGCAL Field Descriptions

Field	Description
23–16 DBGCA [23:16]	**Comparator Address Bits [23:16]**— These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one
15–0 DBGCA [15:0]	**Comparator Address Bits**[15:0]— These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

Table 8-16. COP Watchdog Rates if COPOSCSEL1=1.

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is ACLK divided by 2)
0	0	0	COP disabled
0	0	1	2^{7}
0	1	0	2^{9}
0	1	1	2^{11}
1	0	0	2^{13}
1	0	1	2^{15}
1	1	0	2^{16}
1	1	1	2^{17}

8.3.2.25 S12CPMU_UHV_V10_V6 Protection Register (CPMUPROT)

This register protects the clock configuration registers from accidental overwrite:

CPMUSYNR, CPMUREFDIV, CPMUCLKS, CPMUPLL, CPMUIRCTRIMH/L, CPMUOSC and CPMUOSC2

Module Base + 0x001B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PROT
W								
Reset	0	0	0	0	0	0	0	0

Figure 8-36. S12CPMU_UHV_V10_V6 Protection Register (CPMUPROT)

Read: Anytime

Write: Anytime

Field	Description
PROT	**Clock Configuration Registers Protection Bit** — This bit protects the clock configuration registers from accidental overwrite (see list of protected registers above): Writing 0x26 to the CPMUPROT register clears the PROT bit, other write accesses set the PROT bit. 0 Protection of clock configuration registers is disabled. 1 Protection of clock configuration registers is enabled. (see list of protected registers above).

8.3.2.27 Voltage Regulator Control Register (CPMUVREGCTL)

The CPMUVREGCTL allows to enable or disable certain parts of the voltage regulator.This register must be configured after system startup.

Module Base + 0x001D

	7	6	5	4	3	2	1	0
R W	VRH2EN[1]	VRH1EN[1]	EXTS2ON[1]	EXTS1ON[(1)]	0	EXTCON	EXTXON	INTXON
Reset	0	0	0	0	0	1	1	1

= Unimplemented or Reserved

Figure 8-38. Voltage Regulator Control Register (CPMUVREGCTL)

1. Only available in V10

Read: Anytime

Write: VRH2EN, VRH1EN, EXTS2ON, EXTS1ON anytime
Write: EXTCON, EXTXON, INTXON once in normal modes, anytime in special modes

Table 8-30. Effects of writing the EXTXON and INTXON bits

value of EXTXON to be written	value of INTXON to be written	Write Access
0	0	blocked, no effect
0	1	legal access
1	0	legal access
1	1	blocked, no effect

Table 8-31. CPMUVREGCTL Field Descriptions

Field	Description
7 VRH2EN	**VRH2 Enable Bit** — This bits switches VDDS2 pin to VRH2 of ADC. 0 VRH2 of ADC disconnected (open) 1 VRH2 of ADC connected to VDDS2. In RPM VRH2 is always disconnected from VDDS2 regardless of the value of the VRH2EN bit.
6 VRH1EN	**VRH1 Enable Bit** — This bits switches VDDS1 pin to VRH1 of ADC. 0 VRH1 of ADC disconnected (open) 1 VRH1 of ADC connected to VDDS1. In RPM VRH1 is always disconnected from VDDS1 regardless of the value of the VRH1EN bit.
5 EXTS2ON	**External voltage regulator Enable Bit for VDDS2 domain** — Should be enabled after system startup if VDDS2 is used. 0 VDDS2 domain disabled 1 VDDS2 domain enabled. BCTLS2 pin is active.

11.3.2.13 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 11-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 11-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	Output Compare Pin Disconnect Bits 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

11.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 11-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

NOTE

The IPOL*x* bits take effect at the beginning of the next PWM cycle, regardless of the state of the LDOK bit or global load OK. Select top/bottom software correction by writing 01 to the current select bits, ISENS[1:0], in the PWM control register. Reading the IPOL*x* bits read the buffered value and not necessarily the value currently in effect.

15.3.2.14 PMF Value 0-5 Register (PMFVAL0-PMFVAL5)

Address: Module Base + 0x0010 PMFVAL0
Module Base + 0x0012 PMFVAL1
Module Base + 0x0014 PMFVAL2
Module Base + 0x0016 PMFVAL3
Module Base + 0x0018 PMFVAL4
Module Base + 0x001A PMFVAL5

Access: User read/write(1)

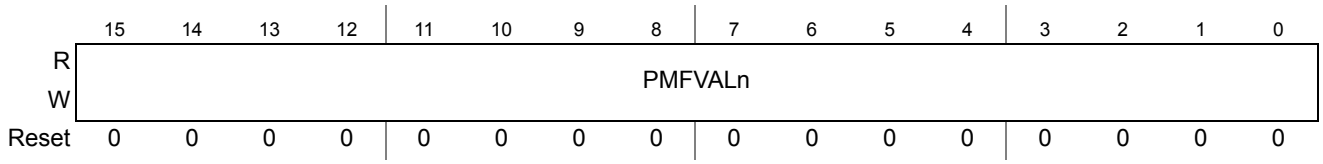

Figure 15-17. PMF Value *n* Register (PMFVAL*n*)

1. Read: Anytime
   Write: Anytime

Table 15-22. PMFVAL*n* Field Descriptions

Field	Description
15–0 PMFVAL*n*	**PMF Value n Bits** — The 16-bit signed value in this buffered register is the pulse width in PWM clock periods. A value less than or equal to zero deactivates the PWM output for the entire PWM period. A value greater than, or equal to the modulus, activates the PWM output for the entire PWM period. See Table 15-40**.** The terms activate and deactivate refer to the high and low logic states of the PWM output. **Note:** PMFVAL*n* is buffered. The value written does not take effect until the related or global load OK bit is set and the next PWM load cycle begins. Reading PMFVAL*n* returns the value in the buffer and not necessarily the value the PWM generator is currently using. *n* is 0, 1, 2, 3, 4 and 5.

15.3.2.15 PMF Reload Overrun Interrupt Enable Register (PMFROIE)

Address: Module Base + 0x001C

Access: User read/write(1)

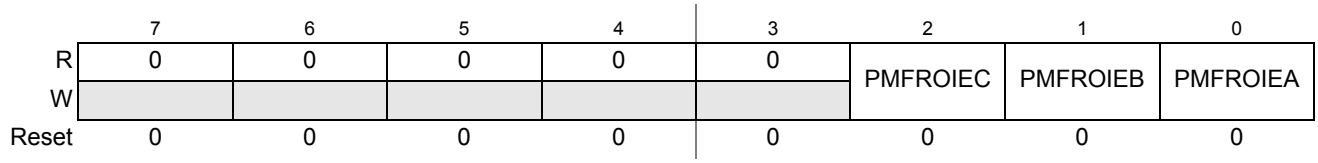

Figure 15-18. PMF Interrupt Enable Register (PMFROIE)

1. Read: Anytime
   Write: Anytime

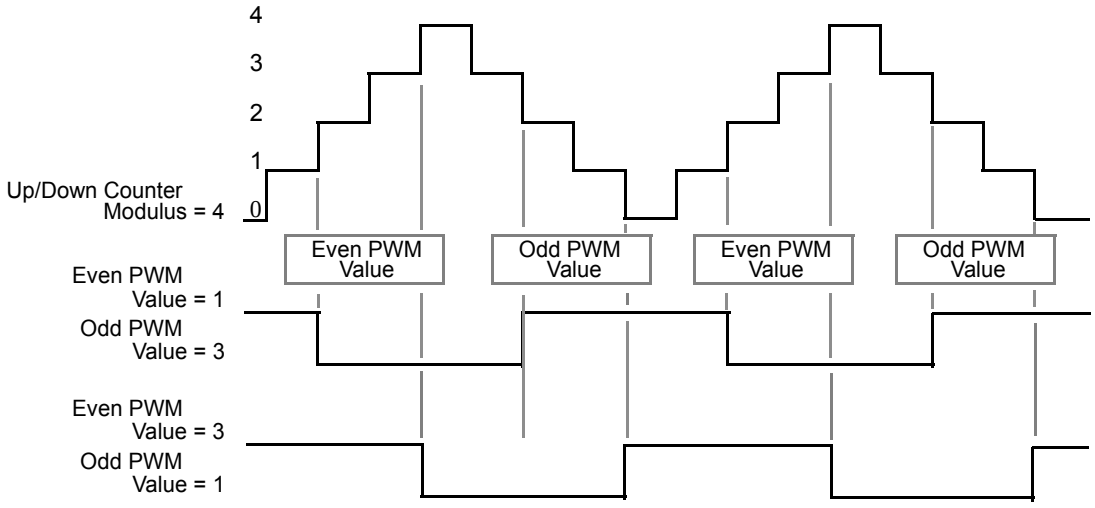

Figure 15-62. Asymmetric Waveform - Phase Shift PWM Output

15.4.8 Variable Edge Placement PWM Output

In complementary edge-aligned mode, the timing of both edges of the PWM output can be controlled using the PEC*x* bits in the PMFICCTL register and the CINV*n* bits in the PMFCINV register.

The edge-aligned signal created by the even value register and the associated CINV*n* bit is ANDed with the signal created by the odd value register and its associated CINV*n* bit. The resulting signal can optionally be negated by PINV*x* and is then fed into the complement and deadtime logic (Figure 15-63). If the value of the inverted register exceeds the non-inverted register value, no output pulse is generated (0% or 100% duty cycle). See right half of Figure 15-64.

In contrast to asymmetric PWM output mode, the PWM phase shift can pass the PWM cycle boundary.

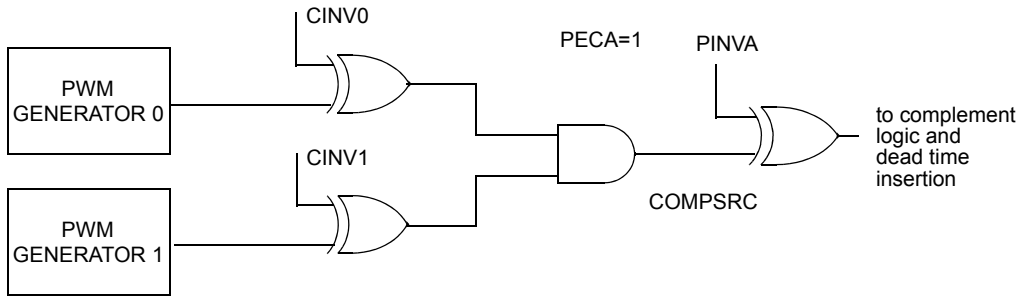

Figure 15-63. Logic AND Function with Signal Inversions

In Figure 16-22 the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The noise flag is not set because the noise occurred before the start bit was found.

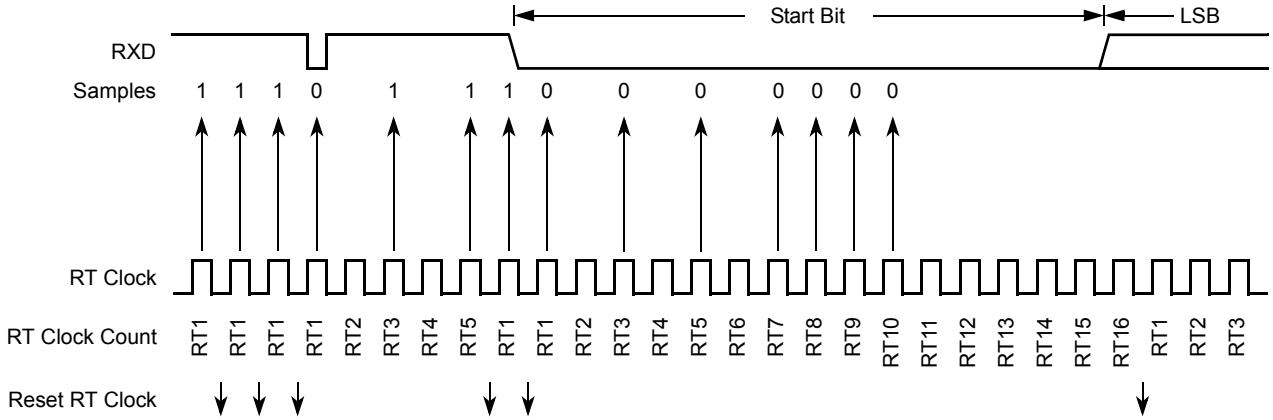

Figure 16-22. Start Bit Search Example 1

In Figure 16-23, verification sample at RT3 is high. The RT3 sample sets the noise flag. Although the perceived bit time is misaligned, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

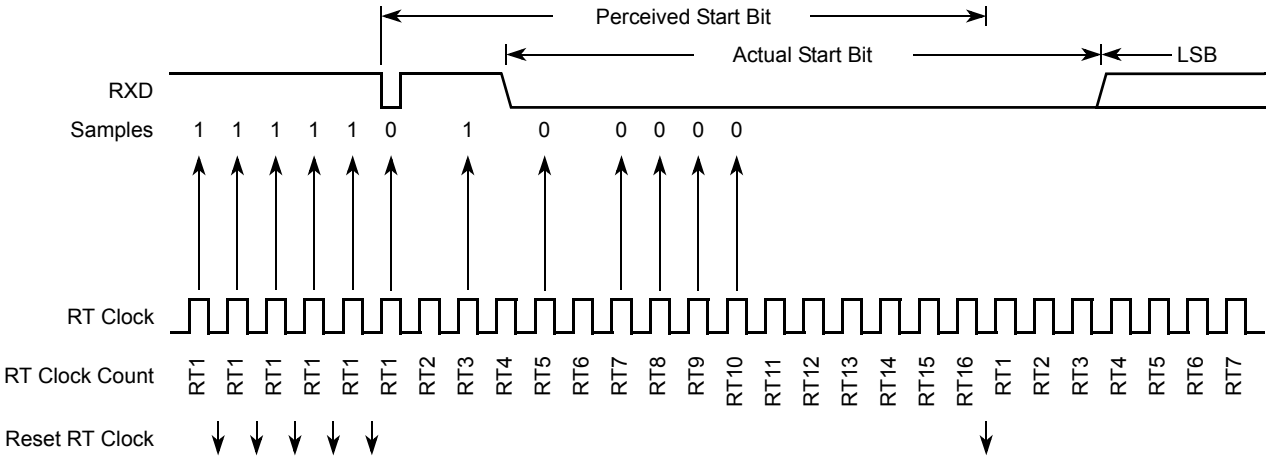

Figure 16-23. Start Bit Search Example 2

The number of DPS bits depends on the size of the implemented EEPROM. The whole implemented EEPROM range can always be protected. Each DPS value increment increases the size of the protected range by 32-bytes. Thus to protect a 1 KB range DPS[4:0] must be set (protected range of 32 x 32 bytes).

20.3.2.11 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F(1)	F1	F1	F1	F1	F1	F1	F1

= Unimplemented or Reserved

Figure 20-16. Flash Option Register (FOPT)

1. Loaded from Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but can only be written in special mode.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0xFF_FE0E located in P-Flash memory (see Table 20-4) as indicated by reset condition F in Figure 20-16. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 20-26. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device overview for proper use of the NV bits.

20.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-17. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 20-23. Flash Common Command Object 2 Low Register (FCCOB2LO)

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 20-24. Flash Common Command Object 3 High Register (FCCOB3HI)

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 20-25. Flash Common Command Object 3 Low Register (FCCOB3LO)

Offset Module Base + 0x0014

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 20-26. Flash Common Command Object 4 High Register (FCCOB4HI)

Offset Module Base + 0x0015

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 20-27. Flash Common Command Object 4 Low Register (FCCOB4LO)

Write: Anytime

Table 22-2. PWME Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PWME7	Pulse Width Channel 7 Enable 0 Pulse width channel 7 is disabled. 1 Pulse width channel 7 is enabled. The pulse modulated signal becomes available at PWM output bit 7 when its clock source begins its next cycle.
6 PWME6	Pulse Width Channel 6 Enable 0 Pulse width channel 6 is disabled. 1 Pulse width channel 6 is enabled. The pulse modulated signal becomes available at PWM output bit 6 when its clock source begins its next cycle. If CON67=1, then bit has no effect and PWM output line 6 is disabled.
5 PWME5	Pulse Width Channel 5 Enable 0 Pulse width channel 5 is disabled. 1 Pulse width channel 5 is enabled. The pulse modulated signal becomes available at PWM output bit 5 when its clock source begins its next cycle.
4 PWME4	Pulse Width Channel 4 Enable 0 Pulse width channel 4 is disabled. 1 Pulse width channel 4 is enabled. The pulse modulated signal becomes available at PWM, output bit 4 when its clock source begins its next cycle. If CON45 = 1, then bit has no effect and PWM output line 4 is disabled.
3 PWME3	Pulse Width Channel 3 Enable 0 Pulse width channel 3 is disabled. 1 Pulse width channel 3 is enabled. The pulse modulated signal becomes available at PWM, output bit 3 when its clock source begins its next cycle.
2 PWME2	Pulse Width Channel 2 Enable 0 Pulse width channel 2 is disabled. 1 Pulse width channel 2 is enabled. The pulse modulated signal becomes available at PWM, output bit 2 when its clock source begins its next cycle. If CON23 = 1, then bit has no effect and PWM output line 2 is disabled.
1 PWME1	Pulse Width Channel 1 Enable 0 Pulse width channel 1 is disabled. 1 Pulse width channel 1 is enabled. The pulse modulated signal becomes available at PWM, output bit 1 when its clock source begins its next cycle.
0 PWME0	Pulse Width Channel 0 Enable 0 Pulse width channel 0 is disabled. 1 Pulse width channel 0 is enabled. The pulse modulated signal becomes available at PWM, output bit 0 when its clock source begins its next cycle. If CON01 = 1, then bit has no effect and PWM output line 0 is disabled.

22.3.2.2 PWM Polarity Register (PWMPOL)

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit in the PWMPOL register. If the polarity bit is one, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x011C	DBGADM0	R W	Bit 31	30	29	28	27	26	25	Bit 24
0x011D	DBGADM1	R W	Bit 23	22	21	20	19	18	17	Bit 16
0x011E	DBGADM2	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x011F	DBGADM3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0120	DBGBCTL	R W	0	0	INST	0	RW	RWE	reserved	COMPE
0x0121- 0x0124	Reserved	R W	0	0	0	0	0	0	0	0
0x0125	DBGBAH	R W	DBGBA[23:16]							
0x0126	DBGBAM	R W	DBGBA[15:8]							
0x0127	DBGBAL	R W	DBGBA[7:0]							
0x0128- 0x012F	Reserved	R W	0	0	0	0	0	0	0	0
0x0130	DBGCCTL2	R W	0	NDB	INST	0	RW	RWE	reserved	COMPE
0x0131- 0x0134	Reserved	R W	0	0	0	0	0	0	0	0
0x0135	DBGCAH2	R W	DBGCA[23:16]							
0x0136	DBGCAM2	R W	DBGCA[15:8]							
0x0137	DBGCAL2	R W	DBGCA[7:0]							
0x0138	DBGCD02	R W	Bit 31	30	29	28	27	26	25	Bit 24
0x0139	DBGCD12	R W	Bit 23	22	21	20	19	18	17	Bit 16
0x013A	DBGCD22	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x013B	DBGCD32	R W	Bit 7	6	5	4	3	2	1	Bit 0