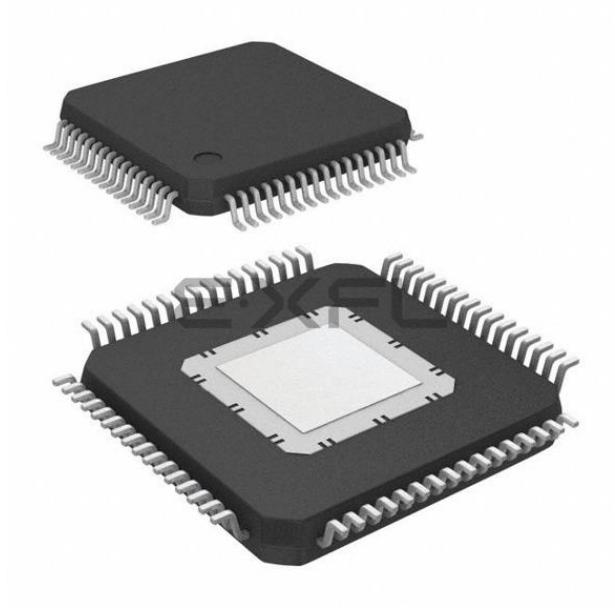

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f2wkh

- 2 trigger input sources and software trigger source
- 2 trigger outputs
- One 16-bit delay register pre-trigger output
- Operation in One-Shot or Continuous modes

1.4.9 LIN physical layer transceiver (ZVML devices only)

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4kBit/s, 20kBit/s and Fast Mode (up to 250kBit/s).
- Switchable 34kΩ/330kΩ pull-ups (in shutdown mode, 330kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Over-current protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.
- Automatic transmitter shutdown in case of an over-current or TxD-dominant timeout.
- Fulfills the OEM “Hardware Requirements for LIN (CAN and FlexRay) Interfaces in Automotive Applications” v1.3.

1.4.10 Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 16-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN

1.4.11 Multi-Scalable Controller Area Network (MSCAN)

- Implementation of the CAN protocol — Version 2.0A/B
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization using a “local priority” concept
- Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, or four 16-bit filters, or either 8-bit filters
- Programmable wake-up functionality with integrated low-pass filter

1.6 Device Memory Map

Table 1-5 shows the device register memory map. All modules that can be instantiated more than once on S12 devices are listed with an index number, even if they are only instantiated once on this device family.

Table 1-5. Module Register Address Ranges

Address	Module	Size (Bytes)
0x0000–0x0003	Part ID Register Section 1.6.2	4
0x0004–0x000F	Reserved	12
0x0010–0x001F	INT	16
0x0020–0x006F	Reserved	80
0x0070–0x008F	MMC	32
0x0090–0x00FF	MMC Reserved	112
0x0100–0x017F	DBG	128
0x0180–0x01FF	Reserved	128
0x0200–0x033F	PIM	320
0x0340–0x037F	Reserved	64
0x0380–0x039F	FTMRZ	32
0x03A0–0x03BF	Reserved	32
0x03C0–0x03CF	RAM ECC	16
0x03D0–0x03FF	Reserved	48
0x0400–0x043F	TIM1 (ZVMC256 only)	64
0x0440–0x047F	Reserved	64
0x0480–0x04AF	PWM0 (ZVMC256 only)	48
0x04B0–0x04FF	Reserved[1]	80
0x0500–0x053F	PMF	64
0x0540–0x057F	Reserved	64
0x0580–0x059F	PTU	32
0x05A0–0x05BF	Reserved	32
0x05C0–0x05EF	TIM0	48
0x05F0–0x05FF	Reserved	16
0x0600–0x063F	ADC0	64
0x0640–0x067F	ADC1	64
0x0680–0x069F	Reserved	32
[2]0x06A0–0x06BF	GDU	32
0x06C0–0x06DF	CPMU	32

Table 1-9. Pin Summary For 80-Pin Package Option (ZVMC256 Only) (Sheet 2 of 5)

Pin #	Pin Name	Function (Priority and routing options defined in PIM chapter)							Supply	Internal Pull Resistor	
		1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.		CTRL	Reset State
11	BCTLS 1	—	—	—	—	—	—		—	—	—
12	VDDS1	VRH0_1	VRH1_1	—	—	—	—		—	—	—
13	SNPS2	—	—	—	—	—	—		—	—	—
14	BCTLS 2	—	—	—	—	—	—		—	—	—
15	VDDS2	VRH0_2	VRH1_2	—	—	—	—		—	—	—
16	LD0	—	—	—	—	—	—		—	—	—
17	LD1	—	—	—	—	—	—		—	—	—
18	LD2	—	—	—	—	—	—		—	—	—
19	PAD0	KWAD0	AN0_0	AMP0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
20	PAD1	KWAD1	AN0_1	AMPM0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
21	PAD2	KWAD2	AN0_2	AMPP0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
22	PAD3	KWAD3	AN0_3	—	—	—	—		V_{DDA}	PERADL/PPSADL	Off
23	PAD4	KWAD4	AN0_4	—	—	—	—		V_{DDA}	PERADL/PPSADL	Off
24	PAD5	KWAD5	AN1_0	AMP1	—	—	—		V_{DDA}	PERADL/PPSADL	Off
25	PAD6	KWAD6	AN1_1	$\overline{SS0}$	AMPM1	—	—		V_{DDA}	PERADL/PPSADL	Off
26	PAD7	KWAD7	AN1_2	AMPP1	—	—	—		V_{DDA}	PERADL/PPSADL	Off
27	PAD8	KWAD8	AN1_3	—	—	—	—		V_{DDA}	PERADH/PPSADH	Off

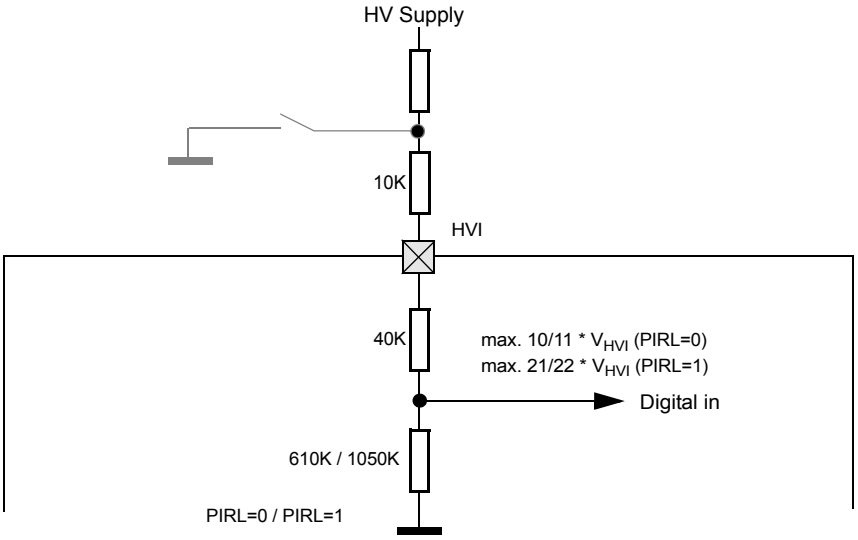


Figure 2-39. Digital Input Read with Pulldown Enabled

2.5.3 Over-Current Protection on EVDD1

Pin PP0 can be used as general-purpose I/O or due to its increased current capability in output mode as a switchable external power supply pin (EVDD1) for external devices like Hall sensors.

EVDD1 is supplied by the digital pad supply VDDX.

An over-current monitor is implemented to protect the controller from short circuits or excess currents on the output which can only arise if the pin is configured for full drive. Although the full drive current is available on the high and low side, the protection is only available on the high side with a current direction from EVDD1 to VSSX. There is also no protection to voltages higher than V_{DDX}.

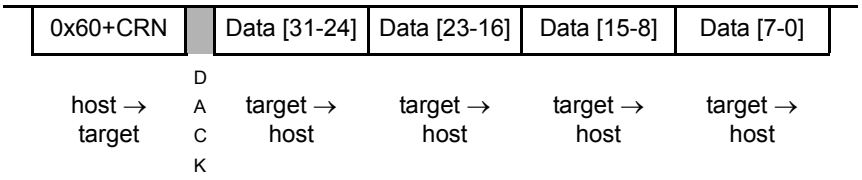
To enable the over-current monitor set the related OCPE1 bit in register PIMMISC.

In stop mode the over-current monitor is disabled for power saving. The increased current capability cannot be maintained to supply the external device. Therefore when using the pin as power supply the external load must be powered down prior to entering stop mode by driving the output low.

An over-current condition is detected if the output current level exceeds the threshold I_{OCD} in run mode. The output driver is immediately forced low and the over-current interrupt flag OCIFx asserts. Refer to Section 2.4.5, “Over-Current Interrupt”.

5.4.4.10 READ_Rn

Read CPU register **Active Background**



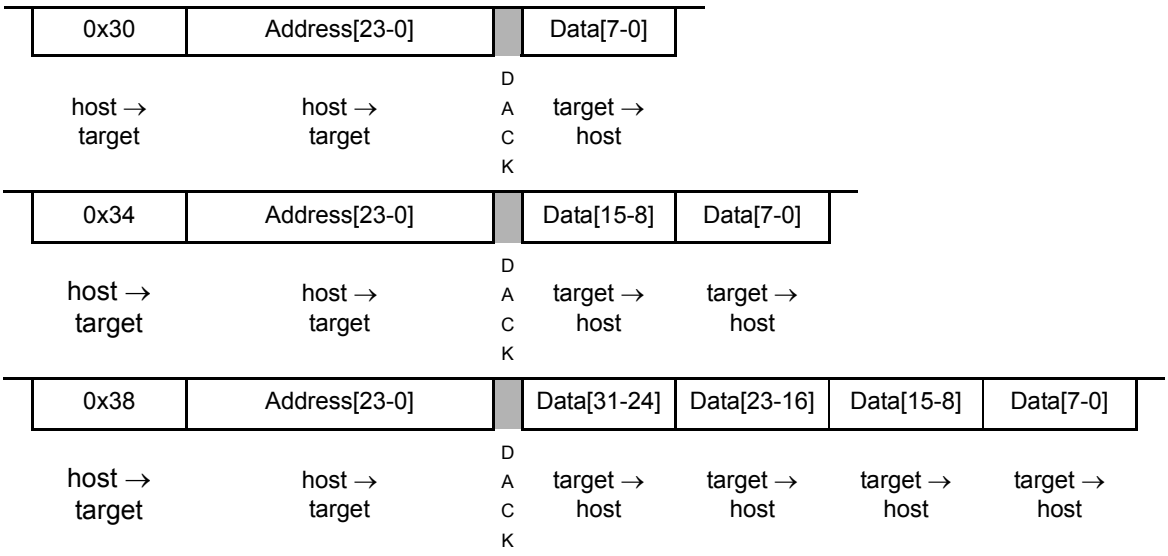
This command reads the selected CPU registers and returns the 32-bit result. Accesses to CPU registers are always 32-bits wide, regardless of implemented register width. Bytes that are not implemented return zero. The register is addressed through the CPU register number (CRN). See Section 5.4.5.1 for the CRN address decoding. If enabled, an ACK pulse is driven before the data bytes are transmitted.

If the device is not in active BDM, this command is illegal, the ILLCMD bit is set and no access is performed.

5.4.4.11 READ_MEM.sz, READ_MEM.sz_WS

READ_MEM.sz

Read memory at the specified address **Non-intrusive**



7.2.2.3 ECC Interrupt Flag Register (ECCIF)

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIF
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime, write 1 to clear

Figure 7-4. ECC Interrupt Flag Register (ECCIF)

Table 7-4. ECCIF Field Description

Field	Description
0 SBEEIF	Single bit ECC Error Interrupt Flag — The flag is set to 1 when a single bit ECC error occurs. 0 No occurrences of single bit ECC error since the last clearing of the flag 1 Single bit ECC error has occured since the last clearing of the flag

Be aware that the output frequency varies with the TC trimming. A frequency trimming correction is therefore necessary. The values provided in Table 8-28 are typical values at ambient temperature which can vary from device to device.

8.3.2.24 S12CPMU_UHV_V10_V6 Oscillator Register (CPMUOSC)

This registers configures the external oscillator (XOSCLCP).

Module Base + 0x001A

	7	6	5	4	3	2	1	0
R	OSCE	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-35. S12CPMU_UHV_V10_V6 Oscillator Register (CPMUOSC)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

Table 8-29. CPMUOSC Field Descriptions

Field	Description
7 OSCE	**Oscillator Enable Bit** — This bit enables the external oscillator (XOSCLCP). The UPOSC status bit in the CPMIUFLG register indicates when the oscillation is stable and when OSCCLK can be selected as source of the Bus Clock or source of the COP or RTI.**If the oscillator clock monitor reset is enabled (OMRE = 1 in CPMUOSC2 register), then a loss of oscillation will lead to an oscillator clock monitor reset.** 0 External oscillator is disabled. REFCLK for PLL is IRCCLK. 1 External oscillator is enabled. Oscillator clock monitor is enabled. External oscillator is qualified by PLLCLK. REFCLK for PLL is the external oscillator clock divided by REFDIV. If OSCE bit has been set (write “1”) the EXTAL and XTAL pins are exclusively reserved for the oscillator and they can not be used anymore as general purpose I/O until the next system reset. **Note:** When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.

8.4.6 System Clock Configurations

8.4.6.1 PLL Engaged Internal Mode (PEI)

This mode is the default mode after System Reset or Power-On Reset.

The Bus Clock is based on the PLLCLK, the reference clock for the PLL is internally generated (IRC1M). The PLL is configured to 50 MHz VCOCLK with POSTDIV set to 0x03. If locked (LOCK=1) this results in a PLLCLK of 12.5 MHz and a Bus Clock of 6.25 MHz. The PLL can be re-configured to other bus frequencies.

The clock sources for COP and RTI can be based on the internal reference clock generator (IRC1M) or the RC-Oscillator (ACLK).

8.4.6.2 PLL Engaged External Mode (PEE)

In this mode, the Bus Clock is based on the PLLCLK as well (like PEI). The reference clock for the PLL is based on the external oscillator.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock or the RC-Oscillator (ACLK).

This mode can be entered from default mode PEI by performing the following steps:

1. Configure the PLL for desired bus frequency.
2. Enable the external Oscillator (OSCE bit).
3. Wait for oscillator to start-up and the PLL being locked (LOCK = 1) and (UPOSC =1).
4. Clear all flags in the CPMUIFLG register to be able to detect any future status bit change.
5. Optionally status interrupts can be enabled (CPMUINT register).

Loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status (UPOSC=0) in PEE mode is as follows:

- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

9.7 Resets

At reset the ADC12B_LBA is disabled and in a power down state. The reset state of each individual bit is listed within Section 9.5.2, “Register Descriptions” which details the registers and their bit-fields.

9.8 Interrupts

The ADC supports three types of interrupts:

- Conversion Interrupt
- Sequence Abort Interrupt
- Error and Conversion Flow Control Issue Interrupt

Each of the interrupt types is associated with individual interrupt enable bits and interrupt flags.

9.8.1 ADC Conversion Interrupt

The ADC provides one conversion interrupt associated to 16 interrupt enable bits with dedicated interrupt flags. The 16 interrupt flags consist of:

- 15 conversion interrupt flags which can be associated to any conversion completion.
- One additional interrupt flag which is fixed to the “End Of List” conversion command type within the active CSL.

The association of the conversion number with the interrupt flag number is done in the conversion command.

9.8.2 ADC Sequence Abort Done Interrupt

The ADC provides one sequence abort done interrupt associated with the sequence abort request for conversion flow control. Hence, there is only one dedicated interrupt flag and interrupt enable bit for conversion sequence abort and it occurs when the sequence abort is done.

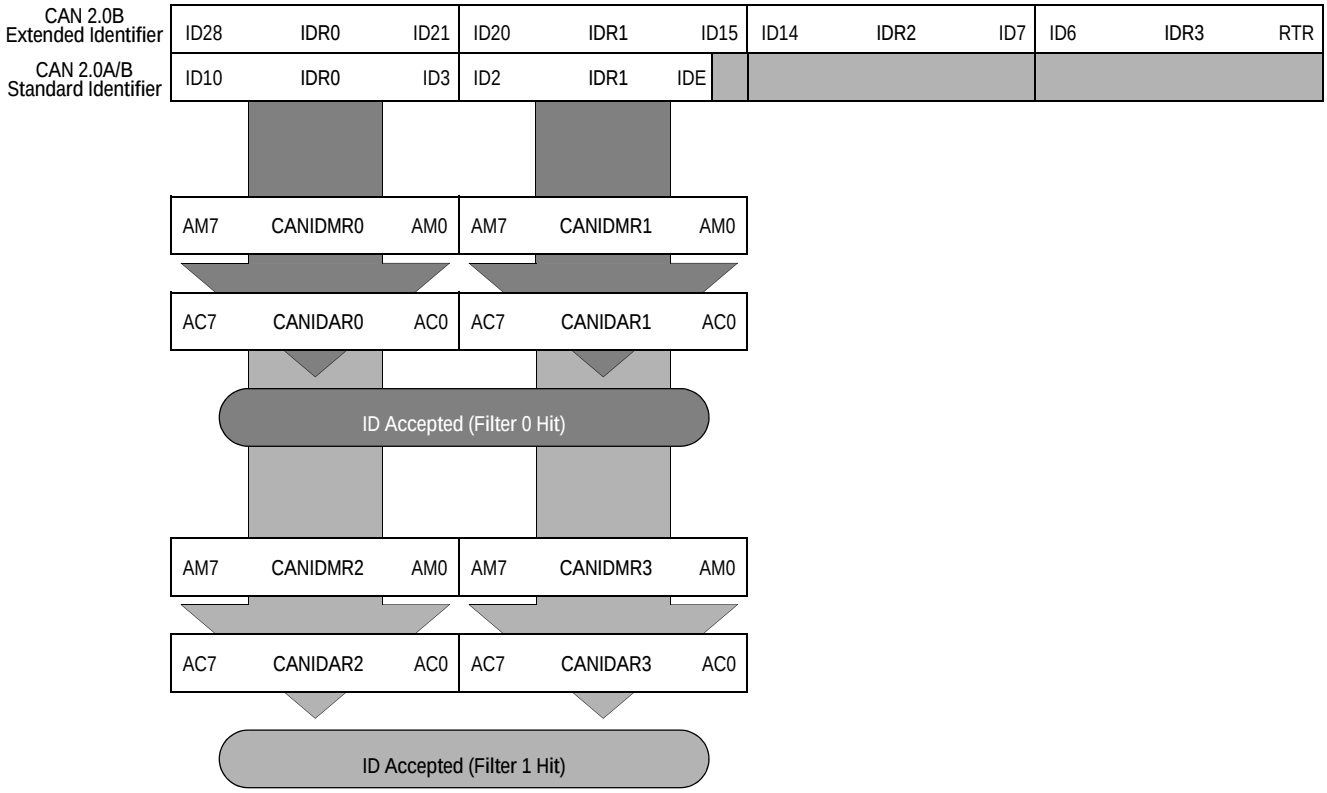


Figure 13-41. 16-bit Maskable Identifier Acceptance Filters

Table 14-4. PTUC Register Field Descriptions

Field	Description
0 PTULDOK	**Load Okay** — When this bit is set by the software, this allows the trigger generator to switch to the alternative list and load the trigger time values at the next reload event from the new list. If the reload event occurs when the PTULDOK bit is not set then the trigger generator generates a reload overrun event and uses the previously used list. At the next reload event this bit is cleared by control logic. Write 0 is only possible if TG0EN and TG1EN is cleared. The PTULDOK can be used by other module as global load OK (glb_ldok).

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKB bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODB returns the value in the buffer. It is not necessarily the value the PWM generator B is currently using.

15.3.2.28 PMF Deadtime B Register (PMFDTMB)

Address: Module Base + 0x002E — Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PMFDTMB											
W																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Figure 15-33. PMF Deadtime B Register (PMFDTMB)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to the maximum value of 0x0FFF, selecting a deadtime of 4095 PWM clock cycles. Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows:

$$T_{DEAD\_B} = PMFDTMB / f_{PWM\_B} = PMFDTMB \times P_B \times T_{core} \qquad \textit{Eqn. 15-2}$$

15.3.2.29 PMF Enable Control C Register (PMFENCC)

Address: Module Base + 0x0030 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-34. PMF Enable Control C Register (PMFENCC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. GLDOKC and RSTRTC cannot be modified after the WP bit is set.

Chapter 18
Gate Drive Unit (GDU)

Table 18-1. Revision History Table

Version Number	Revision Date	Description of Changes
V6 Initial Draft	25-January-2015	Initial Draft based on GDUV4/V5 with following changes for SR Motor support: • additional drain connections LD[2:0] for SR motor drive • GDUCTR1 register with control bits for SR motor drive • Removed EPRES control bit functionality for V5 and V6 • Changed GSUF startup flag functionality for V6
V6	28-January-2016	• Removed EPRES Functionality • Common specification for GSUF with reference to device overview • Common specification for GDUCTR1 with reference to device overview
V6.1	4-February-2016	• Corrected Table 1-2 TDEL availability and low-side driver on or off out of reset dependent on NVM option for GDU V4
V6.2	17-May-2016	• Removed desaturation comparator level and desaturation comparator filter time constant (relocated in electrical spec.)
V6.2	17-May-2016	• Removed desaturation comparator level and desaturation

18.1 Differences GDUV4 vs GDUV5 vs GDUV6

Table 18-2. GDUV4/V5/V6 Differences(1)

Feature	GDU V4	GDU V5	GDU V6
TDEL control bit for t_{delon}/t_{deloff}	available[1.]	not available	available
Number of Overcurrent threshold bits for overcurrent comparator 0/1	GOCT0[3:0] , GOCT1[3:0]	GOCT0[4:0] , GOCT1[4:0]	GOCT0[4:0], GOCT1[4:0]
VLS level select control bit GVLSLVL	not available	available	available
Current sense amplifier offset	adjustable in 5mV steps	adjustable in 3mV steps	adjustable in 3mV steps

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

It is possible to read from P-Flash memory while some commands are executing on EEPROM memory. It is not possible to read from EEPROM memory while a command is executing on P-Flash memory . Simultaneous P-Flash and EEPROM operations are discussed in Section 20.4.6.

Both P-Flash and EEPROM memories are implemented with Error Correction Codes (ECC) that can resolve single bit faults and detect double bit faults. For P-Flash memory, the ECC implementation requires that programming be done on an aligned 8 byte basis (a Flash phrase). Since P-Flash memory is always read by half-phrase, only one single bit fault in an aligned 4 byte half-phrase containing the byte or word accessed will be corrected.

20.1.1 Glossary

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

EEPROM Memory — The EEPROM memory constitutes the nonvolatile memory store for data.

EEPROM Sector — The EEPROM sector is the smallest portion of the EEPROM memory that can be erased. The EEPROM sector consists of 4 bytes.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes two sets of aligned double words with each set including 7 ECC bits for single bit fault correction and double bit fault detection within each double word.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 512 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Version ID, and the Program Once field.

20.1.2 Features

20.1.2.1 P-Flash Features

- Derivatives featuring up to and including 128 KB of P-Flash include one P-Flash block
- Derivatives featuring more than 128 KB of P-Flash include two Flash blocks

Offset Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	CCIE	0	ERSAREQ	IGNSF	WSTAT[1:0]		FDFD	FSFD
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-9. Flash Configuration Register (FCNFG)

CCIE, IGNSF, WSTAT, FDFD, and FSFD bits are readable and writable, ERSAREQ bit is read only, and remaining bits read 0 and are not writable.

Table 20-14. FCNFG Field Descriptions

Field	Description
7 CCIE	**Command Complete Interrupt Enable** — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 20.3.2.7)
5 ERSAREQ	**Erase All Request** — Requests the Memory Controller to execute the Erase All Blocks command and release security. ERSAREQ is not directly writable but is under indirect user control. Refer to the Reference Manual for assertion of the *soc_erase_all_req* input to the FTMRZ module. 0 No request or request complete 1 Request to: a) run the Erase All Blocks command b) verify the erased state c) program the security byte in the Flash Configuration Field to the unsecure state d) release MCU security by setting the SEC field of the FSEC register to the unsecure state as defined in Table 20-9 of Section 20.3.2.2. The ERSAREQ bit sets to 1 when *soc_erase_all_req* is asserted, CCIF=1 and the Memory Controller starts executing the sequence. ERSAREQ will be reset to 0 by the Memory Controller when the operation is completed (see Section 20.4.7.7.1).
4 IGNSF	**Ignore Single Bit Fault** — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 20.3.2.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
3–2 WSTAT[1:0]	**Wait State control bits** — The WSTAT[1:0] bits define how many wait-states are inserted on each read access to the Flash as shown on Table 20-15.Right after reset the maximum amount of wait-states is set, to be later re-configured by the application if needed. Depending on the system operating frequency being used the number of wait-states can be reduced or disabled, please refer to the Data Sheet for details. For additional information regarding the procedure to change this configuration please see Section 20.4.3. The WSTAT[1:0] bits should not be updated while the Flash is executing a command (CCIF=0); if that happens the value of this field will not change and no action will take place.

Table 20-36. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if an invalid global address [23:0] is supplied see Table 20-3)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

20.4.7.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 20-37. Erase Verify P-Flash Section Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x03	Global address [23:16] of a P-Flash block
FCCOB1	Global address [15:0] of the first phrase to be verified	
FCCOB2	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 20-38. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied see Table 20-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

Table 20-65. Program EEPROM Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the EEPROM block
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.16 Erase EEPROM Sector Command

The Erase EEPROM Sector operation will erase all addresses in a sector of the EEPROM block.

Table 20-66. Erase EEPROM Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x12	Global address [23:16] to identify EEPROM block
FCCOB1	Global address [15:0] anywhere within the sector to be erased. See Section 20.1.2.2 for EEPROM sector size.	

Upon clearing CCIF to launch the Erase EEPROM Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase EEPROM Sector operation has completed.

Table 20-67. Erase EEPROM Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied see Table 20-3
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 22-10. PWMCTL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 CON67	Concatenate Channels 6 and 7 0 Channels 6 and 7 are separate 8-bit PWMs. 1 Channels 6 and 7 are concatenated to create one 16-bit PWM channel. Channel 6 becomes the high order byte and channel 7 becomes the low order byte. Channel 7 output pin is used as the output for this 16-bit PWM (bit 7 of port PWMP). Channel 7 clock select control-bit determines the clock source, channel 7 polarity bit determines the polarity, channel 7 enable bit enables the output and channel 7 center aligned enable bit determines the output mode.
6 CON45	Concatenate Channels 4 and 5 0 Channels 4 and 5 are separate 8-bit PWMs. 1 Channels 4 and 5 are concatenated to create one 16-bit PWM channel. Channel 4 becomes the high order byte and channel 5 becomes the low order byte. Channel 5 output pin is used as the output for this 16-bit PWM (bit 5 of port PWMP). Channel 5 clock select control-bit determines the clock source, channel 5 polarity bit determines the polarity, channel 5 enable bit enables the output and channel 5 center aligned enable bit determines the output mode.
5 CON23	Concatenate Channels 2 and 3 0 Channels 2 and 3 are separate 8-bit PWMs. 1 Channels 2 and 3 are concatenated to create one 16-bit PWM channel. Channel 2 becomes the high order byte and channel 3 becomes the low order byte. Channel 3 output pin is used as the output for this 16-bit PWM (bit 3 of port PWMP). Channel 3 clock select control-bit determines the clock source, channel 3 polarity bit determines the polarity, channel 3 enable bit enables the output and channel 3 center aligned enable bit determines the output mode.
4 CON01	Concatenate Channels 0 and 1 0 Channels 0 and 1 are separate 8-bit PWMs. 1 Channels 0 and 1 are concatenated to create one 16-bit PWM channel. Channel 0 becomes the high order byte and channel 1 becomes the low order byte. Channel 1 output pin is used as the output for this 16-bit PWM (bit 1 of port PWMP). Channel 1 clock select control-bit determines the clock source, channel 1 polarity bit determines the polarity, channel 1 enable bit enables the output and channel 1 center aligned enable bit determines the output mode.
3 PSWAI	PWM Stops in Wait Mode — Enabling this bit allows for lower power consumption in wait mode by disabling the input clock to the prescaler. 0 Allow the clock to the prescaler to continue while in wait mode. 1 Stop the input clock to the prescaler whenever the MCU is in wait mode.
2 PFRZ	**PWM Counters Stop in Freeze Mode** — In freeze mode, there is an option to disable the input clock to the prescaler by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode, the input clock to the prescaler is disabled. This feature is useful during emulation as it allows the PWM function to be suspended. In this way, the counters of the PWM can be stopped while in freeze mode so that once normal program flow is continued, the counters are re-enabled to simulate real-time operations. Since the registers can still be accessed in this mode, to re-enable the prescaler clock, either disable the PFRZ bit or exit freeze mode. 0 Allow PWM to continue while in freeze mode. 1 Disable PWM input clock to the prescaler whenever the part is in freeze mode. This is useful for emulation.

22.3.2.7 PWM Clock A/B Select Register (PWMCLKAB)

Each PWM channel has a choice of four clocks to use as the clock source for that channel as described below.

Table A-10. 64LQFP-EP Typical Thermal Package Characteristics (All other devices)

Num	C[1]	Rating	Symbol	masksets 1N95G, 2N95G	maskset 3N95G	Unit
1		Thermal resistance 64LQFP-EP, single sided PCB[2] Natural Convection	θ_{JA}	69	58	°C/W
2		Thermal resistance 64LQFP-EP, double sided PCB[2] with 2 internal planes. Natural Convection.	θ_{JA}	31	28	°C/W
3		Thermal resistance 64LQFP-EP, single sided PCB[3] (@200 ft./min)	θ_{JA}	56	46	°C/W
4		Thermal resistance 64LQFP-EP, double sided PCB[3] with 2 internal planes (@200 ft./min).	θ_{JA}	26	22	°C/W
5		Junction to Board 64LQFP-EP[4]	θ_{JB}	15	11	°C/W
6		Junction to Case Top 64LQFP-EP[5]	θ_{JCtop}	18	14	°C/W
7		Junction to Case Bottom 64LQFP-EP[6]	$\theta_{JCbottom}$	1.7	1.4	°C/W
8		Junction to Package Top 64LQFP-EP[7]	Ψ_{JT}	4	3	°C/W

1. The values for thermal resistance are achieved by package simulations
2. Junction to ambient thermal resistance. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively
3. Junction to ambient thermal resistance. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. A single layer board is used for this simulation.

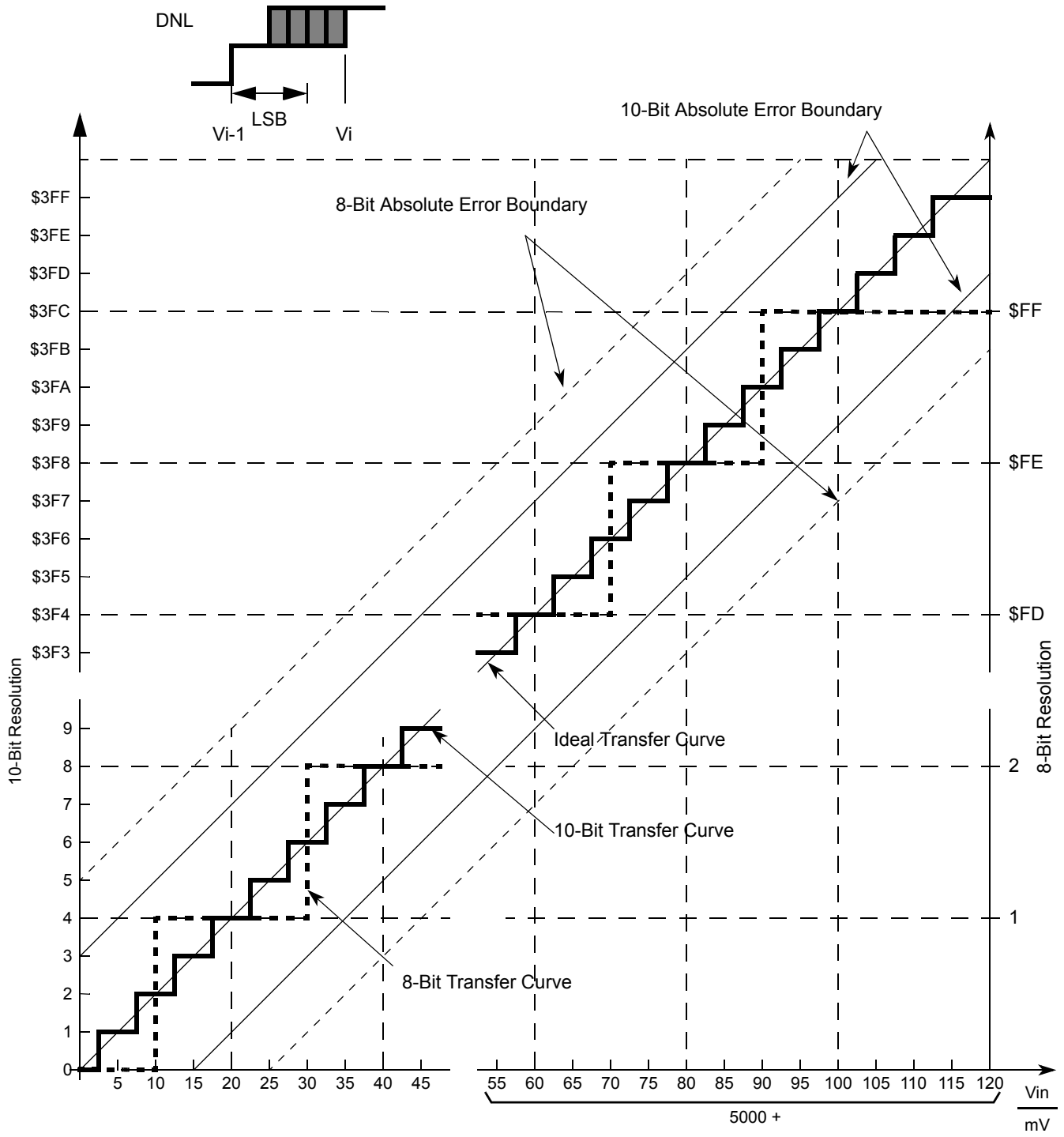


Figure C-2. ADC Accuracy Definitions