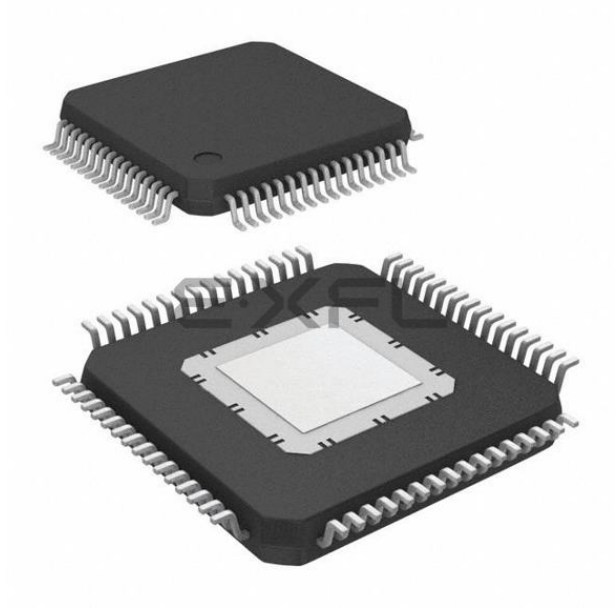

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Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f2wkhr

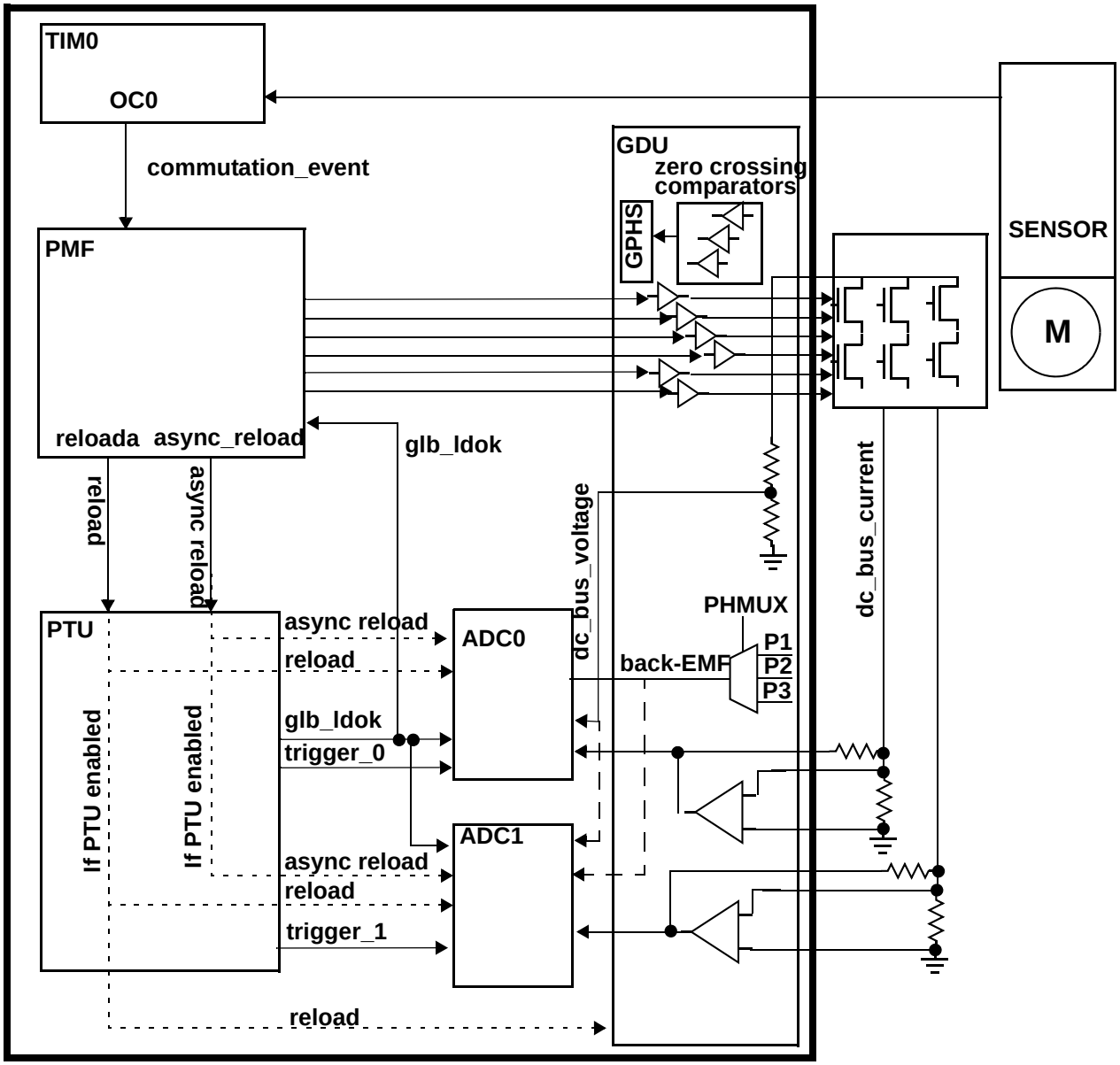
Table 1-8. Pin Summary For 64-Pin and 48-Pin Package Options (Sheet 2 of 4)

LQFP Option				Function (Priority and device dependencies specified in PIM chapter)					Power Supply	Internal Pull Resistor	
64 M/ ML	64 MC	48	Pin	1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
20	20	16	VDD	—	—	—	—	—	V_{DD}	—	—
21	21	17	PAD0	KWAD0	AN0_0	AMP0	—	—	V_{DDA}	PERADL /PPSADL	Off
22	22	18	PAD1	KWAD1	AN0_1	AMPM0	—	—	V_{DDA}	PERADL /PPSADL	Off
23	23	19	PAD2	KWAD2	AN0_2	AMPP0	—	—	V_{DDA}	PERADL /PPSADL	Off
24	24	—	PAD3	KWAD3	AN0_3	—	—	—	V_{DDA}	PERADL /PPSADL	Off
25	25	—	PAD4	KWAD4	AN0_4	—	—	—	V_{DDA}	PERADL /PPSADL	Off
26	26	—	PAD5	KWAD5	AN1_0	AMP1	—	—	V_{DDA}	PERADL /PPSADL	Off
27	27	—	PAD6	KWAD6	AN1_1	AMPM1	SS0	—	V_{DDA}	PERADL /PPSADL	Off
28	28	—	PAD7	KWAD7	AN1_2	AMPP1	—	—	V_{DDA}	PERADL /PPSADL	Off
29	29	20	PAD8	KWAD8	AN1_3	VRH0_0	VRH1_0	—	V_{DDA}	PERADH/PPSADH	Off
30	30	21	VDDA	VRH0_1	VRH1_1	—	—	—	V_{DDA}	—	—
31	31	22	VSSA	VRL0_ [1:0]	VRL1_ [1:0]	—	—	—	V_{DDA}	—	—
32	32	23	LS0	—	—	—	—	—	—	—	—
33	33	24	LG0	—	—	—	—	—	—	—	—
34	34	—	VLS0	—	—	—	—	—	—	—	—
35	35	25	VBS0	—	—	—	—	—	—	—	—

1.13.3.1 Motor Control Loop Overview

The mapping of motor control events at device level as depicted in Figure 1-9 is listed in Table 1-21, whereby the columns list the names used in the module level descriptions

Figure 1-9. Internal Control Loop Configuration



The control loop consists of the PMF, GDU, ADC and PTU modules. The control loop operates using either static, dynamic or asynchronous timing. In the following text the event names given in **bold type** correspond to those shown in Figure 1-9. The PTU and ADC operate using lists stored in memory. These lists define trigger points for the PTU, commands for the ADC and results from the ADC. If the PTU is enabled the reload and async_reload events are immediately passed through to the ADC and GDU modules.

2.3.4.3 Port P Interrupt Flag Register (PIFP)

Address 0x02F7 PIFP Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIF1	0	0	0	0	PIFP2	PIFP1	PIFP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-25. Port P Interrupt Flag Register

1. Read: Anytime
   Write: Anytime, write 1 to clear

Table 2-29. Port P Interrupt Flag Register Field Descriptions

Field	Description
7 OCIF1	**Over-Current Interrupt Flag register —** This flag asserts if an over-current condition is detected on PP0 (Section 2.4.5, “Over-Current Interrupt”). Writing a logic “1” to the corresponding bit field clears the flag. 1 PP0 Over-current event occurred 0 No PP0 over-current event occurred
2-0 PIFP2-0	**See Section 2.3.3.7, “Port Interrupt Flag Register”**

Chapter 5
Background Debug Controller (S12ZBDCV2)

Table 5-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V2.04	03.Dec.2012	Section 5.1.3.3	Included BACKGROUND/ Stop mode dependency
V2.05	22.Jan.2013	Section 5.3.2.2	Improved NORESP description and added STEP1/ Wait mode dependency
V2.06	22.Mar.2013	Section 5.3.2.2	Improved NORESP description of STEP1/ Wait mode dependency
V2.07	11.Apr.2013	Section 5.1.3.3.1	Improved STOP and BACKGROUND interdepency description
V2.08	31.May.2013	Section 5.4.4.4 Section 5.4.7.1	Removed misleading WAIT and BACKGROUND interdepency description Added subsection dedicated to Long-ACK
V2.09	29.Aug.2013	Section 5.4.4.12	Noted that READ_DBGTB is only available for devices featuring a trace buffer.
V2.10	21.Oct.2013	Section 5.1.3.3.2	Improved description of NORESP dependence on WAIT and BACKROUND
V2.11	02.Feb.2015	Section 5.1.3.3.1 Section 5.3.2	Corrected name of clock that can stay active in Stop mode

5.1 Introduction

The background debug controller (BDC) is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC.

The S12ZBDC maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface.

5.1.1 Glossary

Table 5-2. Glossary Of Terms

Term	Definition
DBG	On chip Debug Module
BDM	Active Background Debug Mode
CPU	S12Z CPU
SSC	Special Single Chip Mode (device operating mode
NSC	Normal Single Chip Mode (device operating mode)
BDCSI	Background Debug Controller Serial Interface. This refers to the single pin BKGD serial interface.
EWAIT	Optional S12 feature which allows external devices to delay external accesses until deassertion of EWAIT

9.5.2.2 ADC Control Register 1 (ADCCTL_1)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-5. ADC Control Register 1 (ADCCTL_1)

Read: Anytime

Write:

- Bit CSL_BMOD and RVL_BMOD writable if bit ADC_EN clear or bit SMOD_ACC set
- Bit SMOD_ACC only writable in MCU Special Mode
- Bit AUT_RSTA writable anytime

Table 9-5. ADCCTL_1 Field Descriptions

Field	Description
7 CSL_BMOD	CSL Buffer Mode Select Bit — This bit defines the CSL buffer mode. This bit is only writable if ADC_EN is clear. 0 CSL single buffer mode. 1 CSL double buffer mode.
6 RVL_BMOD	RVL Buffer Mode Select Bit — This bit defines the RVL buffer mode. 0 RVL single buffer mode 1 RVL double buffer mode
5 SMOD_ACC	Special Mode Access Control Bit — This bit controls register access rights in MCU Special Mode. This bit is automatically cleared when leaving MCU Special Mode. Note: When this bit is set also the ADCCMD register is writeable via the data bus to allow modification of the current command for debugging purpose. But this is only possible if the current command is not already processed (conversion not started). Please see access details given for each register. Care must be taken when modifying ADC registers while bit SMOD_ACC is set to not corrupt a possible ongoing conversion. 0 Normal user access - Register write restrictions exist as specified for each bit. 1 Special access - Register write restrictions are lifted.
4 AUT_RSTA	**Automatic Restart Event after exit from MCU Stop and Wait Mode (SWAI set)** — This bit controls if a Restart Event is automatically generated after exit from MCU Stop Mode or Wait Mode with bit SWAI set. It can be configured for ADC conversion flow control mode “Trigger Mode” and “Restart Mode” (anytime during application runtime). 0 No automatic Restart Event after exit from MCU Stop Mode. 1 Automatic Restart Event occurs after exit from MCU Stop Mode.

9.8.3 ADC Error and Conversion Flow Control Issue Interrupt

The ADC provides one error interrupt for four error classes related to conversion interrupt overflow, command validness, DMA access status and Conversion Flow Control issues, and CSL failure. The following error interrupt flags belong to the group of severe issues which cause an error interrupt if enabled and cease ADC operation:

- IA_EIF
- CMD_EIF
- EOL_EIF
- TRIG_EIF

In order to make the ADC operational again, an ADC Soft-Reset must be issued which clears the above listed error interrupt flags.

NOTE

It is important to note that if flag DBECC_ERR is set, the ADC ceases operation as well, but does not cause an ADC error interrupt. Instead, a machine exception is issued. In order to make the ADC operational again an ADC Soft-Reset must be issued.

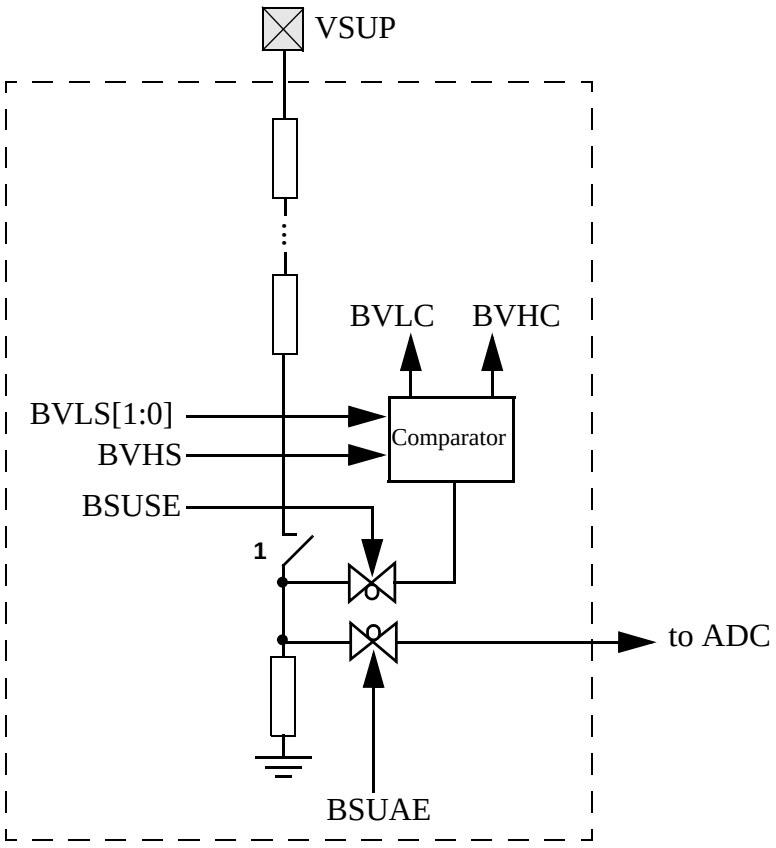
Remaining error interrupt flags cause an error interrupt if enabled, but ADC continues operation. The related interrupt flags are:

- RSTAR_EIF
- LDOK_EIF
- CONIF_OIF

10.1.3 Block Diagram

Figure 10-1 shows a block diagram of the BATS module. See device guide for connectivity to ADC channel.

Figure 10-1. BATS Block Diagram



1 automatically closed if BSUSE and/or BSUAE is active, open during Stop mode

10.2 External Signal Description

This section lists the name and description of all external ports.

10.2.1 VSUP — Voltage Supply Pin

This pin is the chip supply. It can be internally connected for voltage measurement. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC or to a comparator.

Module Base + 0x000A — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TX2	TX1	TX0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-14. MSCAN Transmit Buffer Selection Register (CANTBSEL)

1. Read: Find the lowest ordered bit set to 1, all other bits will be read as 0
   Write: Anytime when not in initialization mode

NOTE

The CANTBSEL register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK=1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-16. CANTBSEL Register Field Descriptions

Field	Description
2-0 TX[2:0]	**Transmit Buffer Select** — The lowest numbered bit places the respective transmit buffer in the CANTXFG register space (e.g., TX1 = 1 and TX0 = 1 selects transmit buffer TX0; TX1 = 1 and TX0 = 0 selects transmit buffer TX1). Read and write accesses to the selected transmit buffer will be blocked, if the corresponding TXEx bit is cleared and the buffer is scheduled for transmission (see Section 13.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”). 0 The associated message buffer is deselected 1 The associated message buffer is selected, if lowest numbered bit

The following gives a short programming example of the usage of the CANTBSEL register:

To get the next available transmit buffer, application software must read the CANTFLG register and write this value back into the CANTBSEL register. In this example Tx buffers TX1 and TX2 are available. The value read from CANTFLG is therefore 0b0000_0110. When writing this value back to CANTBSEL, the Tx buffer TX1 is selected in the CANTXFG because the lowest numbered bit set to 1 is at bit position 1. Reading back this value out of CANTBSEL results in 0b0000_0010, because only the lowest numbered bit position set to 1 is presented. This mechanism eases the application software’s selection of the next available Tx buffer.

- LDAA CANTFLG; value read is 0b0000_0110
- STAA CANTBSEL; value written is 0b0000_0110
- LDAA CANTBSEL; value read is 0b0000_0010

If all transmit message buffers are deselected, no accesses are allowed to the CANTXFG registers.

13.3.2.12 MSCAN Identifier Acceptance Control Register (CANIDAC)

The CANIDAC register is used for identifier acceptance control as described below.

14.3.2.11 Trigger Generator 1 Trigger Number Register (TG1TNUM)

Module Base + 0x000B — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	TG1TNUM[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-13. Trigger Generator 1 Trigger Number Register (TG1TNUM)

1. Read: Anytime
   Write: Never

Table 14-13. TG1TNUM Register Field Descriptions

Field	Description
4:0 TG1TNUM[4:0]	Trigger Generator 1 Trigger Number — This register shows the number of generated triggers since the last reload event. After the generation of 32 triggers this register shows zero. The next reload event clears this register. See also Figure 14-22.

14.3.2.12 Trigger Generator 1 Trigger Value (TG1TVH, TG1TVL)

Module Base + 0x000C — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	TG1TV[15:8]							
W								
Reset	0	0	0	0	0	0	0	0

Module Base + 0x000D — Access: User read only

	7	6	5	4	3	2	1	0
R	TG1TV[7:0]							
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-14. Trigger Generator 1 Trigger Value Register (TG1TVH, TG1TVL)

1. Read: Anytime
   Write: Never

14.3.2.18 PTU Debug Register (PTUDEBUG)

Module Base + 0x001F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	PTUREPE	PTUT1PE	PTUT0PE	0	0	0	0
W						PTUFRE	TG1FTE	TG0FTE
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-21. PTU Debug Register (PTUDEBUG)

1. Read: Anytime
   Write: only in special mode

Table 14-21. PTUDEBUG Register Field Descriptions

Field	Description
6 PTUREPE	**PTURE Pin Enable** — This bit enables the output port for pin PTURE. 0 PTURE output port are disabled 1 PTURE output port are enabled
5 PTUT1PE	**PTU PTUT1 Pin Enable** — This bit enables the output port for pin PTUT1. 0 PTUT1 output port are disabled 1 PTUT1 output port are enabled
4 PTUT0PE	**PTU PTUT0 Pin Enable** — This bit enables the output port for pin PTUT0. 0 PTUT0 output port are disabled 1 PTUT0 output port are enabled
2 PTUFRE	Force Reload event generation — If one of the TGs is enabled then writing 1 to this bit will generate a reload event. The reload event forced by PTUFRE does not set the PTUROIF interrupt flag. Also the ptu_reload signal asserts for one bus clock cyclet. Writing 0 to this bit has no effect. Always reads back as 0. This behavior is not available during stop or freeze mode.
1 TG1FTE	**Trigger Generator 1 Force Trigger Event** — If TG1 is enabled then writing 1 to this bit will generate a trigger event independent on the list based trigger generation. Writing 0 to this bit has no effect. Always reads back as 0.This behavior is not available during stop or freeze mode.
0 TG0FTE	**Trigger Generator 0 Force Trigger Event** — If TG0 is enabled then writing 1 to this bit will generate a trigger event independent on the list based trigger generation. Writing 0 to this bit has no effect. Always reads back as 0. This behavior is not available during stop or freeze mode.

14.4 Functional Description

14.4.1 General

The PTU module consists of two trigger generators (TG0 and TG1). For each TG a separate enable bit is available, so that both TGs can be enabled independently.

If both trigger generators are disabled then the PTU is disabled, the trigger generation stops and the memory accesses are disabled.

15.3.2.31 PMF Counter C Register (PMFCNTC)

Address: Module Base + 0x0032 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFCNTC														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-36. PMF Counter C Register (PMFCNTC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Never

This register displays the state of the 15-bit PWM C counter.

15.3.2.32 PMF Counter Modulo C Register (PMFMODC)

Address: Module Base + 0x0034 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFMODC														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-37. PMF Counter Modulo C Register (PMFMODC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKC bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODC returns the value in the buffer. It is not necessarily the value the PWM generator A is currently using.

15.3.2.33 PMF Deadtime C Register (PMFDTMC)

Address: Module Base + 0x0036 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PMFDTMC											
W																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Figure 15-38. PMF Deadtime C Register (PMFDTMC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set.This register cannot be modified after the WP bit is set.

15.4.12.6 Synchronization Output (pmf_reload)

The PMF uses reload events to output a synchronization pulse, which can be used as an input to the timer module. A high-true pulse occurs for each PWM cycle start of the PWM, regardless of the state of the related LDOK bit or global load OK and load frequency.

15.4.13 Fault Protection

Fault protection can disable any combination of PWM outputs (for all FAULT0-5 inputs) or switch to output control register PMFOUTF on a fault event (for FAULT4-5 only). Faults are generated by an active level[1] on any of the FAULT inputs. Each FAULT input can be mapped arbitrarily to any of the PWM outputs.

In complementary mode, if a FAULT4 or FAULT5 event is programmed to switch to output control on a fault event resulting in a PWM active state on a particular output, then the transition will take place after deadtime insertion. Thus an asynchronous path to disable the PWM output is not available.

On a fault event the PWM generator continues to run.

The fault decoder affects the PWM outputs selected by the fault logic and the disable mapping register.

The fault protection is enabled even when the PWM is not enabled; therefore, a fault will be latched in and will be cleared in order to prevent an interrupt when the PWM is enabled.

15.4.13.1 Fault Input Sample Filter

Each fault input has a sample filter to test for fault conditions. After every bus cycle setting the FAULT*m* input at logic zero, the filter synchronously samples the input once every four bus cycles. QSMP determines the number of consecutive samples that must be logic one for a fault to be detected. When a fault is detected, the corresponding FAULT*m* flag, FIF*m*, is set. FIF*m* can only be cleared by writing a logic one to it.

If the FIE*m*, FAULT*m* interrupt enable bit is set, the FIF*m* flag generates a CPU interrupt request. The interrupt request latch remains set until:

- Software clears the FIF*m* flag by writing a logic one to it
- Software clears the FIE*m* bit by writing a logic zero to it
- A reset occurs

15.4.13.2 Automatic Fault Recovery

Setting a fault mode bit, FMOD*m*, configures faults from the FAULT*m* input for automatically reenabling the PWM outputs.

When FMOD*m* is set, disabled PWM outputs are enabled when the FAULT*m* input returns to logic zero and a new PWM half cycle begins. See Figure 15-83. Clearing the FIF*m* flag does not affect disabled PWM outputs when FMOD*m* is set.

1. The active input level may be defined or programmable at SoC level. The default for internally connected resources is active-high. For availability and configurability of fault inputs on pins refer to the device overview section.

Table 15-46. Effects of OUTCTL and OUT Bits on PWM Output Pair in Complementary Mode

OUTCTL (odd,even)	OUT (odd,even)	PWM (odd)	PWM (even)
00	xx	PWMgen(even)	PWMgen(even)
11	10	$\overline{\text{OUTB(even)}}$=1	OUTB(even)=0
01	x0	0	OUTB(even)=0

The recommended setup is:

```
PMFCFG0[INDEPC,INDEPB,INDEPA] = 0x0;   // Complementary mode
PMFCFG1[ENCE]                 = 1;     // Enable commutation event
PMFOUTB = 0x2A;                        // Set return path pattern, high-side off, low-side on
PMFOUTC = 0x1C;                        // Branch A->B, "mask" C // 0°
```

The commutation sequence is:

```
PMFOUTC = 0x34;                        // Branch A->C, "mask" B // 60°
PMFOUTC = 0x31;                        // Branch B->C, "mask" A // 120°
PMFOUTC = 0x13;                        // Branch B->A, "mask" C // 180°
PMFOUTC = 0x07;                        // Branch C->A, "mask" B // 240°
PMFOUTC = 0x0D;                        // Branch C->B, "mask" A // 300°
PMFOUTC = 0x1C;                        // Branch A->B, "mask" C // 360°
```

Table 15-47. Unipolar Switching Sequence

Branch	Channel	0°	60°	120°	180°	240°	300°
A	PWM0	PWMgen		0	0		0
	PWM1	PWMgen		0	1		0
B	PWM2	0	0	PWMgen		0	0
	PWM3	1	0	PWMgen		0	1
C	PWM4	0	0		0	PWMgen	
	PWM5	0	1		0	PWMgen	

15.8.2.2 Bipolar Switching Mode

Bipolar switching mode uses register bits MSK5-0 and PINVA, B, C to perform commutation.

The recommended setup is:

```
PMFCFG0[INDEPC,INDEPB,INDEPA] = 0x0;  // Complementary mode
PMFCFG1[ENCE]                 = 1;    // Enable commutation event
PMFCFG2[MSK5:MSK0]            = 0x30; // Branch A<->B, mask C // 0°
PMFCFG3[PINVC,PINVB,PINVA]    = 0x2;  // Invert B
```

The commutation sequence is:

```
PMFCFG2[MSK5:MSK0]            = 0x03; // Branch C<->B, mask A // 60°
PMFCFG3[PINVC,PINVB,PINVA]    = 0x2;  // Invert B
```

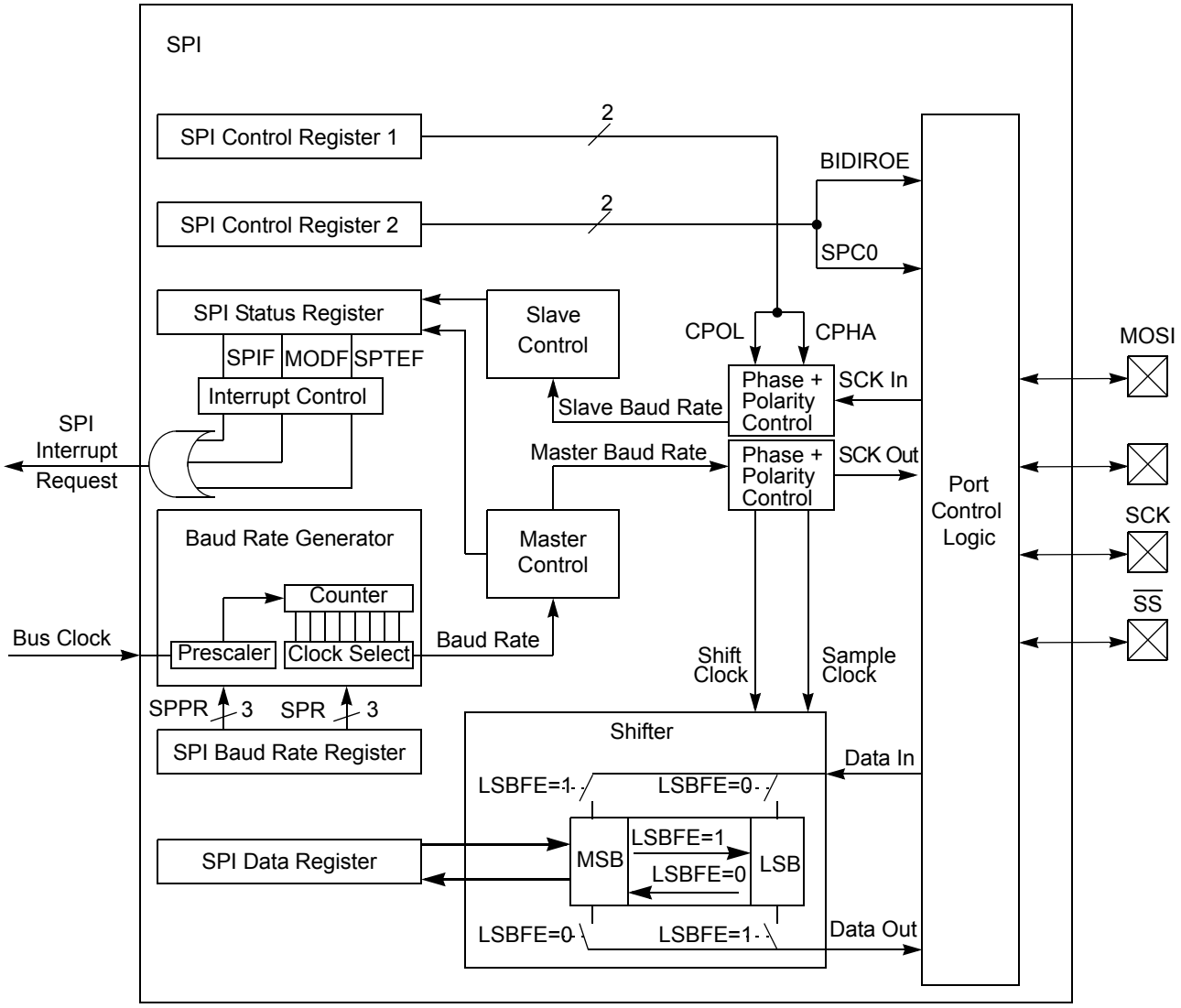


Figure 17-1. SPI Block Diagram

17.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

17.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

Table 18-2. GDUV4/V5/V6 Differences(1)

Feature	GDU V4	GDU V5	GDU V6
On chip bootstrap diode	not available, off chip bootstrap diode required	available	not available, off chip bootstrap diode required
Desaturation filter bits GDSFLS/GDSFHS	not available	available	available
Fault[3] output to PMF	driven by GLVLSIF	driven by GLVLSF	driven by GLVLSF
Fault[4] output to PMF	driven by GHHDIF	driven by GHHDF	driven by GHHDF
Low-side drivers on or off out of reset dependent on NVM option	available[1.]	available[1.]	available
additional drain connections LD[2:0] to external low-side power FETs	not available	not available	available
Control bits GSRMOD1/0 for SR motor drive	not available	not available	available

1. Refer to device overview for mask set / GDU version info.

The GDU module is a Field Effect Transistor (FET) pre-driver designed for three phase motor control applications.

18.1.1 Features

The GDU module includes these distinctive features:

- 11V voltage regulator for FET pre-drivers
- Boost converter option for low supply voltage condition
- 3-phase bridge FET pre-drivers
- Bootstrap circuit for high-side FET pre-drivers with external bootstrap capacitor
- Charge pump for static high-side driver operation
- Phase voltage measurement with internal ADC
- Two low-side current measurement amplifiers for DC phase current measurement
- Phase comparators for BEMF zero crossing detection in sensorless BLDC applications
- Voltage measurement on HD pin (DC-Link voltage) with internal ADC
- Desaturation comparator for high-side drivers and low-side drivers protection
- Undervoltage detection on FET pre-driver supply pin VLS
- Two overcurrent comparators with programmable voltage threshold
- Overvoltage detection on 3-phase bridge supply HD pin

Table 18-18. Charge Pump Clock Divider Factors k = f_{BUS} / f_{CP}

GCPCD[3:0]	f_{CP}
0000	f_{BUS} / 16
0001	f_{BUS} / 24
0010	f_{BUS} / 32
0011	f_{BUS} / 48
0100	f_{BUS} / 64
0101	f_{BUS} / 96
0110	f_{BUS} / 100
0111	f_{BUS} / 128
1000	f_{BUS} / 192
1001	f_{BUS} / 200
1010	f_{BUS} / 256
1011	f_{BUS} / 384
1100	f_{BUS} / 400
1101	f_{BUS} / 512
1110	f_{BUS} / 768
1111	f_{BUS} / 800

Figure 18-25. Short to Supply Detection

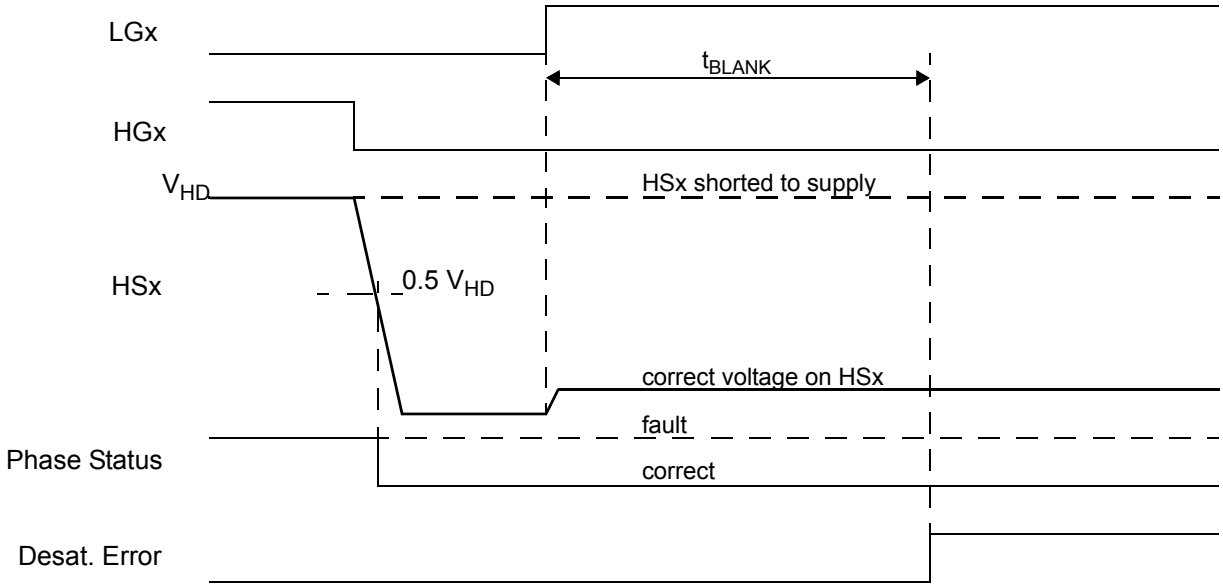


Figure 18-26. Short to Ground Detection

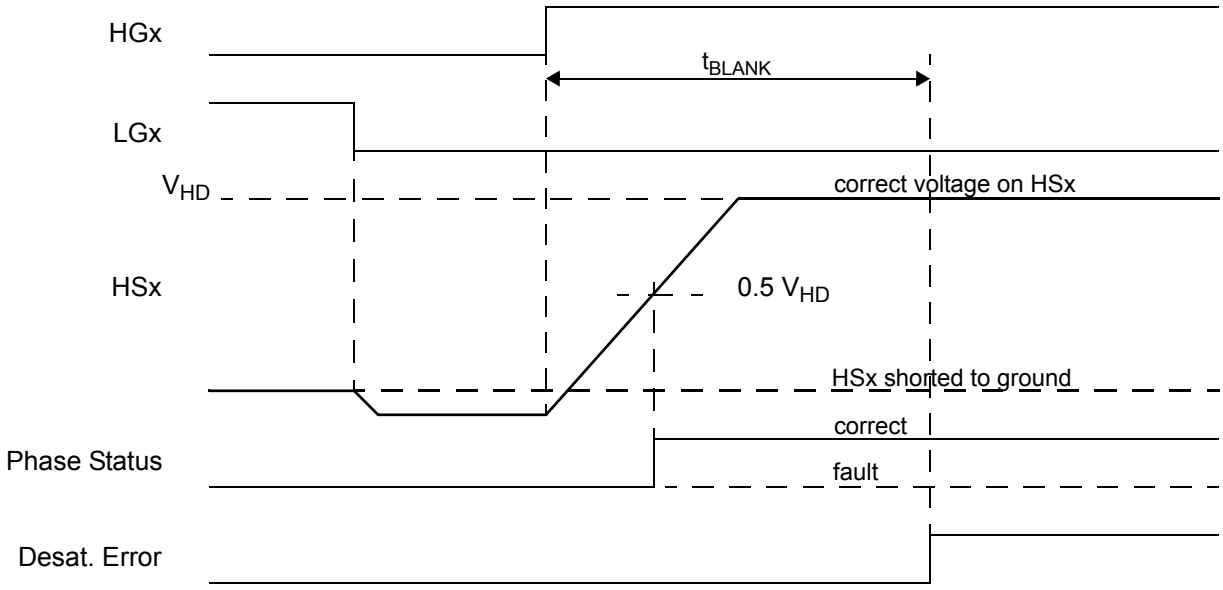


Table 20-43. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters
FCCOB3	Program Once word 1 value
FCCOB4	Program Once word 2 value
FCCOB5	Program Once word 3 value

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Table 20-44. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed(1)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1. If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

20.4.7.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and EEPROM memory space.

Table 20-45. Erase All Blocks Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 22.4.2.5, “Left Aligned Outputs” and Section 22.4.2.6, “Center Aligned Outputs” for more details).

Table 22-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

22.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 22-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 22-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 22.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

Table H-3. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 175°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
7	Non-Differential Slew Rate (CANL or CANH) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	 t_{SL6} t_{SL5} t_{SL4} t_{SL2} t_{SL1} t_{SL0}	—	 6 10 19 23 35 55	—	V/µs
8	Bus Communication Rate	t_{BUS}	—	—	1.0 M	bps
9	Settling time after entering Normal mode	t_{CP_set}	—	—	10	µs
10	CPTXD-dominant timeout	$t_{CPTXDDT}$	—	2	—	ms
11	CANPHY wake-up dominant pulse filtered	t_{CPWUP}	—	—	1.5	µs
12	CANPHY wake-up dominant pulse pass	t_{CPWUP}	5	—	—	µs