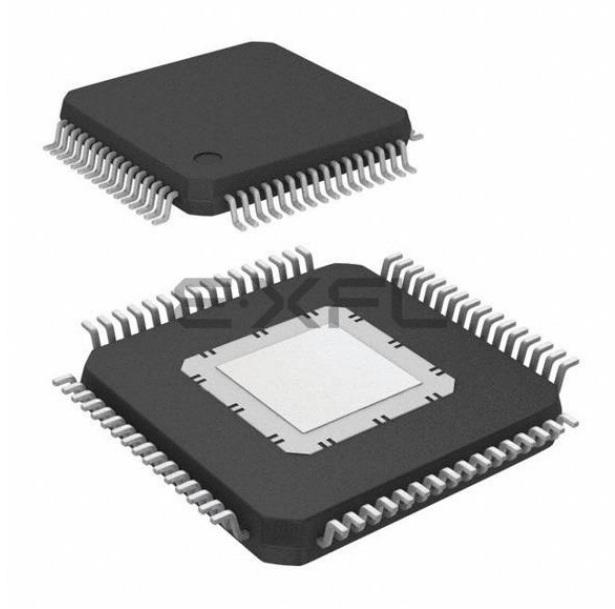

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f3mkhr

Chapter 10
Supply Voltage Sensor - (BATSV3)

- When a reset occurs the debugger pulls BKGD low until the reset ends, forcing SSC mode entry.
- Then the debugger reads the reset flags to determine the cause of reset.
- If required, the debugger can read the trace buffer to see what happened just before reset. Since the trace buffer and DBGCNT register are not affected by resets other than POR.
- The debugger configures and arms the DBG to start tracing on returning to application code.
- The debugger then sets the PC according to the reset flags.
- Then the debugger returns to user code with GO or STEP1.

6.5.3 Breakpoints from other S12Z sources

The DBG is neither affected by CPU BGND instructions, nor by BDC BACKGROUND commands.

6.5.4 Code Profiling

The code profiling data output pin PDO is mapped to a device pin that can also be used as GPIO in an application. If profiling is required and all pins are required in the application, it is recommended to use the device pin for a simple output function in the application, without feedback to the chip. In this way the application can still be profiled, since the pin has no effect on code flow.

The PDO provides a simple bit stream that must be strobed at both edges of the profiling clock when profiling. The external development tool activates profiling by setting the DBG ARM bit, with PROFILE and PDOE already set. Thereafter the first bit of the profiling bit stream is valid at the first rising edge of the profiling clock. No start bit is provided. The external development tool must detect this first rising edge after arming the DBG. To detect the end of profiling, the DBG ARM bit can be monitored using the BDC.

8.3.2.10 S12CPMU_UHV_V10_V6 PLL Control Register (CPMUPLL)

This register controls the PLL functionality.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	FM1	FM0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 8-15. S12CPMU_UHV_V10_V6 PLL Control Register (CPMUPLL)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

NOTE

Care should be taken to ensure that the bus frequency does not exceed the specified maximum when frequency modulation is enabled.

Table 8-9. CPMUPLL Field Descriptions

Field	Description
5, 4 FM1, FM0	PLL **Frequency Modulation Enable Bits** — FM1 and FM0 enable frequency modulation on the VCOCLK. This is to reduce noise emission. The modulation frequency is f_{ref} divided by 16. See Table 8-10 for coding.

Table 8-10. FM Amplitude selection

FM1	FM0	FM Amplitude / f_{VCO} Variation
0	0	FM off
0	1	±1%
1	0	±2%
1	1	±4%

The procedure to change APICLK or APIR[15:0] is first to clear APIFE, then write to APICLK or APIR[15:0], and afterwards set APIFE.

The API Trimming bits ACLKTR[5:0] must be set so the minimum period equals 0.2 ms if stable frequency is desired.

See Table 8-21 for the trimming effect of ACLKTR[5:0].

NOTE

The first period after enabling the counter by APIFE might be reduced by API start up delay t_{sdel}.

It is possible to generate with the API a waveform at the external pin API_EXTCLK by setting APIFE and enabling the external access with setting APIEA.

8.7 Initialization/Application Information

8.7.1 General Initialization Information

Usually applications run in MCU Normal Mode.

It is recommended to write the CPMUCOP register in any case from the application program initialization routine after reset no matter if the COP is used in the application or not, even if a configuration is loaded via the flash memory after reset. By doing a “controlled” write access in MCU Normal Mode (with the right value for the application) the write once for the COP configuration bits (WCOP,CR[2:0]) takes place which protects these bits from further accidental change. In case of a program sequencing issue (code runaway) the COP configuration can not be accidentally modified anymore.

8.7.2 Application information for COP and API usage

In many applications the COP is used to check that the program is running and sequencing properly. Often the COP is kept running during Stop Mode and periodic wake-up events are needed to service the COP on time and maybe to check the system status.

For such an application it is recommended to use the ACLK as clock source for both COP and API. This guarantees lowest possible IDD current during Stop Mode. Additionally it eases software implementation using the same clock source for both, COP and API.

The Interrupt Service Routine (ISR) of the Autonomous Periodic Interrupt API should contain the write instruction to the CPMUARMCOP register. The value (byte) written is derived from the “main routine” (alternating sequence of $55 and $AA) of the application software.

Using this method, then in the case of a runtime or program sequencing issue the application “main routine” is not executed properly anymore and the alternating values are not provided properly. Hence the COP is written at the correct time (due to independent API interrupt request) but the wrong value is written (alternating sequence of $55 and $AA is no longer maintained) which causes a COP reset.

If the COP is stopped during any Stop Mode it is recommended to service the COP shortly before Stop Mode is entered.

9.9.3 List Usage — CSL double buffer mode and RVL double buffer mode

In this use case both list types are configured for double buffer mode (CSL_BMOD=1’b1 and RVL_BMOD=1’b1) and whenever a Command Sequence List (CSL) is finished or aborted the command Sequence List is swapped by the simultaneous assertion of bits LDOK and RSTA.

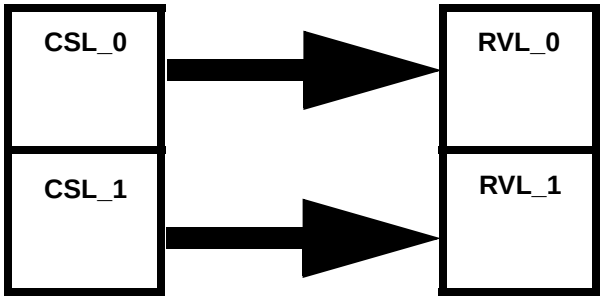


Figure 9-37. CSL Double Buffer Mode — RVL Double Buffer Mode Diagram

This use case can be used if the channel order or CSL length varies very frequently in an application.

9.9.4 List Usage — CSL double buffer mode and RVL single buffer mode

In this use case the CSL is configured for double buffer mode (CSL_BMOD=1’b1) and the RVL is configured for single buffer mode (RVL_BMOD=1’b0).

The two command lists can be different sizes and the allocated result list memory area in the RAM must be able to hold as many entries as the larger of the two command lists. Each time when the end of a Command Sequence List is reached, if bits LDOK and RSTA are set, the commands list is swapped.

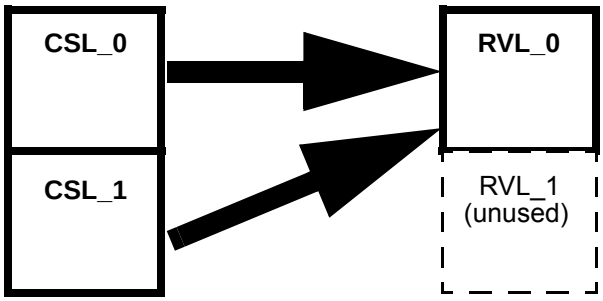


Figure 9-38. CSL Double Buffer Mode — RVL Single Buffer Mode Diagram

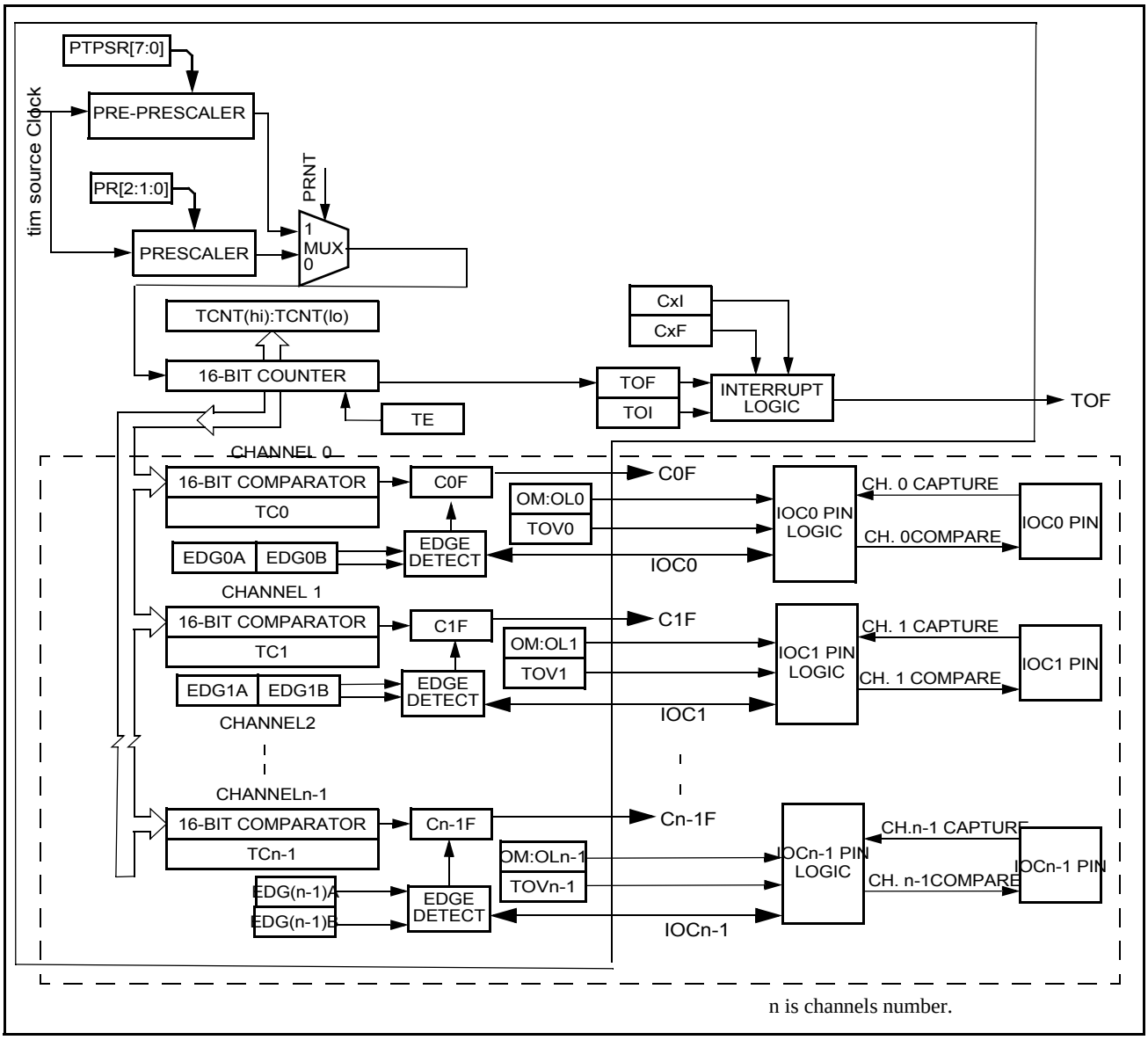


Figure 12-22. Detailed Timer Block Diagram

12.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

13.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
W								
Reset:	0	0	0	1	0	0	0	1

= Unimplemented

Figure 13-5. MSCAN Control Register 1 (CANCTL1)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-3. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 13.4.3.2, “Clock System,” and Section Figure 13-43., “MSCAN Clocking Scheme,”). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 13.4.4.4, “Listen-Only Mode”). In addition, the error counters are frozen. Listen only mode supports applications which require “hot plugging” or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
3 BORM	**Bus-Off Recovery Mode** — This bit configures the bus-off state recovery mode of the MSCAN. Refer to Section 13.5.2, “Bus-Off Recovery,” for details. 0 Automatic bus-off recovery (see Bosch CAN 2.0A/B protocol specification) 1 Bus-off recovery upon user request

Table 14-6. PTUIEL Register Field Descriptions

Field	Description
5 TG1TEIE	Trigger Generator 1 Timing Error Interrupt Enable — Enables trigger generator timing error interrupt. 0 No interrupt will be requested whenever TG1TEIF is set 1 Interrupt will be requested whenever TG1TEIF is set
4 TG1DIE	Trigger Generator 1 Done Interrupt Enable — Enables trigger generator done interrupt. 0 No interrupt will be requested whenever TG1DIF is set 1 Interrupt will be requested whenever TG1DIF is set
3 TG0AEIE	Trigger Generator 0 Memory Access Error Interrupt Enable — Enables trigger generator memory access error interrupt. 0 No interrupt will be requested whenever TG0AEIF is set 1 Interrupt will be requested whenever TG0AEIF is set
2 TG0REIE	Trigger Generator 0 Reload Error Interrupt Enable — Enables trigger generator reload error interrupt. 0 No interrupt will be requested whenever TG0REIF is set 1 Interrupt will be requested whenever TG0REIF is set
1 TG0TEIE	Trigger Generator 0 Timing Error Interrupt Enable — Enables trigger generator timing error interrupt. 0 No interrupt will be requested whenever TG0TEIF is set 1 Interrupt will be requested whenever TG0TEIF is set
0 TG0DIE	Trigger Generator 0 Done Interrupt Enable — Enables trigger generator done interrupt. 0 No interrupt will be requested whenever TG0DIF is set 1 Interrupt will be requested whenever TG0DIF is set

To generate a reload event or trigger event independent from the PWM status the debug register bits PTUFRE or TGxFTE can be used. A write one to this bits will generate the associated event.This behavior is not available during stop or freeze mode.

15.3.2.22 PMF Counter Modulo A Register (PMFMODA)

Address: Module Base + 0x0024 Access: User read/write(1)

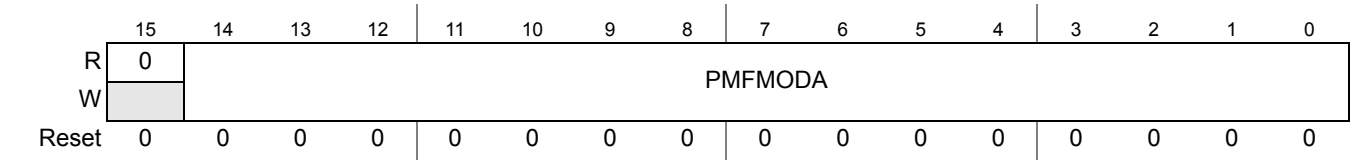


Figure 15-27. PMF Counter Modulo A Register (PMFMODA)

1. Read: Anytime
   Write: Anytime. Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKA bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODA returns the value in the buffer. It is not necessarily the value the PWM generator A is currently using.

15.3.2.23 PMF Deadtime A Register (PMFDTMA)

Address: Module Base + 0x0026 Access: User read/write(1)

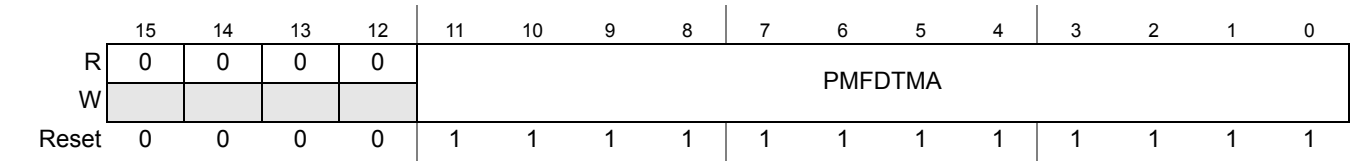


Figure 15-28. PMF Deadtime A Register (PMFDTMA)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to the maximum value of 0x0FFF, selecting a deadtime of 4095 PWM clock cycles. Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows:

$$T_{DEAD\_A} = PMFDTMA / f_{PWM\_A} = PMFDTMA \times P_A \times T_{core} \qquad \textit{Eqn. 15-1}$$

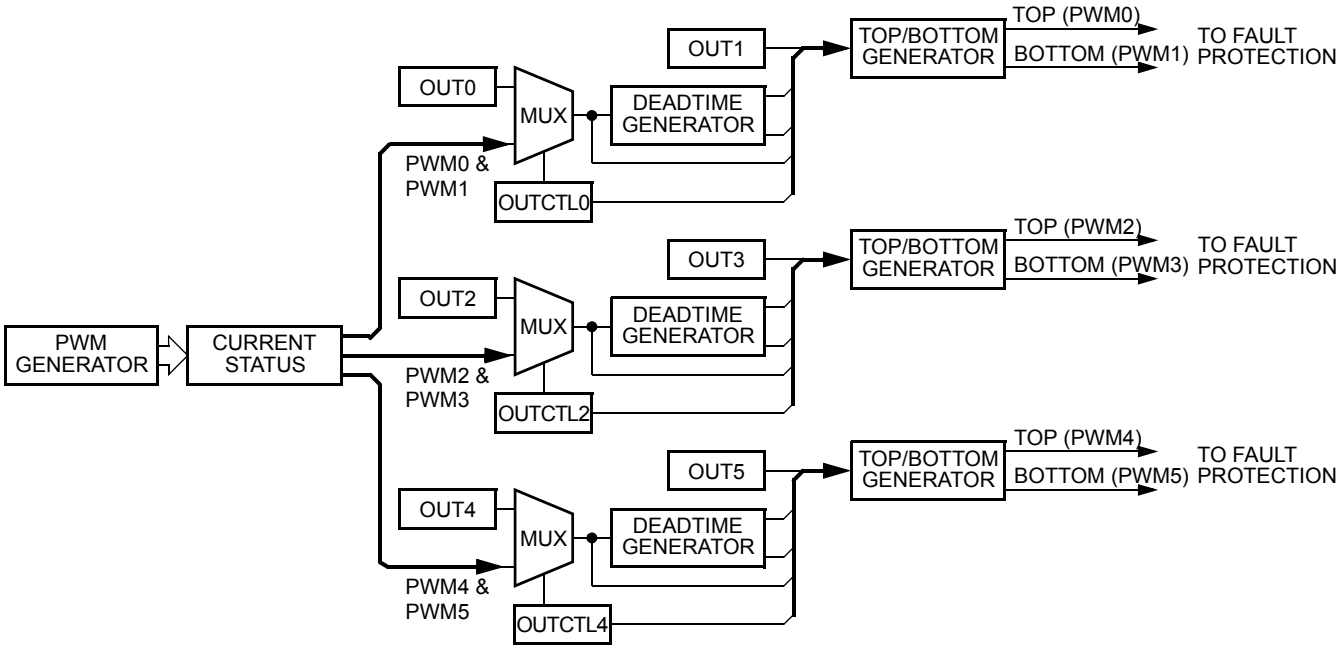


Figure 15-50. Deadtime Generators

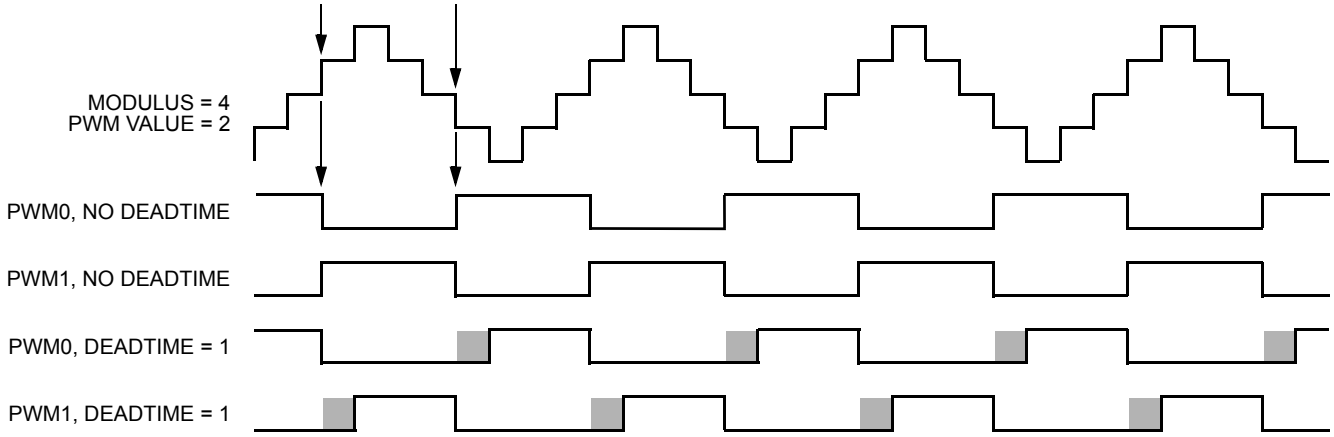


Figure 15-51. Deadtime Insertion, Center Alignment

18.3.2.11 GDU Current Sense Offset Register (GDUCSO)

Module Base + 0x000A — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	GCSO1[2:0]			0	GCSO0[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-13. GDU Current Sense Offset (GDUCSO)

1. Read: Anytime
   Write: Anytime

Table 18-14. GDUCSO Register Field Descriptions

Field	Description (See also Section 18.4.8, “Current Sense Amplifier and Overcurrent Comparator)
6:4 GCSO1[2:0]	GDU Current Sense Amplifier 1 Offset — These bits adjust the offset of the current sense amplifier 000 No offset 001 Offset is +3mV (GDUV5 and V6). Offset is +5mV (GDUV4). 010 Offset is +6mV (GDUV5 and V6). Offset is +10mV (GDUV4) 011 Offset is +9mV (GDUV5 and V6). Offset is +15mV (GDUV4) 100 No offset 101 Offset is -9mV (GDUV5 and V6). Offset is -15mV (GDUV4) 110 Offset is -6mV (GDUV5 and V6). Offset is -10mV (GDUV4). 111 Offset is -3mV (GDUV5 and V6). Offset is -5mV (GDUV4).
2:0 GCSO0[2:0]	GDU Current Sense Amplifier 0 Offset — These bits adjust the offset of the current sense amplifier. 000 No offset 001 Offset is +3mV (GDUV5 and V6). Offset is +5mV (GDUV4). 010 Offset is +6mV (GDUV5 and V6). Offset is +10mV (GDUV4) 011 Offset is +9mV (GDUV5 and V6). Offset is +15mV (GDUV4) 100 No offset 101 Offset is -9mV (GDUV5 and V6). Offset is -15mV (GDUV4) 110 Offset is -6mV (GDUV5 and V6). Offset is -10mV (GDUV4). 111 Offset is -3mV (GDUV5 and V6). Offset is -5mV (GDUV4).

18.3.2.12 GDU Desaturation Level Register (GDUDSLVL)

Module Base + 0x000B — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GDSFHS	GDSLHS[2:0]			GDSFLS	GDSLLS[2:0]		
W								
Reset	0	0	0	0	0	1	1	1

= Unimplemented

Figure 18-14. GDU Desaturation Level Register (GDUDSLVL)

1. Read: Anytime
   Write: Only if GWP=0

18.3.2.17 GDU Control Register 1 (GDUCTR1)

Module Base + 0x0010 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GSRMOD1	GSRMOD0	0	0	0	0	0	TDEL
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-19. GDU Control Register 1 (GDUCTR1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-21. GDUCTR1 Register Field Descriptions

Field	Description
7 GSRMOD1	GDU Switched Reluctance Motor Mode 1 — This bit cannot be modified after GWP bit is set. This bit controls the routing of the LDx pins to the low-side desaturation comparators for switched reluctance motor. See Figure 18-23 0 HSx routed to low-side desaturation comparator 1 LDx routed to low-side desaturation comparator
6 GSRMOD0	GDU Switched Reluctance Motor Mode 0 — This bit cannot be modified after GWP bit is set. 0 BLDC mode. Don't allow HGx and LGx high at the same time. 1 SR mode. Allow HGx and LGx high at the same time.
0 TDEL	**t_{delon} / t_{deloff} Control** — This bit controls the parameters t_{delon} and t_{deloff}. It cannot be modified after GWP bit is set. This bit must be set to meet the min and max values for t_{delon} and t_{deloff} specified in the electrical specification. If this bit is cleared the values for t_{delon} and t_{deloff} are out of spec.

NOTE

GDU Control Register 1 GDUCTR1 availability is defined at device level.

Chapter 19
LIN/HV Physical Layer (S12LINPHYV3)

Table 19-1. Revision History Table

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V02.09	27 Jun 2013	Feature list	- Added the SAE J2602-2 LIN compliance.
V02.10	21 Aug 2013	Overcurrent and TxD-dominant timeout interrupt descriptions	- Specified the time after which the interrupt flags are set again after having been cleared while the error condition is still present.
V02.11	19 Sep 2013	All	- Removed preliminary note. - Fixed grammar and spelling throughout the document.
V02.12	20 Sep 2013	Standby Mode	- Clarified Standby mode behavior.
V02.13	8 Oct 2013	All	- More grammar, spelling, and formating fixes throughout the document.
V03.01	08 May 2014	All	- Added HV PHY feature.

19.1 Introduction

This chapter provides information for both the LIN physical interface and the HV interface. Devices may include either a LINPHY or HVPHY module. The device overview section specifies the LINPHY/HVPHY to device mapping.

The LIN (Local Interconnect Network) bus pin provides a physical layer for single-wire communication in automotive applications. The LIN Physical Layer is designed to meet the LIN Physical Layer 2.2 specification from LIN consortium.

The HV physical interface provides a physical layer for single-wire communication. It can be used, among other examples, for PWM applications since it can be connected to an internal timer.

NOTE

All references to LIN (e.g. names of bits, registers, signals, pins, interrupts, etc.) apply to the HV physical interface as well. The same names have been kept to highlight and facilitate the hardware and software compatibility between both versions. Nevertheless, cases where particular LIN features do not apply to the HV physical interface version are specifically mentioned.

19.3.2.2 LIN Control Register (LPCR)

Module Base + Address 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 19-4. LIN Control Register (LPCR)

1. Read: Anytime

   Write: Anytime,

Table 19-3. LPCR Field Description

Field	Description
3 LPE	LIN Enable Bit — If set, this bit enables the LIN Physical Layer. 0 The LIN Physical Layer is in shutdown mode. None of the LIN Physical Layer functions are available, except that the bus line is held in its recessive state by a high ohmic (330kΩ) resistor. All registers are normally accessible. 1 The LIN Physical Layer is not in shutdown mode.
2 RXONLY	Receive Only Mode bit — This bit controls RXONLY mode. 0 The LIN Physical Layer is not in receive only mode. 1 The LIN Physical Layer is in receive only mode.
1 LPWUE	LIN Wake-Up Enable — This bit controls the wake-up feature in standby mode. 0 In standby mode the wake-up feature is disabled. 1 In standby mode the wake-up feature is enabled.
0 LPPUE	LIN Pullup Resistor Enable — Selects pullup resistor. 0 The pullup resistor is high ohmic (330 kΩ). 1 The 34 kΩ pullup is switched on (except if LPE=0 or when in standby mode with LPWUE=0).

20.4.5.4 P-Flash Commands

Table 20-30 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 20-30. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.
0x02	Erase Verify Block	Verify that a P-Flash block is erased.
0x03	Erase Verify P-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x04	Read Once	Read a dedicated 64 byte field in the nonvolatile information register in P-Flash block that was previously programmed using the Program Once command.
0x06	Program P-Flash	Program a phrase in a P-Flash block.
0x07	Program Once	Program a dedicated 64 byte field in the nonvolatile information register in P-Flash block that is allowed to be programmed only once.
0x08	Erase All Blocks	Erase all P-Flash (and EEPROM) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the DFPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a P-Flash (or EEPROM) block. An erase of the full P-Flash block is only possible when FPLDIS, FPHDIS and FPOPEN bits in the FPROT register are set prior to launching the command.
0x0A	Erase P-Flash Sector	Erase all bytes in a P-Flash sector.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all P-Flash (and EEPROM) blocks and verifying that all P-Flash (and EEPROM) blocks are erased.
0x0C	Verify Backdoor Access Key	Supports a method of releasing MCU security by verifying a set of security keys.
0x0D	Set User Margin Level	Specifies a user margin read level for all P-Flash blocks.
0x0E	Set Field Margin Level	Specifies a field margin read level for all P-Flash blocks (special modes only).
0x13	Protection Override	Supports a mode to temporarily override Protection configuration (for P-Flash and/or EEPROM) by verifying a key.

20.4.5.5 EEPROM Commands

Table 20-31 summarizes the valid EEPROM commands along with the effects of the commands on the EEPROM block.

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low or high order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

Either left aligned or center aligned output mode can be used in concatenated mode and is controlled by the low order CAEx bit. The high order CAEx bit has no effect.

Table 22-13 is used to summarize which channels are used to set the various control bits when in 16-bit mode.

Table 22-13. 16-bit Concatenation Mode Summary

Note: Bits related to available channels have functional significance.

CONxx	PWMEx	PPOLx	PCLKx	CAEx	PWMx Output
CON67	PWME7	PPOL7	PCLK7	CAE7	PWM7
CON45	PWME5	PPOL5	PCLK5	CAE5	PWM5
CON23	PWME3	PPOL3	PCLK3	CAE3	PWM3
CON01	PWME1	PPOL1	PCLK1	CAE1	PWM1

22.4.2.8 PWM Boundary Cases

Table 22-14 summarizes the boundary conditions for the PWM regardless of the output mode (left aligned or center aligned) and 8-bit (normal) or 16-bit (concatenation).

Table 22-14. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
$00 (indicates no duty)	>$00	1	Always low
$00 (indicates no duty)	>$00	0	Always high
XX	$00[1] (indicates no period)	1	Always high
XX	$00[1] (indicates no period)	0	Always low
>= PWMPERx	XX	1	Always high
>= PWMPERx	XX	0	Always low

1. Counter = $00 and does not count.

22.5 Resets

The reset state of each individual bit is listed within the Section 22.3.2, “Register Descriptions” which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters do not count.

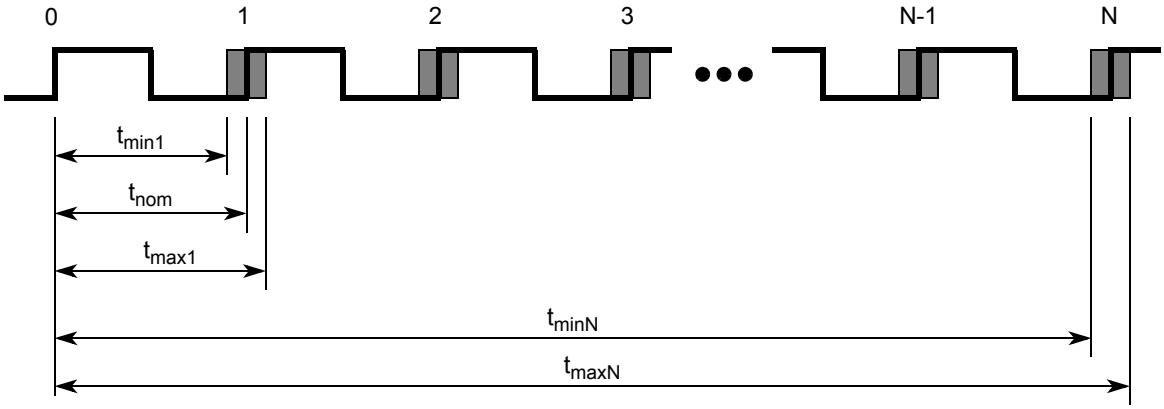


Figure B-1. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

The following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N(POSTDIV + 1)}}$$

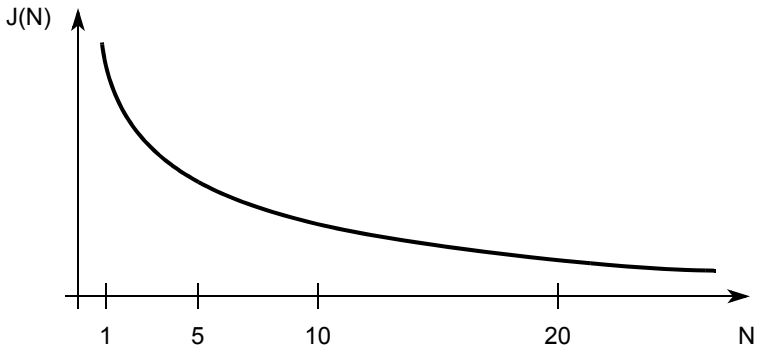
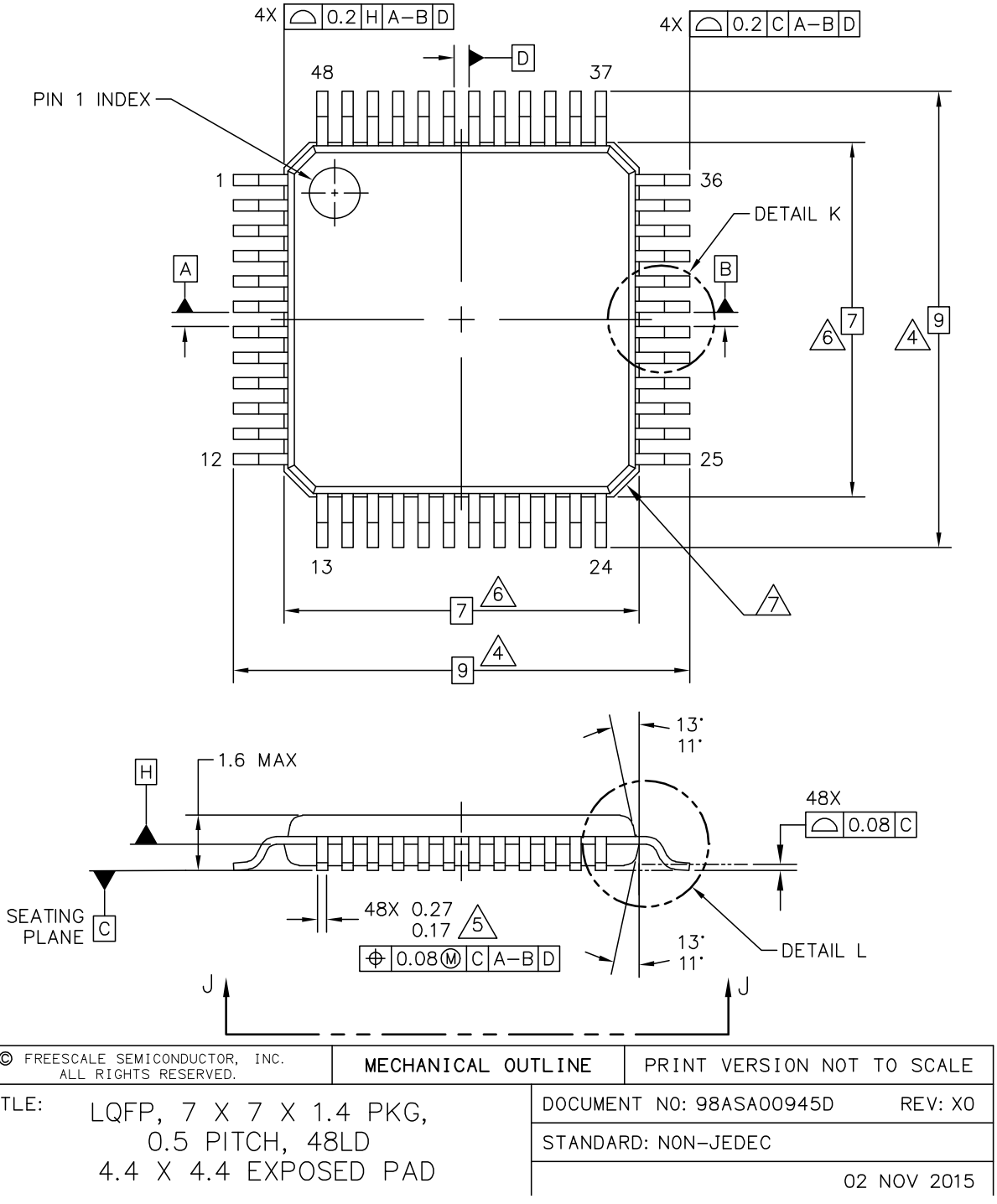


Figure B-2. Maximum Bus Clock Jitter Approximation (N = number of bus cycles)

K.1 48LQFP-EP Mechanical Information

Figure K-1. 48LQFP-EP Mechanical Information



M.14 0x0640-0x067F ADC1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0640	ADC1CTL_0	R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
		W								
0x0641	ADC1CTL_1	R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
		W								
0x0642	ADC1STS	R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
		W								
0x0643	ADC1TIM	R	0	PRS[6:0]						
		W								
0x0644	ADC1FMT	R	DJM	0	0	0	0	SRES[2:0]		
		W								
0x0645	ADC1FLWCTL	R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
		W								
0x0646	ADC1EIE	R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
		W								
0x0647	ADC1IE	R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
		W								
0x0648	ADC1EiF	R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
		W								
0x0649	ADC1IF	R	SEQAD_IF	CONIF_OIF	Reserved	0	0	0	0	0
		W								
0x064A	ADC1CONIE_0	R	CON_IE[15:8]							
		W								
0x064B	ADC1CONIE_1	R	CON_IE[7:1]							EOL_IE
		W								
0x064C	ADC1CONIF_0	R	CON_IF[15:8]							
		W								
0x064D	ADC1CONIF_1	R	CON_IF[7:1]							EOL_IF
		W								
0x064E	ADC1IMDRI_0	R	CSL_IMD	RVL_IMD	0	0	0	0	0	0
0x064F	ADC1IMDRI_1	R	0	0	RIDX_IMD					
		W								
0x0650	ADC1EOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0651	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0652	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0653	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0654	ADC1CMD_0	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0655	ADC1CMD_1 (not ZVMC256)	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0655	ADC1CMD_1 (ZVMC256)	R	VRH_SEL[1:0]		CH_SEL[5:0]					
		W								