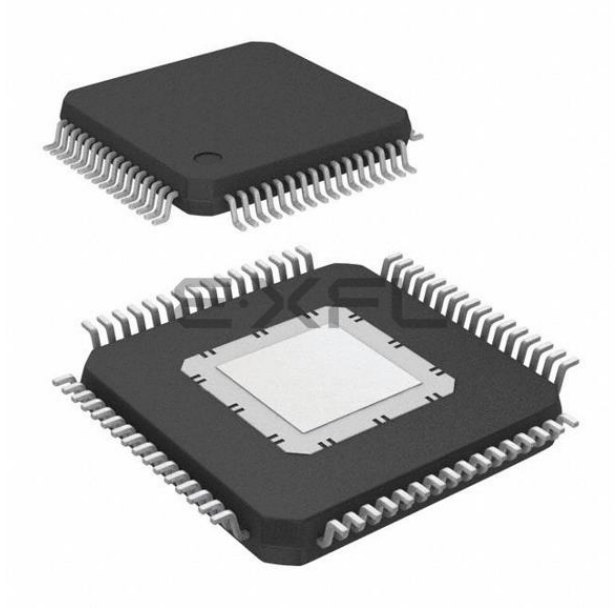

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f3vkh

Table 5-6. BDCCSRL Field Descriptions (continued)

Field	Description
0 ILLCMD	**Illegal Command Flag** — Indicates an illegal BDC command. This bit is set in the following cases: When an unimplemented BDC command opcode is received. When a DUMP_MEM{_WS}, FILL_MEM{_WS} or READ_SAME{_WS} is attempted in an illegal sequence. When an active BDM command is received whilst BDM is not active When a non Always-available command is received whilst the BDC is disabled or a flash mass erase is ongoing. When a non Always-available command is received whilst the device is secure Read commands return a value of 0xEE for each data byte Writing a “1” to this bit, clears the bit. 0 No illegal command detected. 1 Illegal BDC command detected.

5.4 Functional Description

5.4.1 Security

If the device resets with the system secured, the device clears the BDCCSR UNSEC bit. In the secure state BDC access is restricted to the BDCCSR register. A mass erase can be requested using the ERASE_FLASH command. If the mass erase is completed successfully, the device programs the security bits to the unsecure state and sets the BDC UNSEC bit. If the mass erase is unsuccessful, the device remains secure and the UNSEC bit is not set.

For more information regarding security, please refer to device specific security information.

5.4.2 Enabling BDC And Entering Active BDM

BDM can be activated only after being enabled. BDC is enabled by setting the ENBDC bit in the BDCCSR register, via the single-wire interface, using the command WRITE_BDCCSR.

After being enabled, BDM is activated by one of the following[1]:

- The BDC BACKGROUND command
- A CPU BGND instruction
- The DBG Breakpoint mechanism

Alternatively BDM can be activated directly from reset when resetting into Special Single Chip Mode.

The BDC is ready for receiving the first command 10 core clock cycles after the deassertion of the internal reset signal. This is delayed relative to the external pin reset as specified in the device reset documentation. On S12Z devices an NVM initialization phase follows reset. During this phase the BDC commands classified as always available are carried out immediately, whereas other BDC commands are subject to delayed response due to the NVM initialization phase.

NOTE

After resetting into SSC mode, the initial PC address must be supplied by the host using the WRITE_Rn command before issuing the GO command.

1. BDM active immediately out of special single-chip reset.

5.4.5.2.1 FILL_MEM and DUMP_MEM Increments and Alignment

FILL_MEM and DUMP_MEM increment the previously accessed address by the previous access size to calculate the address of the current access. On misaligned longword accesses, the address bits [1:0] are forced to zero, therefore the following FILL_MEM or DUMP_MEM increment to the first address in the next 4-byte field. This is shown in Table 5-11, the address of the first DUMP_MEM.32 following READ_MEM.32 being calculated from 0x004000+4.

When misaligned word accesses are realigned, then the original address (not the realigned address) is incremented for the following FILL_MEM, DUMP_MEM command.

Misaligned word accesses can cause the same locations to be read twice as shown in rows 6 and 7. The hardware ensures alignment at an attempted misaligned word access across a 4-byte boundary, as shown in row 7. The following word access in row 8 continues from the realigned address of row 7.

Table 5-11. Consecutive Accesses With Variable Size

Row	Command	Address	Address[1:0]	00	01	10	11
1	READ_MEM.32	0x004003	11	Accessed	Accessed	Accessed	Accessed
2	DUMP_MEM.32	0x004004	00	Accessed	Accessed	Accessed	Accessed
3	DUMP_MEM.16	0x004008	00	Accessed	Accessed		
4	DUMP_MEM.16	0x00400A	10			Accessed	Accessed
5	DUMP_MEM.08	0x00400C	00	Accessed			
6	DUMP_MEM.16	0x00400D	01		Accessed	Accessed	
7	DUMP_MEM.16	0x00400E	10			Accessed	Accessed
8	DUMP_MEM.16	0x004010	01	Accessed	Accessed		

5.4.5.2.2 READ_SAME Effects Of Variable Access Size

READ_SAME uses the unadjusted address given in the previous READ_MEM command as a base address for subsequent READ_SAME commands. When the READ_MEM and READ_SAME size parameters differ then READ_SAME uses the original base address buts aligns 32-bit and 16-bit accesses, where those accesses would otherwise cross the aligned 4-byte boundary. Table 5-12 shows some examples of this.

Table 5-12. Consecutive READ_SAME Accesses With Variable Size

Row	Command	Base Address	00	01	10	11
1	READ_MEM.32	0x004003	Accessed	Accessed	Accessed	Accessed
2	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
3	READ_SAME.16	—			Accessed	Accessed
4	READ_SAME.08	—				Accessed
5	READ_MEM.08	0x004000	Accessed			
6	READ_SAME.08	—	Accessed			
7	READ_SAME.16	—	Accessed	Accessed		
8	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
9	READ_MEM.08	0x004002			Accessed	

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 ECCSTAT	R	0	0	0	0	0	0	0	RDY
	W								
0x0001 ECCIE	R	0	0	0	0	0	0	0	SBEEIE
	W								
0x0002 ECCIF	R	0	0	0	0	0	0	0	SBEEIF
	W								
0x0003 - 0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 ECCDPTRH	R	DPTR[23:16]							
	W								
0x0008 ECCDPTRM	R	DPTR[15:8]							
	W								
0x0009 ECCDPTRL	R	DPTR[7:1]							0
	W								
0x000A - 0x000B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x000C ECCDDH	R	DDATA[15:8]							
	W								
0x000D ECCDDL	R	DDATA[7:0]							
	W								
0x000E ECCDE	R	0	0	DECC[5:0]					
	W								
0x000F ECCDCMD	R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
	W								

= Unimplemented, Reserved, Read as zero

Figure 7-1. SRAM_ECC Register Summary

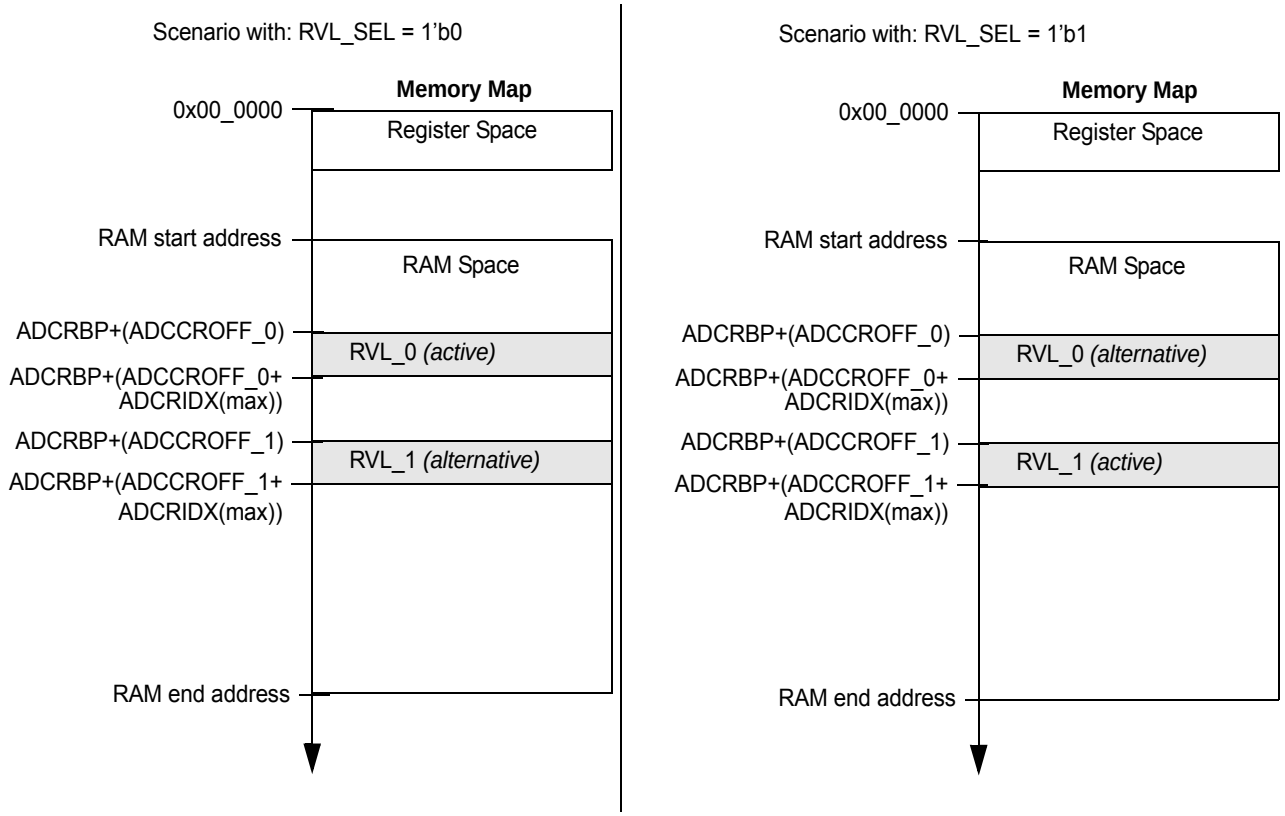
```
/* put your code to loop and wait for the LOCKIF or */
/* poll CPMUIFLG register until both LOCK status is “1” */
/* that is CPMUIFLG == 0x18 */

/*..............continue to your main code execution here..............*/
```

9.6.3.2.3 Introduction of the two Result Value Lists (RVLs)

The same list-based architecture as described above for the CSL has been implemented for the Result Value List (RVL) with corresponding address registers (ADCRBP, ADCCROFF_0/1, ADCRIDX).
The final address for conversion result storage is calculated by the sum of these registers (e.g.: ADCRBP+ADCCROFF_0+ADCRIDX or ADCRBP+ADCCROFF_1+ADCRIDX).
The RVL_BMOD bit selects if the RVL is used in double buffer or single buffer mode. In double buffer mode the RVL is swapped:

- Each time an “End Of List” command type got executed followed by the first conversion from top of the next CSL and related (first) result is about to be stored
- A CSL got aborted (bit SEQA=1’b1) and ADC enters idle state (becomes ready for new flow control events)

Using the RVL in double buffer mode the RVL is not swapped after exit from Stop Mode or Wait Mode with bit SWAI set. Hence the RVL used before entry of Stop or Wait Mode with bit SWAI set is overwritten after exit from the MCU Operating Mode (see also Section 9.3.1.2, “MCU Operating Modes).
Which list is actively used for the ADC conversion result storage is indicated by bit RVL_SEL. The register to define the RVL start addresses (ADCRBP) can be set to any even location of the system RAM area. It is the user’s responsibility to make sure that the different ADC lists do not overlap or exceed the system RAM area. The error flag IA_EIF will be set for accesses to ranges outside system RAM area and cause an error interrupt if enabled.



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 9-33. Result Value List Schema in Double Buffer Mode

13.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
W								
Reset:	0	0	0	1	0	0	0	1

= Unimplemented

Figure 13-5. MSCAN Control Register 1 (CANCTL1)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-3. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 13.4.3.2, “Clock System,” and Section Figure 13-43., “MSCAN Clocking Scheme,”). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 13.4.4.4, “Listen-Only Mode”). In addition, the error counters are frozen. Listen only mode supports applications which require “hot plugging” or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
3 BORM	**Bus-Off Recovery Mode** — This bit configures the bus-off state recovery mode of the MSCAN. Refer to Section 13.5.2, “Bus-Off Recovery,” for details. 0 Automatic bus-off recovery (see Bosch CAN 2.0A/B protocol specification) 1 Bus-off recovery upon user request

Module Base + 0x000F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-19. MSCAN Transmit Error Counter (CANTXERR)

1. Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
   Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

13.3.2.17 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 13.3.3.1, “Identifier Registers (IDR0–IDR3)”) of incoming messages in a bit by bit manner (see Section 13.4.3, “Identifier Acceptance Filter”).

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

Module Base + 0x0010 to Module Base + 0x0013 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 13-20. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

14.3.2.3 PTU Interrupt Enable Register High (PTUIEH)

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTUROIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-5. PTU Interrupt Enable Register High (PTUIEH)

1. Read: Anytime
   Write: Anytime

Table 14-5. PTUIEH Register Field Descriptions

Field	Description
0 PTUROIE	PTU Reload Overrun Interrupt Enable — Enables PTU reload overrun interrupt. 0 No interrupt will be requested whenever PTUROIF is set 1 Interrupt will be requested whenever PTUROIF is set

14.3.2.4 PTU Interrupt Enable Register Low (PTUIEL)

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TG1AEIE	TG1REIE	TG1TEIE	TG1DIE	TG0AEIE	TG0REIE	TG0TEIE	TG0DIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-6. PTU Interrupt Enable Register Low (PTUIEL)

1. Read: Anytime
   Write: Anytime

Table 14-6. PTUIEL Register Field Descriptions

Field	Description
7 TG1AEIE	Trigger Generator 1 Memory Access Error Interrupt Enable — Enables trigger generator memory access error interrupt. 0 No interrupt will be requested whenever TG1AEIF is set 1 Interrupt will be requested whenever TG1AEIF is set
6 TG1REIE	Trigger Generator 1 Reload Error Interrupt Enable — Enables trigger generator reload error interrupt. 0 No interrupt will be requested whenever TG1REIF is set 1 Interrupt will be requested whenever TG1REIF is set

14.3.2.15 Trigger Generator 0 List 0 Index (TG0L0IDX)

Module Base + 0x0014 Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	TG0L0IDX[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-17. Trigger Generator 0 List 0 Index (TG0L0IDX)

1. Read: Anytime
   Write: Never

Table 14-17. TG0L0IDX Register Field Descriptions

Field	Description
6:0 TG0L0IDX [6:0]	Trigger Generator 0 List 0 Index Register — This register defines offset of the start point for the trigger event list 0 used by trigger generator 0. This register is read only, so the list 0 for trigger generator 0 will start at the PTUPTR address. For more information see Section 14.4.2, “Memory based trigger event list”.

14.3.2.16 Trigger Generator 0 List 1 Index (TG0L1IDX)

Module Base + 0x0015 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	TG0L1IDX[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-18. Trigger Generator 0 List 1 Index (TG0L1IDX)

1. Read: Anytime
   Write: Anytime, if TG0EN bit is cleared

Table 14-18. TG0L1IDX Register Field Descriptions

Field	Description
6:0 TG0L1IDX [6:0]	Trigger Generator 0 List 1 Index Register — This register cannot be modified after the TG0EN bit is set. This register defines offset of the start point for the trigger event list 1 used by trigger generator 0. For more information see Section 14.4.2, “Memory based trigger event list”.

15.3.2 Register Descriptions

15.3.2.1 PMF Configure 0 Register (PMFCFG0)

Address: Module Base + 0x0000 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
Reset	0	0	0	0	0	0	0	0

Figure 15-3. PMF Configure 0 Register (PMFCFG0)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

Table 15-6. PMFCFG0 Field Descriptions

Field	Description
7 WP	**Write Protect**— This bit enables write protection to be used for all write-protectable registers. While clear, WP allows write-protected registers to be written. When set, WP prevents any further writes to write-protected registers. Once set, WP can be cleared only by reset. 0 Write-protectable registers may be written 1 Write-protectable registers are write-protected
6 MTG	**Multiple Timebase Generators** — This bit determines the number of timebase counters used. This bit cannot be modified after the WP bit is set. If MTG is set, PWM generators B and C and registers 0x0028 – 0x0037 are availabled.The three generators have their own variable frequencies and are not synchronized. If MTG is cleared, PMF registers from 0x0028 – 0x0037 can not be written and read zeroes, and bits EDGEC and EDGEB are ignored. Pair A, Pair B, and Pair C PWMs are synchronized to PWM generator A and use registers from 0x0020 – 0x0027. 0 Single timebase generator 1 Multiple timebase generators
5 EDGEC	**Edge-Aligned or Center-Aligned PWM for Pair C —** This bit determines whether PWM4 and PWM5 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are center-aligned PWMs 1 PWM4 and PWM5 are edge-aligned PWMs
4 EDGEB	**Edge-Aligned or Center-Aligned PWM for Pair B —** This bit determines whether PWM2 and PWM3 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are center-aligned PWMs 1 PWM2 and PWM3 are edge-aligned PWMs
3 EDGEA	**Edge-Aligned or Center-Aligned PWM for Pair A—** This bit determines whether PWM0 and PWM1 channels will use edge-aligned or center-aligned waveforms. It determines waveforms for Pair B and Pair C if the MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM0 and PWM1 are center-aligned PWMs 1 PWM0 and PWM1 are edge-aligned PWMs
2 INDEPC	**Independent or Complementary Operation for Pair C**— This bit determines if the PWM channels 4 and 5 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are complementary PWM pair 1 PWM4 and PWM5 are independent PWMs

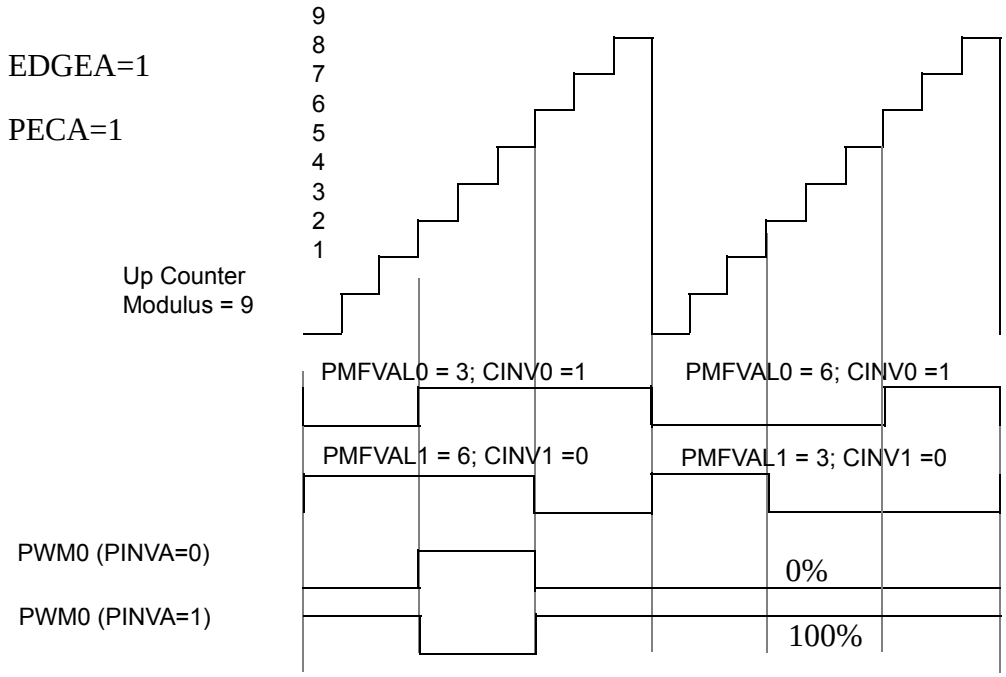


Figure 15-64. Variable Edge Placement Waveform - Phase Shift PWM Output (Edge-Aligned)

15.4.9 Double Switching PWM Output

By using the AND function in Figure 15-63 in complementary center-aligned mode, the PWM output can be configured for double switching operation (Figure 15-65, Figure 15-66). By setting the non-inverted value register greater or equal to the PWM modulus the output function can be switched to single pulse generation on PWM reload cycle basis.

16.4.6 Receiver

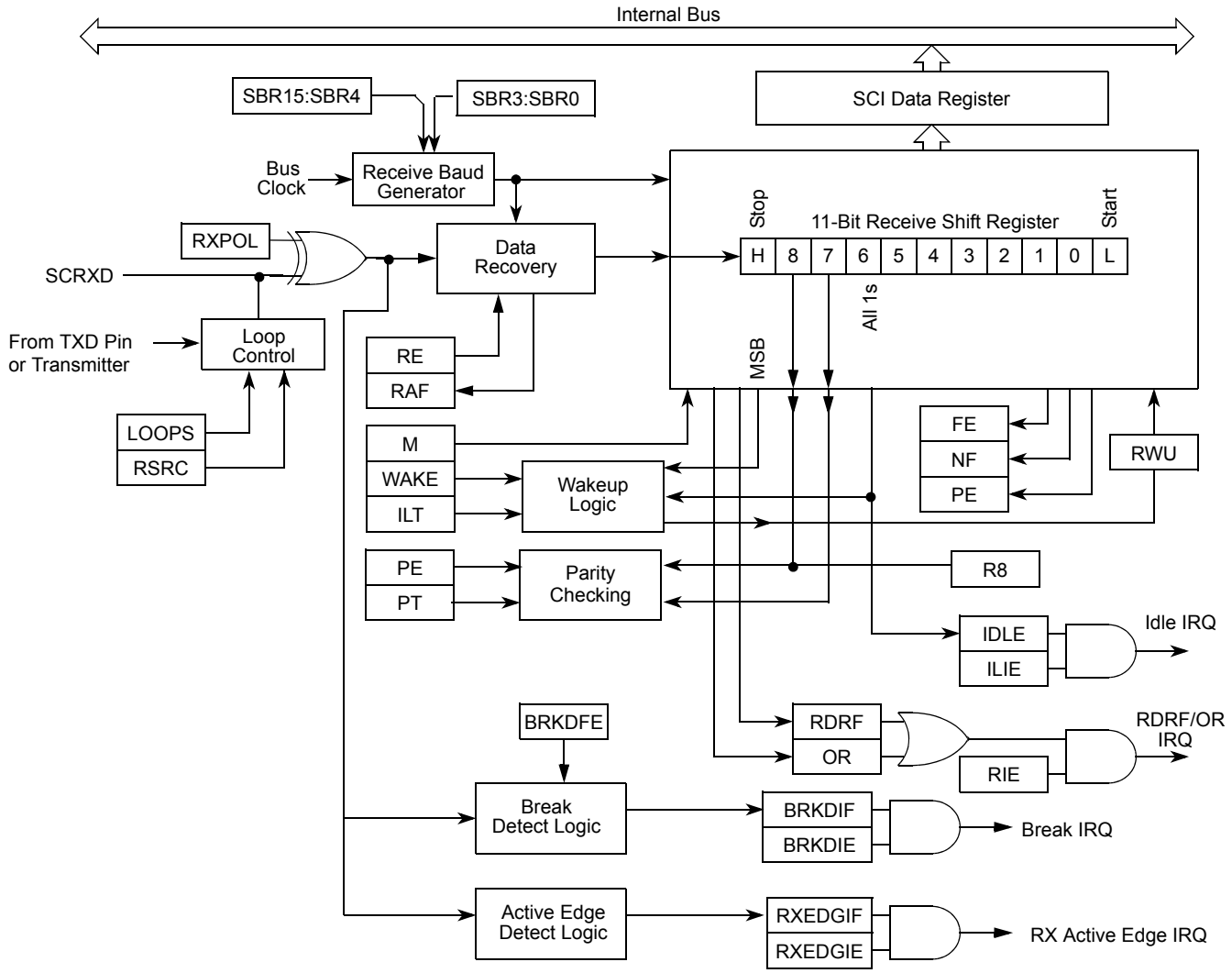


Figure 16-20. SCI Receiver Block Diagram

16.4.6.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

16.4.6.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

Table 20-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]		BUSCLK Frequency (MHz)		FDIV[5:0]
MIN(1)	MAX(2)			MIN[1]	MAX[2]	
18.6	19.6	0x12		44.6	45.6	0x2C
19.6	20.6	0x13		45.6	46.6	0x2D
20.6	21.6	0x14		46.6	47.6	0x2E
21.6	22.6	0x15		47.6	48.6	0x2F
22.6	23.6	0x16		48.6	49.6	0x30
23.6	24.6	0x17		49.6	50.6	0x31
24.6	25.6	0x18				
25.6	26.6	0x19				

1. BUSCLK is Greater Than this value.

2. BUSCLK is Less Than or Equal to this value.

20.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Offset Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	KEYEN[1:0]		RNV[5:2]				SEC[1:0]	
W								
Reset	F(1)	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 20-6. Flash Security Register (FSEC)

1. Loaded from Flash configuration field, during reset sequence.

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0xFF_FE0F located in P-Flash memory (see Table 20-4) as indicated by reset condition F in Figure 20-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

into the Reference Manual for details). Forcing the DFDF status bit by setting FDFD (see Section 20.3.2.5) has effect only on the DFDF status bit value and does not result in an invalid access.

To guarantee the proper read timing from the Flash array, the Flash will control (i.e. pause) the S12Z core accesses, considering that the MCU can be configured to fetch data at a faster frequency than the Flash block can support. Right after reset the Flash will be configured to run with the maximum amount of wait-states enabled; if the user application is setup to run at a slower frequency the control bits FCNFG[WSTAT] (see Section 20.3.2.5) can be configured by the user to disable the generation of wait-states, so it does not impose a performance penalty to the system if the read timing of the S12Z core is setup to be within the margins of the Flash block. For a definition of the frequency values where wait-states can be disabled please refer to the device electrical parameters.

The following sequence must be followed when the transition from a higher frequency to a lower frequency is going to happen:

- Flash resets with wait-states enabled;
- system frequency must be configured to the lower target;
- user writes to FNCNF[WSTAT] to disable wait-states;
- user reads the value of FPSTAT[WSTATACK], the new wait-state configuration will be effective when it reads as 1;
- user must re-write FCLKDIV to set a new value based on the lower frequency.

The following sequence must be followed on the contrary direction, going from a lower frequency to a higher frequency:

- user writes to FCNFG[WSTAT] to enable wait-states;
- user reads the value of FPSTAT[WSTATACK], the new wait-state configuration will be effective when it reads as 1;
- user must re-write FCLKDIV to set a new value based on the higher frequency;
- system frequency must be set to the upper target.

> If the application is going to require the frequency setup to change, the value to be loaded on register FCLKDIV will have to be updated according to the new frequency value. In this scenario the application must take care to avoid locking the value of the FCLKDIV register: bit FDIVLCK must not be set if the value to be loaded on FDIV is going to be re-written, otherwise a reset is going to be required. Please refer to Section 20.3.2.1, “Flash Clock Divider Register (FCLKDIV) and Section 20.4.5.1, “Writing the FCLKDIV Register.

20.4.4 Internal NVM resource

IFR is an internal NVM resource readable by CPU. The IFR fields are shown in Table 20-5.

The NVM Resource Area global address map is shown in Table 20-6.

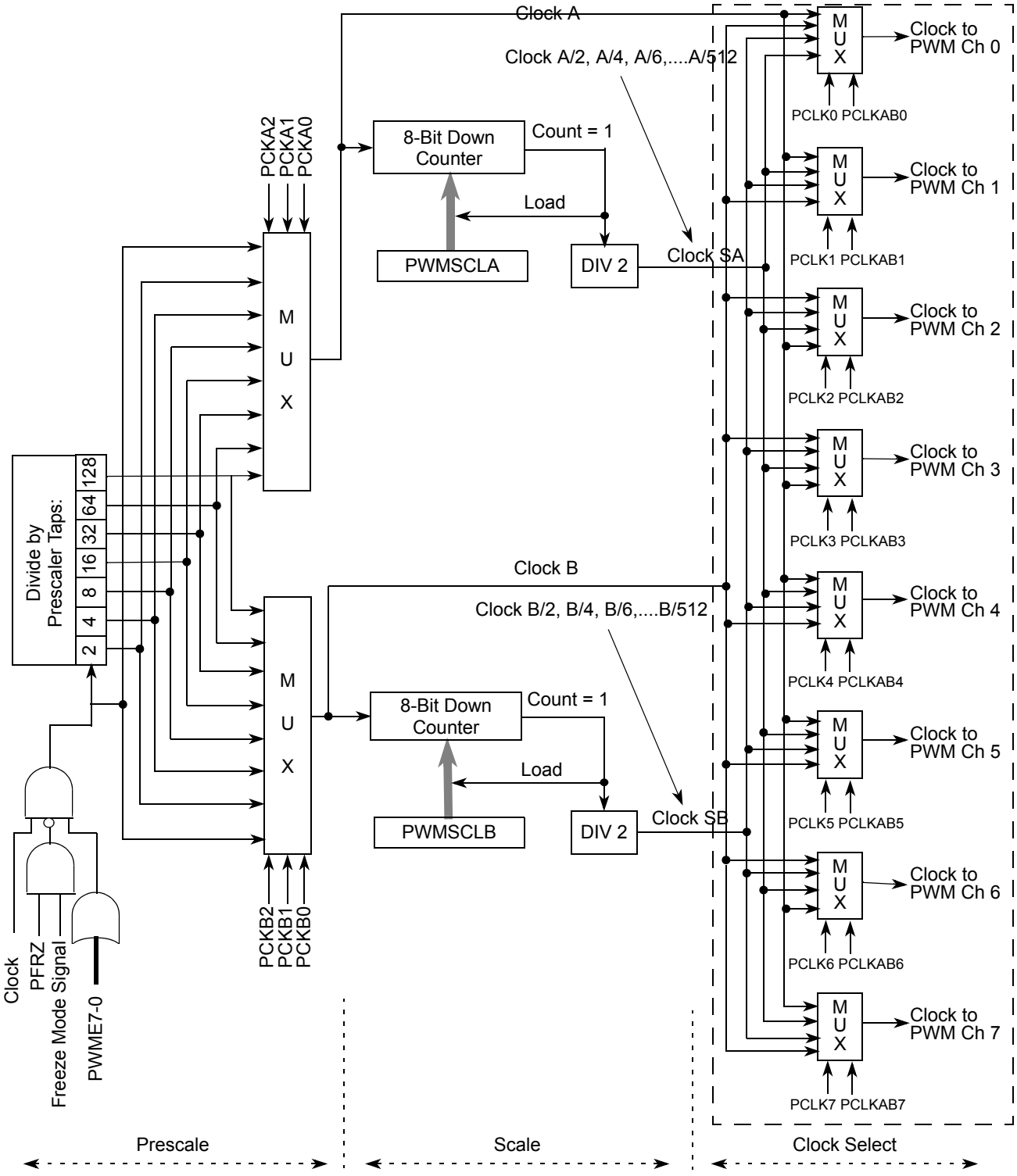


Figure 22-15. PWM Clock Select Block Diagram

Table B-1. Voltage Regulator Electrical Characteristics (Junction Temperature From –40°C To +175°C unless otherwise stated)

Note: VDDA and VDDX must be shorted on the application board.

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
5c		Load Current VDDX[2][3] without external PNP Full Performance Mode 3.5V <= V_{SUP} <=6V -40°C < T_J < 150°C	I_{DDX}	0	—	25	mA
5d		Short Circuit VDDX fall back current V_{DDX} <=0.5V	I_{DDX}	—	100	—	mA
6		Output Voltage VDDC with external PNP[4] Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop) V_{SUP} > =3.5V	V_{DDC}	4.85 4.50 3.13 2.5	5.0 5.0 — 5.5	5.15 5.15 5.15 5.75	V V V V
7		Load Current VDDC Reduced Performance Mode (stop mode)	I_{DDC}	0	—	2.5	mA
8		Low Voltage Interrupt Assert Level[5] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V V
9a		VDDX Low Voltage Reset deassert[6]	V_{LVRXD}	—	3.05	3.13	V
9b		VDDX Low Voltage Reset assert [7]	V_{LVRXA}	2.95	3.02	—	V
10		Trimmed ACLK output frequency	f_{ACLK}	—	20	—	KHz
11		Trimmed ACLK internal clock $\Delta f / f_{nominal}$ [8]	df_{ACLK}	- 6%	—	+ 6%	—
12		The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
13		Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
14		Temperature Sensor output voltage (T_J = 150°C) untrimmed	V_{HT}	—	2.4	—	V
15		High Temperature Interrupt Assert[9] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
16		Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
17		Bandgap output voltage V_{SUP} dependency 3.5 < V_{SUP} < 18V	Δ_{VBGV}	-5[10]	—	5[10]	mV
18		Bandgap output voltage temperature dependency V_{SUP} =12V, -40°C < T_J < 150°C	Δ_{VBGT}	-20	—	20	mV
19a		Max. Base Current For External PNP (VDDX)[11] -40°C < T_J < 150°C	$I_{BCTLMAX}$	2.3	—	—	mA
19b		Max. Base Current For External PNP (VDDX)[11] 150°C < T_J < 175°C	$I_{BCTLMAX}$	1.5	—	—	mA
20a		Max. Base Current For External PNP (VDDC)**[11]** -40°C < T_J < 150°C	$I_{BCTLCMAX}$	2.3	—	—	mA
20b		Max. Base Current For External PNP (VDDC)**[11]** 150°C < T_J < 175°C	$I_{BCTLCMAX}$	1.5	—	—	mA

Appendix G
BATS Electrical Specifications

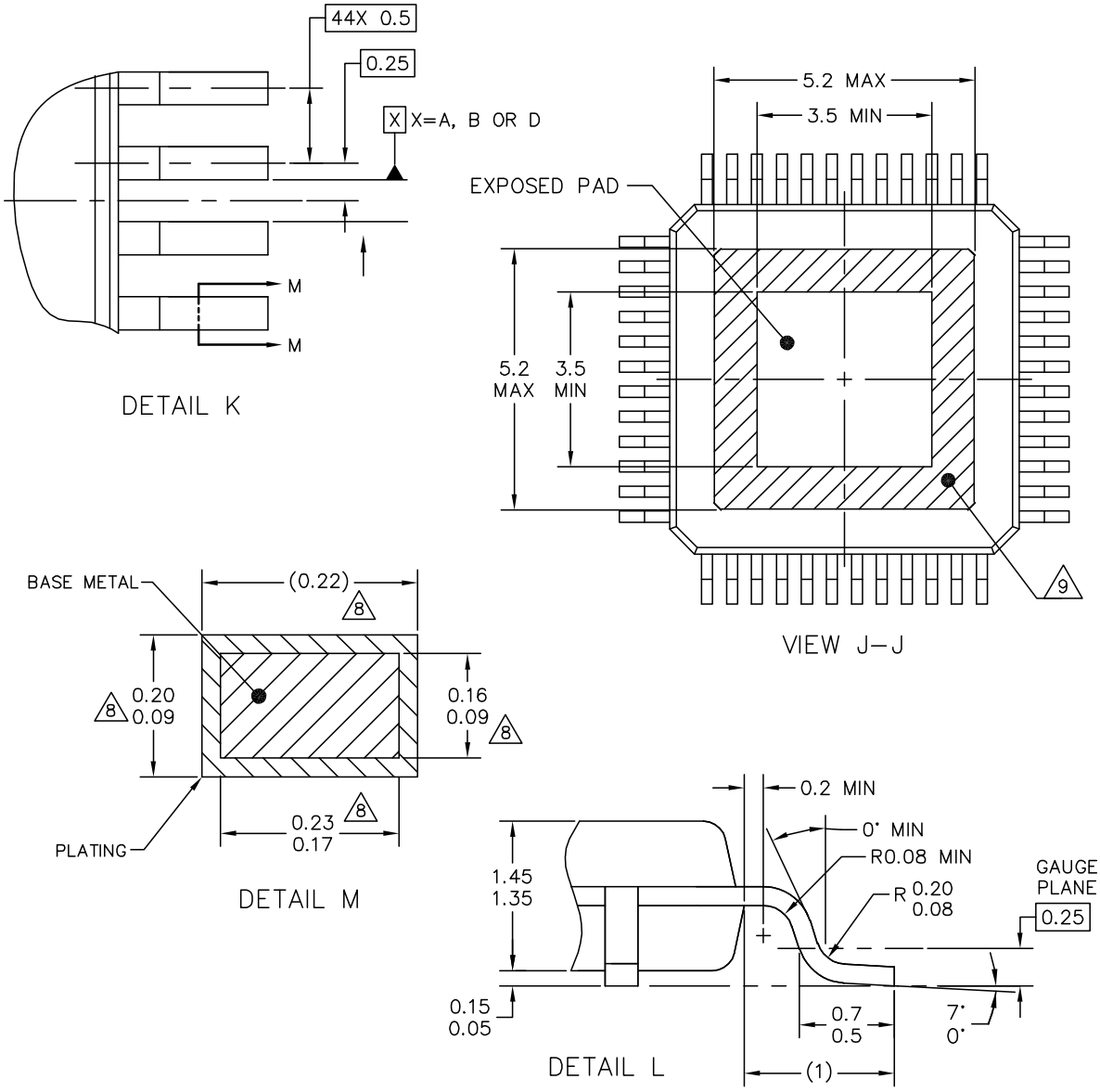
G.1 Static Electrical Characteristics

Table G-1. Static Electrical Characteristics - BATS (Junction Temperature From -40°C To +175°C)

Typical values reflect the approximate parameter mean at T_A = 25°C(1) under nominal conditions unless otherwise noted.							
Num	**C**	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Low Voltage Warning (LBI 1) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI1_A} V_{LBI1_D} V_{LBI1_H}	 4.75 – –	 5.5 – 0.4	 6 6.5 –	 V V V
2		Low Voltage Warning (LBI 2) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI2_A} V_{LBI2_D} V_{LBI2_H}	 6 – –	 6.75 – 0.4	 7.25 7.75 –	 V V V
3		Low Voltage Warning (LBI 3) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI3_A} V_{LBI3_D} V_{LBI3_H}	 7 – –	 7.75 – 0.4	 8.5 9 –	 V V V
4		Low Voltage Warning (LBI 4) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI4_A} V_{LBI4_D} V_{LBI4_H}	 8 – –	 9 – 0.4	 10 10.5 –	 V V V
5		High Voltage Warning (HBI 1) Assert (Measured on VSUP pin, rising edge) Deassert (Measured on VSUP pin, falling edge) Hysteresis (measured on VSUP pin)	 V_{HBI1_A} V_{HBI1_D} V_{HBI1_H}	 14.5 14 –	 16.5 – 1.0	 18 – –	 V V V
6		High Voltage Warning (HBI 2) Assert (Measured on VSUP pin, rising edge) Deassert (Measured on VSUP pin, falling edge) Hysteresis (measured on VSUP pin)	 V_{HBI2_A} V_{HBI2_D} V_{HBI2_H}	 25 24 –	 27.5 – 1.0	 30 – –	 V V V
7		Pin Input Divider Ratio(2) $Ratio_{VSUP} = V_{SUP} / V_{ADC}$ 5.5V < VSUP < 29 V	$Ratio_{VSUP}$	–	9	–	–
8		Analog Input Matching Absolute Error on V_{ADC} - compared to V_{SUP} / $Ratio_{VSUP}$	$AI_{Matching}$	–	+-2%	+-5%	–

1. T_A: Ambient Temperature

2. V_{ADC}: Voltage accessible at the ADC input channel



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TITLE: LQFP, 7 X 7 X 1.4 PKG, 0.5 PITCH, 48LD 4.4 X 4.4 EXPOSED PAD	DOCUMENT NO: 98ASA00945D	REV: X0
	STANDARD: NON-JEDEC	
	02 NOV 2015	

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0506	PMFFIE	R	0	FIE5	0	FIE4	FIE3	FIE2	FIE1	FIE0
		W								
0x0507	PMFFIF	R	0	FIF5	0	FIF4	FIF3	FIF2	FIF1	FIF0
		W								
0x0508	PMFQSMP0	R	0	0	0	0	QSMP5		QSMP4	
		W								
0x0509	PMFQSMP1	R	QSMP3		QSMP2		QSMP1		QSMP0	
		W								
0x050A-0x050B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x050C	PMFOUTC	R	0	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0
		W								
0x050D	PMFOUTB	R	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
		W								
0x050E	PMFDTMS	R	0	0	DT5	DT4	DT3	DT2	DT1	DT0
		W								
0x050F	PMFCCTL	R	0	0	ISENS		0	IPOLC	IPOLB	IPOLA
		W								
0x0510	PMFVAL0	R	PMFVAL0							
		W								
0x0511	PMFVAL0	R	PMFVAL0							
		W								
0x0512	PMFVAL1	R	PMFVAL1							
		W								
0x0513	PMFVAL1	R	PMFVAL1							
		W								
0x0514	PMFVAL2	R	PMFVAL2							
		W								
0x0515	PMFVAL2	R	PMFVAL2							
		W								
0x0516	PMFVAL3	R	PMFVAL3							
		W								
0x0517	PMFVAL3	R	PMFVAL3							
		W								

M.12 0x05C0-0x05FF TIM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05C0	TIM0TIOS	R					IOS3	IOS2	IOS1	IOS0
		W								
0x05C1	TIM0CFORC	R	0	0	0	0	0	0	0	0
		W					FOC3	FOC2	FOC1	FOC0
0x05C2	Reserved	R								
		W								
0x05C3	Reserved	R								
		W								
0x05C4	TIM0TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
		W								
0x05C5	TIM0TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
		W								
0x05C6	TIM0TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
		W								
0x05C7	TIM0TTOV	R					TOV3	TOV2	TOV1	TOV0
		W								
0x05C8	TIM0TCTL1	R								
		W								
0x05C9	TIM0TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		W								
0x05CA	TIM0TCTL3	R								
		W								
0x05CB	TIM0TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		W								
0x05CC	TIM0TIE	R					C3I	C2I	C1I	C0I
		W								
0x05CD	TIM0TSCR2	R	TOI	0	0	0		PR2	PR1	PR0
		W								
0x05CE	TIM0TFLG1	R					C3F	C2F	C1F	C0F
		W								
0x05CF	TIM0TFLG2	R	TOF	0	0	0	0	0	0	0
		W								
0x05D0	TIM0TC0H	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x05D1	TIM0TC0L	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								