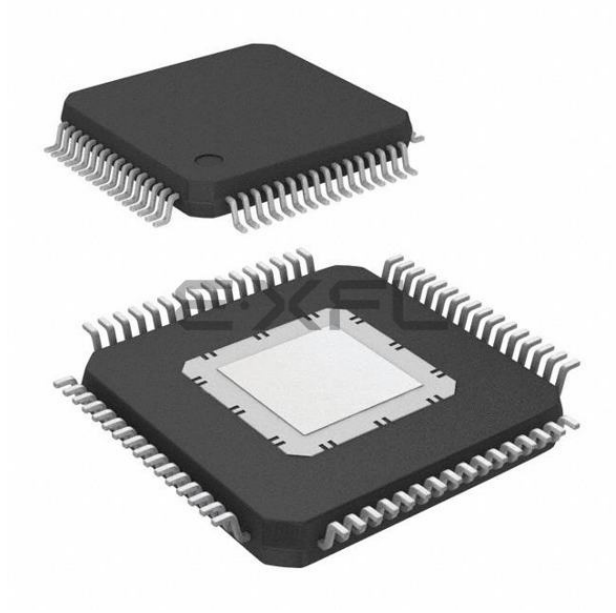

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f3vkhr

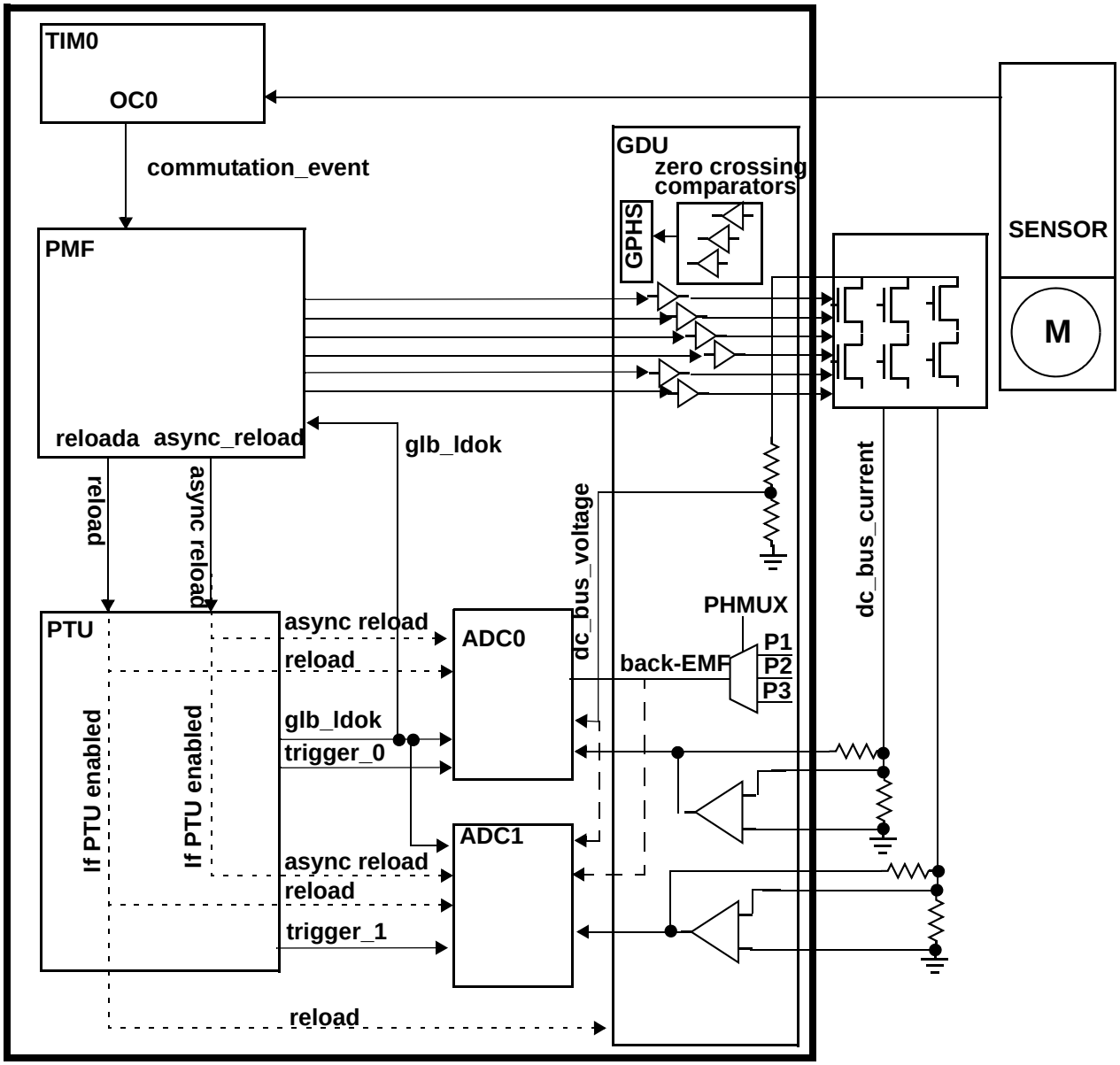
Chapter 3
Memory Mapping Control (S12ZMMCV1)

Chapter 4
Interrupt (S12ZINTV0)

1.13.3.1 Motor Control Loop Overview

The mapping of motor control events at device level as depicted in Figure 1-9 is listed in Table 1-21, whereby the columns list the names used in the module level descriptions

Figure 1-9. Internal Control Loop Configuration



The control loop consists of the PMF, GDU, ADC and PTU modules. The control loop operates using either static, dynamic or asynchronous timing. In the following text the event names given in **bold type** correspond to those shown in Figure 1-9. The PTU and ADC operate using lists stored in memory. These lists define trigger points for the PTU, commands for the ADC and results from the ADC. If the PTU is enabled the reload and async_reload events are immediately passed through to the ADC and GDU modules.

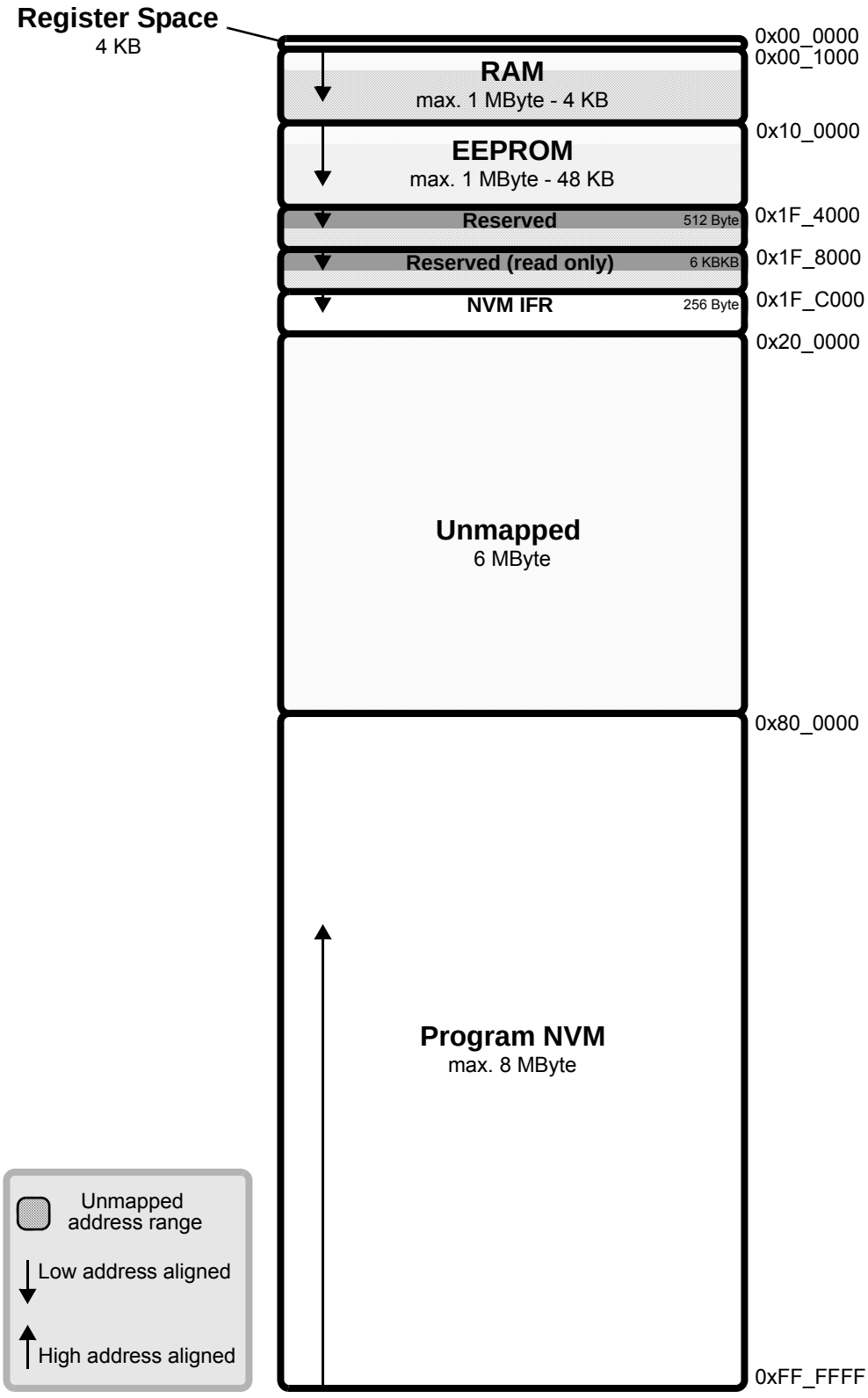


Figure 3-8. Global Memory Map

Table 6-17. DBGSCR1 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State1 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State1 following a match1.
5–4 C2SC[1:0]	Channel 2 State Control. These bits select the targeted next state whilst in State1 following a match2.
7–6 C3SC[1:0]	Channel 3 State Control. If EEVE !=10, these bits select the targeted next state whilst in State1 following a match3. If EEVE = 10, these bits select the targeted next state whilst in State1 following an external event.

Table 6-18. State1 Match State Sequencer Transitions

CxSC[1:0]	Function
00	Match has no effect
01	Match forces sequencer to State2
10	Match forces sequencer to State3
11	Match forces sequencer to Final State

In the case of simultaneous matches, the match on the higher channel number (3...0) has priority.

6.3.2.8 Debug State Control Register 2 (DBGSCR2)

Address: 0x0108

	7	6	5	4	3	2	1	0
R W	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
Reset	0	0	0	0	0	0	0	0

Figure 6-10. Debug State Control Register 2 (DBGSCR2)

Read: Anytime.

Write: If DBG is not armed and PTACT is clear.

The state control register 2 selects the targeted next state whilst in State2. The matches refer to the outputs of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.12”. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-19. DBGSCR2 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State2 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State2 following a match1.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x000F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0010	CPMU HTCTL	R	Reserved	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x0011	CPMU LVCTL	R	0	0	0	0	VDDSIE	LVDS	LVIE	LVIF
		W								
0x0012	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x0013	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x0014	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x0015	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x0016	RESERVED CPMUTEST3	R	0	0	0	0	0	0	0	0
		W								
0x0017	CPMUHTTR	R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
		W								
0x0018	CPMU IRCTRIMH	R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
		W								
0x0019	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x001A	CPMUOSC	R	OSCE	0	0	0	0	0	0	0
		W								
0x001B	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x001C	RESERVED CPMUTEST2	R	0	0	0	0	0	0	0	0
		W								
0x001D	CPMU VREGCTL	R	VRH2EN	VRH1EN	EXTS2ON	EXTS1ON	0	EXTCON	EXTXON	INTXON
		W								
0x001E	CPMUOSC2	R	0	0	0	0	0	0	OMRE	OSCMOD
		W								
0x001F	CPMUVDDS	R	SCS2	SCS1	LVDS2	LVDS1	SCS2IF	SCS1IF	LVS2IF	LVS1IF
		W								

= Unimplemented or Reserved

Figure 8-5. CPMU Register Summary

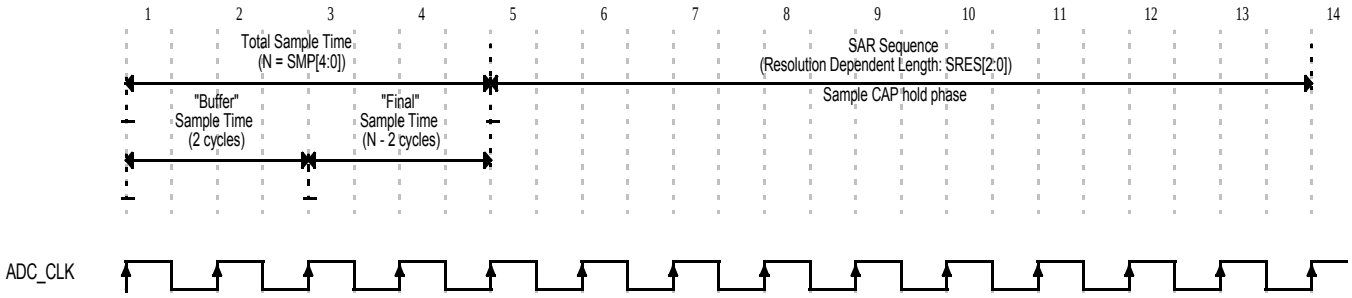


Figure 9-28. Sampling and Conversion Timing Example (8-bit Resolution, 4 Cycle Sampling)

Please note that there is always a pump phase of two ADC_CLK cycles before the sample phase begins, hence glitches during the pump phase could impact the conversion accuracy for short sample times.

9.6.3 Digital Sub-Block

The digital sub-block contains a list-based programmer's model and the control logic for the analog sub-block circuits.

9.6.3.1 Analog-to-Digital (A/D) Machine

The A/D machine performs the analog-to-digital conversion. The resolution is program selectable to be either 8- or 10- or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages.

By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

Only analog input signals within the potential range of VRL_0/1 to VRH_0/1/3 (availability of VRL_1 and VRH_2 see Table 9-2) (A/D reference potentials) will result in a non-railed digital output code.

9.6.3.2 Introduction of the Programmer's Model

The ADC_LBA provides a programmer's model that uses a system memory list-based architecture for definition of the conversion command sequence and conversion result handling.
The Command Sequence List (CSL) and Result Value List (RVL) are implemented in double buffered manner and the buffer mode is user selectable for each list (bits CSL_BMOD, RVL_BMOD). The 32-bit wide conversion command is double buffered and the currently active command is visible in the ADC register map at ADCCMD register space.

9.9.9 Triggered Conversion — Single CSL

Applications that require the conversion of one or more groups of different channels in a periodic and timed manner can make use of a configuration in “Trigger Mode” with a single CSL containing a list of sequences. This means the CSL consists of several sequences each separated by an “End of Sequence” command. The last command of the CSL uses the “End Of List” command with wrap to top of CSL and waiting for a Trigger (CMD_SEL[1:0] =2’b11). Hence after the initial Restart Event each sequence can be launched via a Trigger Event and repetition of the CSL can be launched via a Trigger after execution of the “End Of List” command.

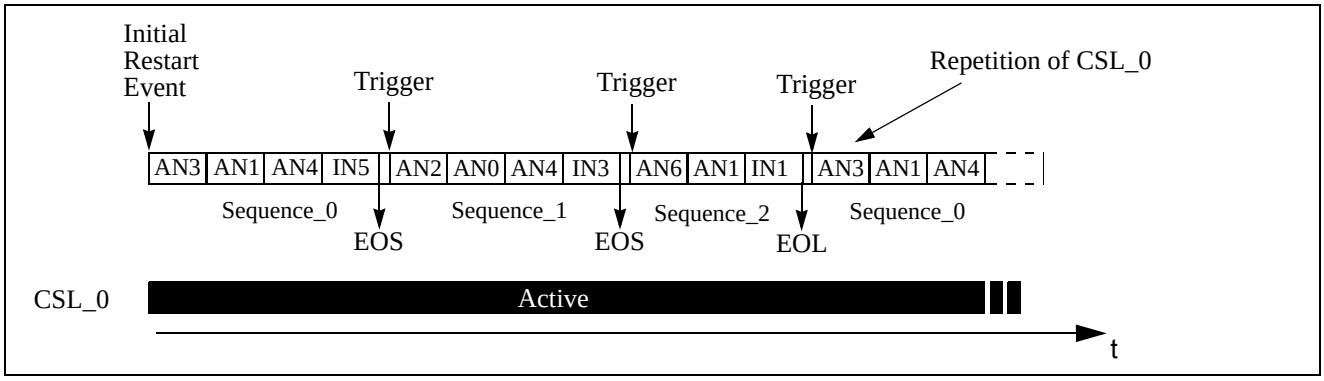


Figure 9-42. Conversion Flow Control Diagram — Triggered Conversion (CSL Repetition)

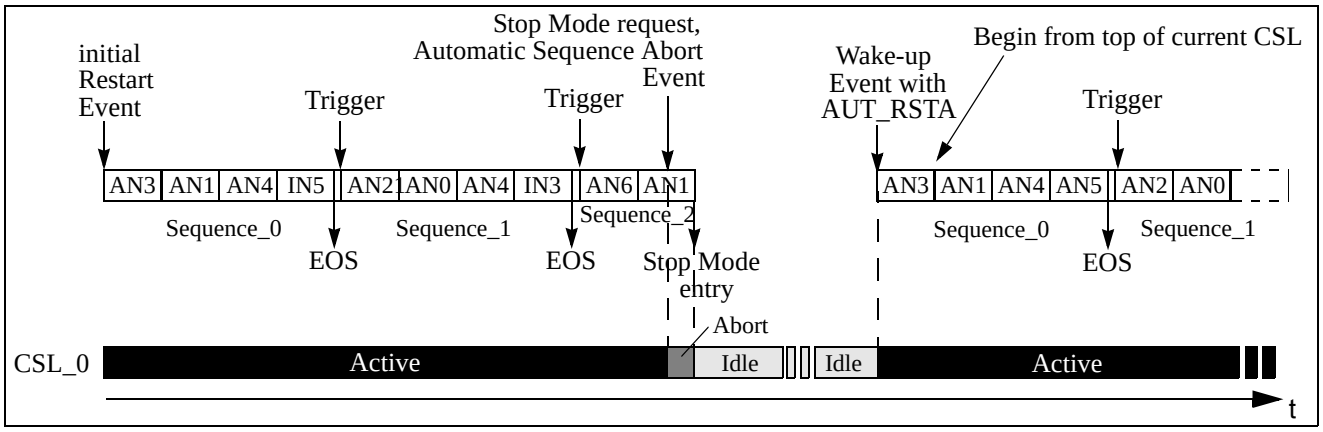


Figure 9-43. Conversion Flow Control Diagram — Triggered Conversion (with Stop Mode)

In case a Low Power Mode is used:
If bit AUT_RSTA is set before Low Power Mode is entered, the conversion continues automatically as soon as a low power mode (Stop Mode or Wait Mode with bit SWAI set) is exited.

13.3.3.3 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.

Module Base + 0x00XC

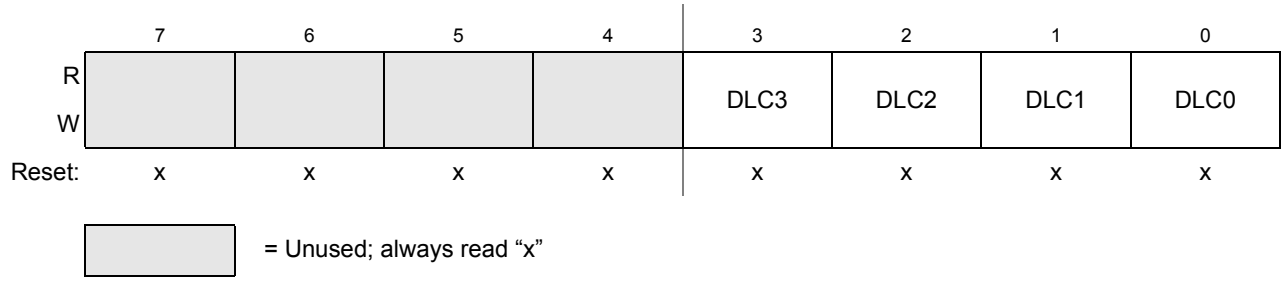


Figure 13-35. Data Length Register (DLR) — Extended Identifier Mapping

Table 13-33. DLR Register Field Descriptions

Field	Description
3-0 DLC[3:0]	**Data Length Code Bits** — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 13-34 shows the effect of setting the DLC bits.

Table 13-34. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

13.3.3.4 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.

Table 15-33. PMFENCC Field Descriptions

Field	Description
7 PWMENC	**PWM Generator C Enable** — If MTG is clear, this bit reads zero and cannot be written. If MTG is set, this bit when set enables the PWM generator C and the PWM4 and PWM5 outputs. When PWMENC is clear, PWM generator C is disabled, and the PWM4 and PWM5 outputs are in their inactive states unless the corresponding OUTCTL bits are set. After setting this bit a reload event is generated at the beginning of the PWM cycle. 0 PWM generator C and PWM4–5 outputs disabled unless the respective OUTCTL bit is set 1 PWM generator C and PWM4–5 outputs enabled
6 GLDOKC	**Global Load Okay C** — When this bit is set, a PMF external global load OK defined on device level replaces the function of LDOKC. This bit cannot be modified after the WP bit is set. 0 LDOKC controls reload of double buffered registers 1 PMF external global load OK controls reload of double buffered registers
2 RSTRTC	**Restart Generator C** — When this bit is set, PWM generator C will be restarted at the next commutation event. This bit cannot be modified after the WP bit is set. 0 No PWM generator C restart at the next commutation event 1 PWM generator C restart at the next commutation event
1 LDOKC	**Load Okay C** — If MTG is clear, this bit reads zero and can not be written. If MTG is set, this bit loads the PRSCC bits, the PMFMODC register and the PMFVAL4–5 registers into a set of buffers. The buffered prescaler divisor C, PWM counter modulus C value, PWM4–5 pulse widths take effect at the next PWM reload. Set LDOKC by reading it when it is logic zero and then writing a logic one to it. LDOKC is automatically cleared after the new values are loaded, or can be manually cleared before a reload by writing a logic zero to it. Reset clears LDOKC. 0 Do not load new modulus C, prescaler C, and PWM4–5 values 1 Load prescaler C, modulus C, and PWM4–5 values **Note:** Do not set PWMENC bit before setting the LDOKC bit and do not clear the LDOKC bit at the same time as setting the PWMENC bit.
0 PWMRIEC	**PWM Reload Interrupt Enable C** — If MTG is clear, this bit reads zero and cannot be written. If MTG is set, this bit enables the PWMRFC flag to generate CPU interrupt requests. 0 PWMRFC CPU interrupt requests disabled 1 PWMRFC CPU interrupt requests enabled

15.3.2.30 PMF Frequency Control C Register (PMFFQCC)

Address: Module Base + 0x0031 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	LDFQC				HALFC	PRSCC		PWMRFC
Reset	0	0	0	0	0	0	0	0

Figure 15-35. PMF Frequency Control C Register (PMFFQCC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set.

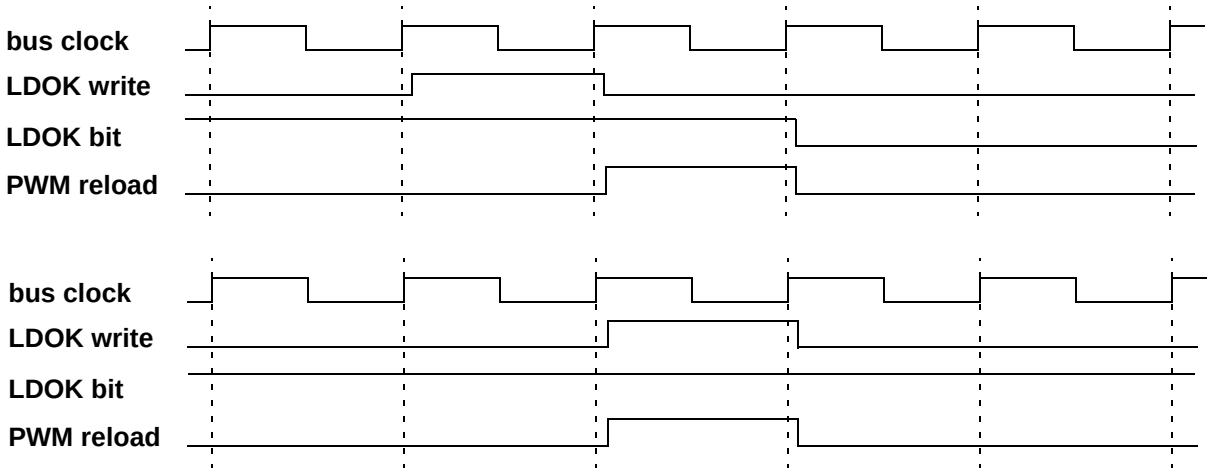


Figure 15-72. Setting asserted LDOK bit at PWM reload event

15.4.12.2 Global Load Enable

If a global load enable bit GLDOKA, B, or C is set, the global load OK bit defined on device level as input to the PMF replaces the function of the related local LDOKA, B, or C bits. The global load OK signal is typically shared between multiple IP blocks with the same double buffer scheme. Software handling must be transferred to the global load OK bit at the chip level.

15.4.12.3 Load Frequency

The LDFQ3, LDFQ2, LDFQ1, and LDFQ0 bits in the PWM control register (PMFFQCx) select an integral loading frequency of 1 to 16-PWM reload opportunities. The LDFQ bits take effect at every PWM reload opportunity, regardless the state of the related load okay bit or global load OK. The *half* bit in the PMFFQC register controls half-cycle reloads for center-aligned PWMs. If the *half* bit is set, a reload opportunity occurs at the beginning of every PWM cycle and half cycle when the count equals the modulus. If the half bit is not set, a reload opportunity occurs only at the beginning of every cycle. Reload opportunities can only occur at the beginning of a PWM cycle in edge-aligned mode.

NOTE

Setting the half bit takes effect immediately. Depending on whether the counter is incrementing or decrementing at this point in time, reloads at even-numbered reload frequencies (every 2, 4, 6,... reload opportunities) will occur only when the counter matches the modulus or only when the counter equals zero, respectively (refer to example of reloading at every two opportunities in Figure 15-74).

NOTE

Loading a new modulus on a half cycle will force the count to the new modulus value minus one on the next clock cycle. Half cycle reloads are possible only in center-aligned mode. Enabling or disabling half-cycle reloads in edge-aligned mode will have no effect on the reload rate.

17.4.7.5.2 SPIF

SPIF occurs when new data has been received and copied to the SPI data register. After SPIF is set, it does not clear until it is serviced. SPIF has an automatic clearing process, which is described in Section 17.3.2.4, “SPI Status Register (SPISR)”.

17.4.7.5.3 SPTEF

SPTEF occurs when the SPI data register is ready to accept new data. After SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process, which is described in Section 17.3.2.4, “SPI Status Register (SPISR)”.

Chapter 18
Gate Drive Unit (GDU)

Table 18-1. Revision History Table

Version Number	Revision Date	Description of Changes
V6 Initial Draft	25-January-2015	Initial Draft based on GDUV4/V5 with following changes for SR Motor support: • additional drain connections LD[2:0] for SR motor drive • GDUCTR1 register with control bits for SR motor drive • Removed EPRES control bit functionality for V5 and V6 • Changed GSUF startup flag functionality for V6
V6	28-January-2016	• Removed EPRES Functionality • Common specification for GSUF with reference to device overview • Common specification for GDUCTR1 with reference to device overview
V6.1	4-February-2016	• Corrected Table 1-2 TDEL availability and low-side driver on or off out of reset dependent on NVM option for GDU V4
V6.2	17-May-2016	• Removed desaturation comparator level and desaturation comparator filter time constant (relocated in electrical spec.)
V6.2	17-May-2016	• Removed desaturation comparator level and desaturation

18.1 Differences GDUV4 vs GDUV5 vs GDUV6

Table 18-2. GDUV4/V5/V6 Differences(1)

Feature	GDU V4	GDU V5	GDU V6
TDEL control bit for t_{delon}/t_{deloff}	available[1.]	not available	available
Number of Overcurrent threshold bits for overcurrent comparator 0/1	GOCT0[3:0] , GOCT1[3:0]	GOCT0[4:0] , GOCT1[4:0]	GOCT0[4:0], GOCT1[4:0]
VLS level select control bit GVLSLVL	not available	available	available
Current sense amplifier offset	adjustable in 5mV steps	adjustable in 3mV steps	adjustable in 3mV steps

Table 20-31. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x01	Erase Verify All Blocks	Verify that all EEPROM (and P-Flash) blocks are erased.
0x02	Erase Verify Block	Verify that the EEPROM block is erased.
0x08	Erase All Blocks	Erase all EEPROM (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the DFPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a EEPROM (or P-Flash) block. An erase of the full EEPROM block is only possible when DPOPEN bit in the DFPROT register is set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all EEPROM (and P-Flash) blocks and verifying that all EEPROM (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the EEPROM block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the EEPROM block (special modes only).
0x10	Erase Verify EEPROM Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program EEPROM	Program up to four words in the EEPROM block.
0x12	Erase EEPROM Sector	Erase all bytes in a sector of the EEPROM block.
0x13	Protection Override	Supports a mode to temporarily override Protection configuration (for P-Flash and/or EEPROM) by verifying a key.

20.4.6 Allowed Simultaneous P-Flash and EEPROM Operations

Only the operations marked ‘OK’ in Table 20-32 are permitted to be run simultaneously on Program Flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the EEPROM, providing read (P-Flash) while write (EEPROM) functionality. Any attempt to access P-Flash and EEPROM simultaneously when it is not allowed will result in an illegal access that will trigger a machine exception in the CPU (see device information for details). Please note that during the execution of each command there is a period, before the operation in the Flash array actually starts, where reading is allowed and valid data is returned. Even if the simultaneous operation is marked as not allowed the Flash will report an illegal access only in the cycle the read collision actually happens, maximizing the time the array is available for reading.

If more than one hardblock exists on a device, then read operations on one hardblock are permitted whilst program or erase operations are executed on the other hardblock.

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 22.4.2.5, “Left Aligned Outputs” and Section 22.4.2.6, “Center Aligned Outputs” for more details).

Table 22-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

22.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 22-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 22-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 22.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

Table A-18. Run and Wait Current Characteristics

Conditions see Table A-16 and Table A-17, V_{SUP}=18 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Run Current, -40°C < TJ < 150°C, fbus= 50MHz ZVMC256 Other devices	I_{SUPR}	— —	56 53	70 66	mA
2		Wait Current, -40°C < TJ < 150°C, fbus= 50MHz ZVMC256 Other devices	I_{SUPW}	— —	50 42	66 55	mA
3		Run Current, TJ =175°C, fbus= 40MHz ZVMC256 Other devices	I_{SUPR}	— —	50 45	66 55	mA
4		Wait Current, TJ = 175°C, fbus= 40MHz ZVMC256 Other devices	I_{SUPW}	— —	40 36	56 45	mA

Table A-19. Stop Current Characteristics

Conditions are: V_{SUP}=12 V[1] [2]							
Num	**C**	**Rating[3]**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Stop Current all modules off							
1		TA = TJ= -40°C ZVMC256 Other devices	I_{SUPS}	— —	25 20	40 35	μA
2		$T_A = T_J$= 150°C ZVMC256 Other devices	I_{SUPS}	— —	600 350	2400 1050	μA
3		$T_A = T_J$ = 25°C ZVMC256 Other devices	I_{SUPS}	— —	27 25	95 40	μA
4		$T_A = T_J$ = 85°C ZVMC256 Other devices	I_{SUPS}	— —	120 95	250 —	μA
5		$T_A = T_J$ = 105°C ZVMC256 Other devices	I_{SUPS}	— —	140 105	600 250	μA
Stop Current API enabled & LINPHY in standby (only for devices featuring LINPHY)							
6		$T_A = T_J$ = 25°C	I_{SUPS}	—	35	45	μA
Stop Current API enabled & CANPHY in standby (only for devices featuring CANPHY)							
7		$T_A = T_J$ = 25°C	I_{SUPS}	—	50	—	μA

1. This is the total current flowing into the VSUP and HD pins, to account for mask sets where HD is the LINPHY supply.

2. Stop current values for ZVMC256 are subject to change following characterization.

3. If MCU is in Stop mode long enough then TA = TJ . Die self heating due to stop current can be ignored.

C.1.2 ADC Accuracy

Table C-3. specifies the ADC conversion performance excluding any errors due to current injection, input capacitance and source resistance.

C.1.2.1 ADC Accuracy Definitions

For the following definitions see also **Figure C-2.**.
Differential non-linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The integral non-linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

Appendix I
SPI Electrical Specifications

This section provides electrical parametrics and ratings for the SPI.

In **Figure I-1.** the measurement conditions are listed.

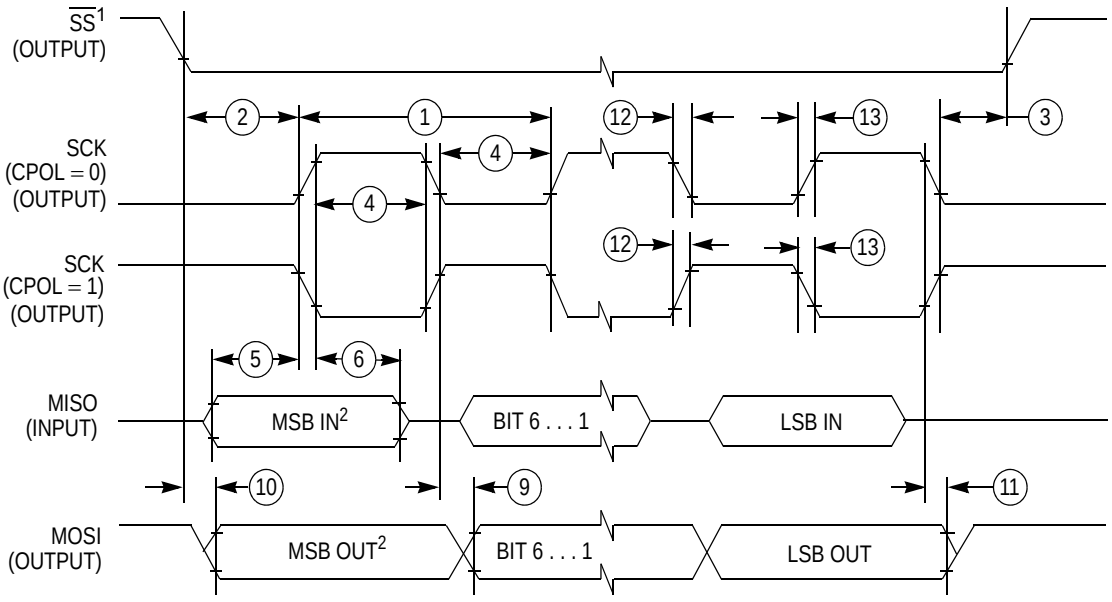
Figure I-1. Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}[(1)], on all outputs	50	pF
Thresholds for delay measurement points	(35% / 65%) VDDX	V

1. Timing specified for equal load on all SPI output pins. Avoid asymmetric load.

I.1 Master Mode

In **Figure I-2.** the timing diagram for master mode with transmission format CPHA=0 is depicted.



1. If enabled.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-2. SPI Master Timing (CPHA=0)

In **Figure I-3.** the timing diagram for master mode with transmission format CPHA=1 is depicted.

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		PAGE: 2139
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 4.9 X 4.9 EXPOSED PAD	CASE NUMBER: 2139–01	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: IN AGILE	SHEET: 3 OF 4

M.6 0x0380-0x039F FTMRZ128K512 (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0384	FCNFG	R	CCIE	0	ERSAREQ	IGNSF	WSTAT[1:0]		FDFD	FSFD
		W								
0x0385	FERCNFG	R	0	0	0	0	0	0	0	SFDIE
		W								
0x0386	FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
		W								
0x0387	FERSTAT	R	0	0	0	0	0	0	DFDF	SFDIF
		W								
0x0388	FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		W								
0x0389	DFPROT	R	DPOPEN	0	0	0	DPS3	DPS2	DPS1	DPS0
		W								
0x038A	FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
		W								
0x038B	FRSV1	R	0	0	0	0	0	0	0	0
		W								
0x038C	FCCOB0HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x038D	FCCOB0LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x038E	FCCOB1HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x038F	FCCOB1LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0390	FCCOB2HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0391	FCCOB2LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0392	FCCOB3HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0393	FCCOB3LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0394	FCCOB4HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0395	FCCOB4LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								