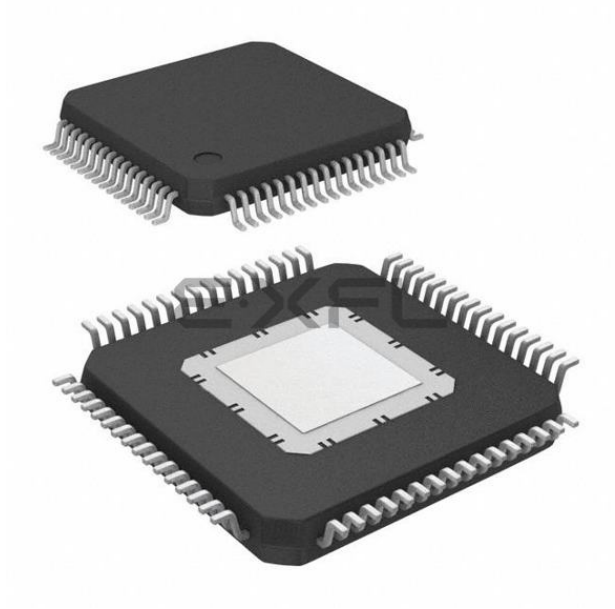

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f3wkh

Chapter 2
Port Integration Module (S12ZVMPIMV3)

1.2.3 Functional Differences Between Masksets

The parts ZVML128, ZVMC128, ZVML64, ZVMC64 and ZVML32 have the following mask set options.

Table 1-19

Table 1-4. N95G Option Table

Feature	0N95G[1]	1N95G	2N95G	3N95G
LINPHY supply pin	HD	HD	VSUP	HD
BST pin function available	Yes	Yes	No	Yes
GDU low side driver state in HD over-voltage case	on	GOCA1	GOCA1	GOCA1

1. 0N95G is not a production mask set

1.3 Chip-Level Features

On-chip modules available within the family include the following features:

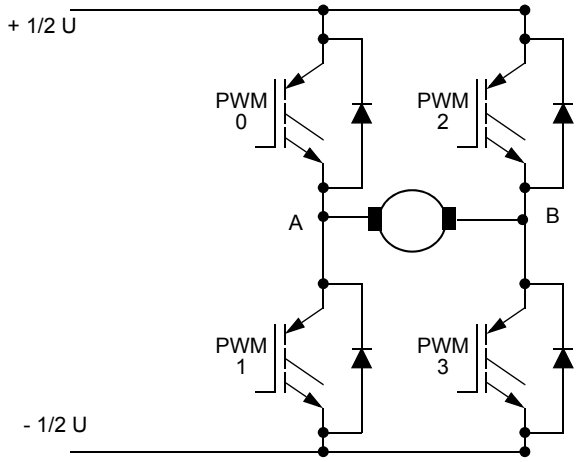
- S12Z CPU core
- 256, 128, 64, 32 or 16KB on-chip flash with ECC
- 1K, 512 or 128 byte EEPROM with ECC
- 32, 8, 4 or 2 KB on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range
- 4-20MHz amplitude controlled pierce oscillator
- Internal COP (watchdog) module
- 6-channel, 15-bit pulse width modulator with fault protection (PMF)
- Low side and high side FET pre-drivers for each phase
  - Gate drive pre-regulator
  - LDO (Low Dropout Voltage Regulator) (typically 11V)
  - High side gate supply generated using bootstrap circuit with external diode and capacitor
  - Sustaining charge pump with two external capacitors and diodes
  - High side drain (HD) monitoring on internal ADC channel using HD/5 voltage
- Two parallel analog-to-digital converters (ADC) with 12-bit resolution and up to 16 channels available on external pins
- Programmable Trigger Unit (PTU) for synchronization of PMF and ADC
- One serial peripheral interface (SPI) module
- One serial communication interface (SCI) module with interface to internal LIN physical layer transceiver (with RX connected to a timer channel for frequency calibration purposes, if desired)

Table 1-9. Pin Summary For 80-Pin Package Option (ZVMC256 Only) (Sheet 2 of 5)

Pin #	Pin Name	Function (Priority and routing options defined in PIM chapter)							Supply	Internal Pull Resistor	
		1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.		CTRL	Reset State
11	BCTLS 1	—	—	—	—	—	—		—	—	—
12	VDDS1	VRH0_1	VRH1_1	—	—	—	—		—	—	—
13	SNPS2	—	—	—	—	—	—		—	—	—
14	BCTLS 2	—	—	—	—	—	—		—	—	—
15	VDDS2	VRH0_2	VRH1_2	—	—	—	—		—	—	—
16	LD0	—	—	—	—	—	—		—	—	—
17	LD1	—	—	—	—	—	—		—	—	—
18	LD2	—	—	—	—	—	—		—	—	—
19	PAD0	KWAD0	AN0_0	AMP0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
20	PAD1	KWAD1	AN0_1	AMPM0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
21	PAD2	KWAD2	AN0_2	AMPP0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
22	PAD3	KWAD3	AN0_3	—	—	—	—		V_{DDA}	PERADL/PPSADL	Off
23	PAD4	KWAD4	AN0_4	—	—	—	—		V_{DDA}	PERADL/PPSADL	Off
24	PAD5	KWAD5	AN1_0	AMP1	—	—	—		V_{DDA}	PERADL/PPSADL	Off
25	PAD6	KWAD6	AN1_1	$\overline{SS0}$	AMPM1	—	—		V_{DDA}	PERADL/PPSADL	Off
26	PAD7	KWAD7	AN1_2	AMPP1	—	—	—		V_{DDA}	PERADL/PPSADL	Off
27	PAD8	KWAD8	AN1_3	—	—	—	—		V_{DDA}	PERADH/PPSADH	Off

The DC Brushed motor power stage topology is a classical full bridge as shown in Figure 1-11. The DC Brushed motor is driven by the DC voltage source. A rotational field is created by means of commutator and brushes on the motor. These drives are still very popular because sophisticated calculations and algorithms such as commutation, waveform generation, or space vector modulation are not required.

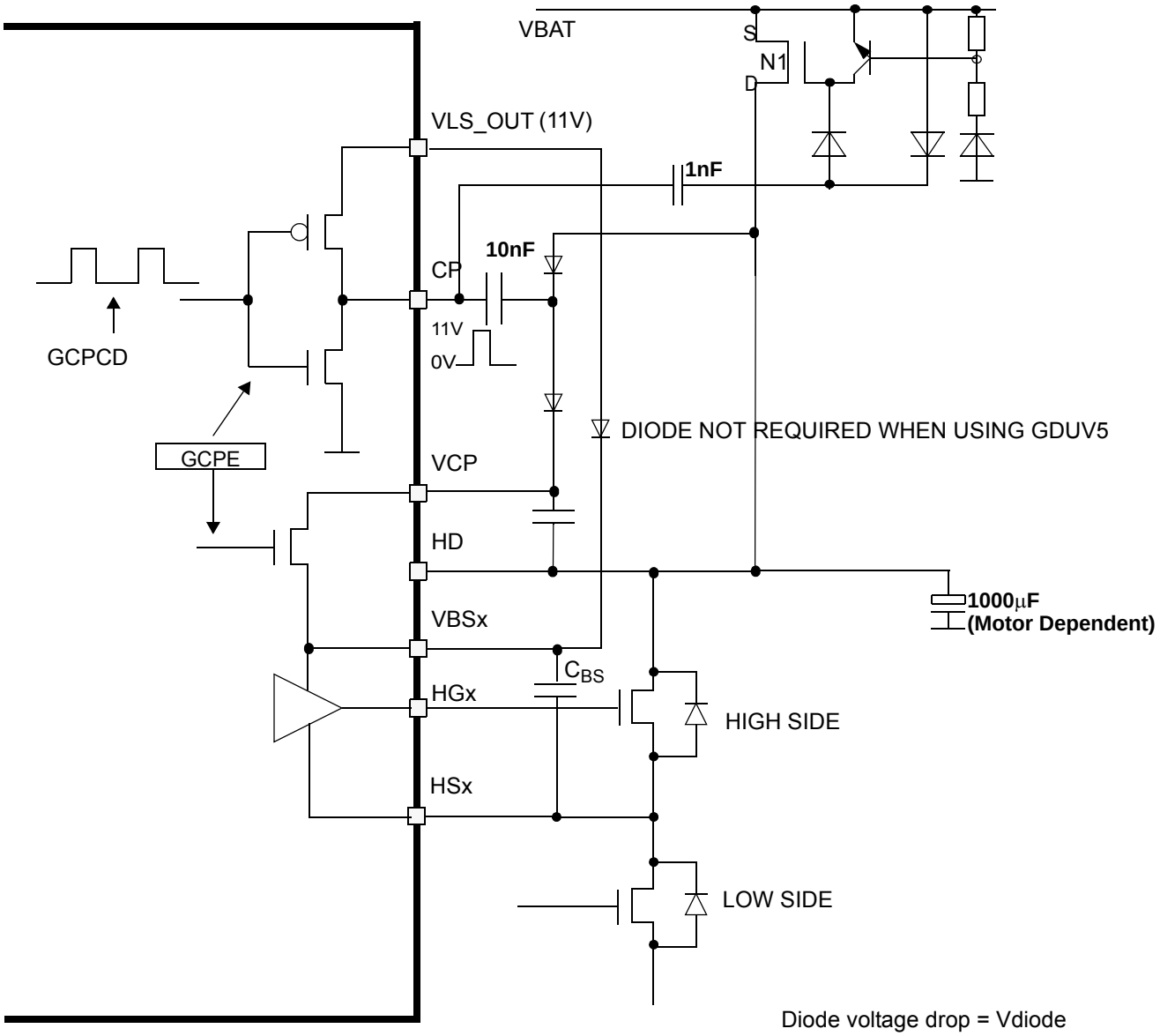
Figure 1-11. DC Brushed Motor External Configuration



Usually the control consists of an outer, speed control loop with inner current (torque) control loop. The inner loop controls DC voltage applied onto the motor winding. The control loop is calculated regularly within a given period. In most cases, this period matches the PWM reload period.

Driving the DC motor from a DC voltage source, the motor can work in all four quadrants. The complementary mode of operation with deadtime insertion is needed for smooth reversal of the motor

Figure 1-20. High Side Supply and Charge Pump Concept



External pulldown device (Figure 2-38):

1. Enable analog function on HVI in non-direct mode (PTAENL[PTAENL0]=1, PTAENL[PTADIRL0]=0)
2. Select internal pullup device on HVI (PTPSL[PTPSL0]=1)
3. Enable function to force input buffer active on HVI in analog mode (PTTEL[PTTEL0]=1)
4. Verify PTIL=0 for a connected external pulldown device; read PTIL=1 for an open input

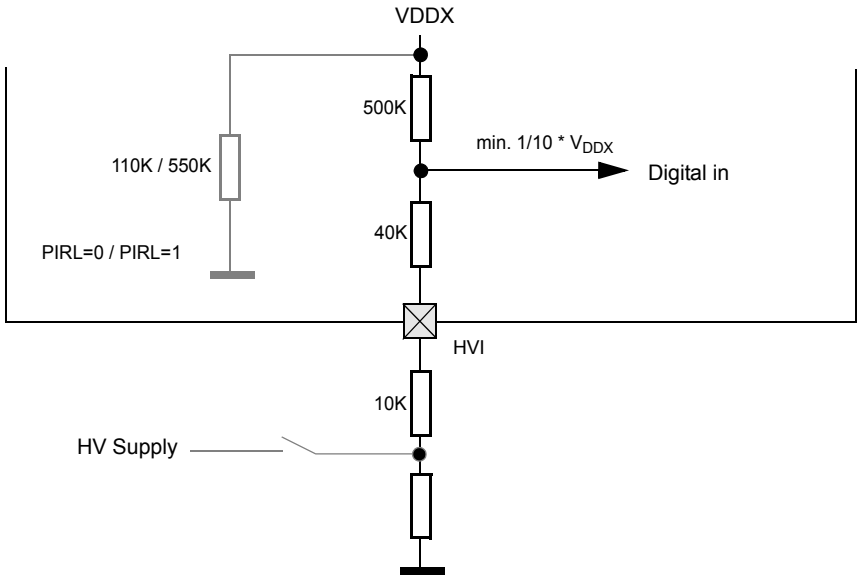


Figure 2-38. Digital Input Read with Pullup Enabled

External pullup device (Figure 2-39):

1. Enable analog function on HVI in non-direct mode (PTAENL[PTAENL0]=1, PTADIRL[PTADIRL0]=0)
2. Select internal pulldown device on HVI (PTPSL[PTPSL0]=0)
3. Enable function to force input buffer active on HVI in analog mode (PTTEL[PTTEL0]=1)
4. Verify PTIL0=1 for a connected external pullup device; read PTIL0=0 for an open input

- All illegal accesses performed by an ADC or PTU module trigger error interrupts. See ADC and PTU section for details.

NOTE

Illegal accesses caused by S12ZCPU opcode prefetches will also trigger machine exceptions, even if those opcodes might not be executed in the program flow. To avoid these machine exceptions, S12ZCPU instructions must not be executed from the last (high addresses) 8 bytes of RAM, EEPROM, and Flash.

3.4.3 Uncorrectable ECC Faults

RAM and flash use error correction codes (ECC) to detect and correct memory corruption. Each uncorrectable memory corruption, which is detected during a S12ZCPU, ADC or PTU access triggers a machine exception. Uncorrectable memory corruptions which are detected during a S12ZBDC access, are captured in the RAMWF or the RDINV bit of the BDCCSRL register.

- Initialize the interrupt processing level configuration data registers (INT_CFADDR, INT_CFDATA0–7) for all interrupt vector requests with the desired priority levels. It might be a good idea to disable unused interrupt requests.
- Enable I-bit maskable interrupts by clearing the I-bit in the CCW.
- Enable the X-bit maskable interrupt by clearing the X-bit in the CCW (if required).

4.5.2 Interrupt Nesting

The interrupt request priority level scheme makes it possible to implement priority based interrupt request nesting for the I-bit maskable interrupt requests.

- I-bit maskable interrupt requests can be interrupted by an interrupt request with a higher priority, so that there can be up to seven nested I-bit maskable interrupt requests at a time (refer to Figure 4-14 for an example using up to three nested interrupt requests).

I-bit maskable interrupt requests cannot be interrupted by other I-bit maskable interrupt requests per default. In order to make an interrupt service routine (ISR) interruptible, the ISR must explicitly clear the I-bit in the CCW (CLI). After clearing the I-bit, I-bit maskable interrupt requests with higher priority can interrupt the current ISR.

An ISR of an interruptible I-bit maskable interrupt request could basically look like this:

- Service interrupt, e.g., clear interrupt flags, copy data, etc.
- Clear I-bit in the CCW by executing the CPU instruction CLI (thus allowing interrupt requests with higher priority)
- Process data
- Return from interrupt by executing the instruction RTI

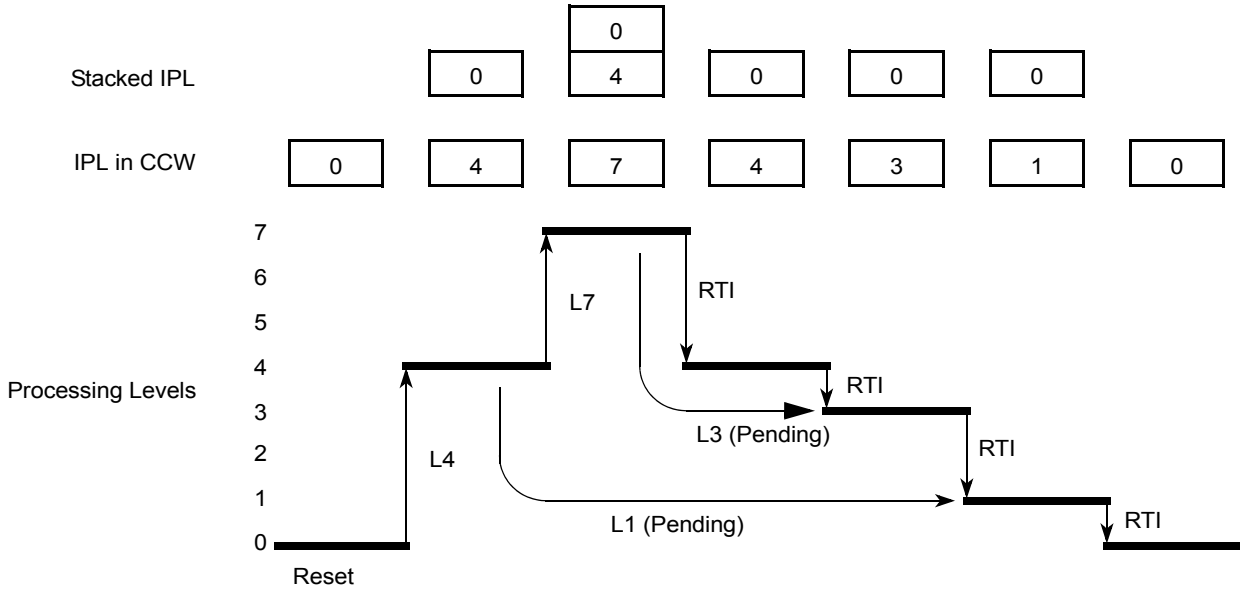


Figure 4-14. Interrupt Processing Example

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0128-0x012F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0130	DBGCCTL	R	0	NDB	INST	0	RW	RWE	reserved	COMPE
		W								
0x0131-0x0134	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0135	DBGCAH	R	DBGCA[23:16]							
		W								
0x0136	DBGCAM	R	DBGCA[15:8]							
		W								
0x0137	DBGCAL	R	DBGCA[7:0]							
		W								
0x0138	DBGCD0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x0139	DBGCD1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013A	DBGCD2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013B	DBGCD3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x013C	DBGCDM0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x013D	DBGCDM1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013E	DBGCDM2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013F	DBGCDM3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								

Figure 6-2. Quick Reference to DBG Registers

8.3.2.22 High Temperature Trimming Register (CPMUHTTR)

The CPMUHTTR register configures the trimming of the S12CPMU_UHV_V10_V6 temperature sense.

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	F	F	F	F

After de-assert of System Reset a trim value is automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 8-30. High Temperature Trimming Register (CPMUHTTR)

Read: Anytime

Write: Anytime

Table 8-25. CPMUHTTR Field Descriptions

Field	Description
7 HTOE	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled. 0 The temperature sense offset is disabled. HTTR[3:0] bits don't care. 1 The temperature sense offset is enabled. HTTR[3:0] select the temperature offset.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 8-26 for trimming effects.

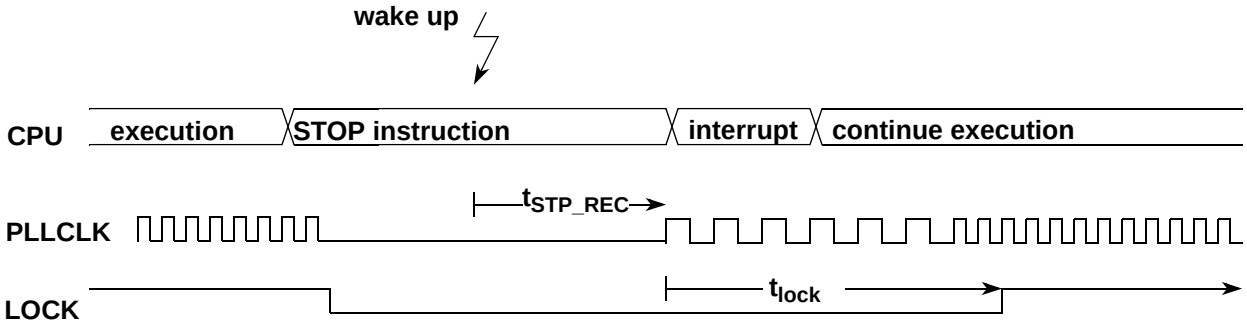
Table 8-26. Trimming Effect of HTTR

HTTR[3:0]	Temperature sensor voltage V_{HT}	Interrupt threshold temperatures T_{HTIA} and T_{HTID}
0000	lowest	highest
0001	increasing	decreasing
....		
1110		
1111	highest	lowest

8.4.3 Stop Mode using PLLCLK as source of the Bus Clock

An example of what happens going into Stop Mode and exiting Stop Mode after an interrupt is shown in Figure 8-42. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop Mode.

Figure 8-42. Stop Mode using PLLCLK as source of the Bus Clock



Depending on the COP configuration there might be an additional significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

8.4.4 Full Stop Mode using Oscillator Clock as source of the Bus Clock

An example of what happens going into Full Stop Mode and exiting Full Stop Mode after an interrupt is shown in Figure 8-43.

Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop Mode.

15.3.2.17 PMF Internal Correction Control Register (PMFICCTL)

Address: Module Base + 0x001E

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	PECC	PECB	PECA	ICCC	ICCB	ICCA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-20. PMF Internal Correction Control Register (PMFICCTL)

1. Read: Anytime
   Write: Anytime

This register is used to control PWM pulse generation for various applications, such as a power-supply phase-shifting application.

ICC*x* bits apply only in center-aligned operation during complementary mode. These control bits determine whether values set in the IPOL*x* bits control or the whether PWM count direction controls which PWM value register is used.

NOTE

The ICC*x* bits are buffered. The value written does not take effect until the next PWM load cycle begins regardless of the state of the LDOK bit or global load OK. Reading ICC*x* returns the value in a buffer and not necessarily the value the PWM generator is currently using.

The PEC*x* bits apply in edge-aligned and center-aligned operation during complementary mode. Setting the PEC*x* bits overrides the ICC*x* settings. This allows the PWM pulses generated by both the odd and even PWM value registers to be ANDed together prior to the complementary logic and deadtime insertion.

NOTE

The PEC*x* bits are buffered. The value written does not take effect until the related LDOK bit or global load OK is set and the next PWM load cycle begins. Reading PEC*n* returns the value in a buffer and not necessarily the value the PWM generator is currently using.

Figure 15-21. PMF Internal Correction Control Register (PMFICCTL) Descriptions

Field	Description
5 PECC	Pulse Edge Control — This bit controls PWM4/PWM5 pair. 0 Normal operation 1 Allow one of PMFVAL4 and PMFVAL5 to activate the PWM pulse and the other to deactivate the pulse
4 PECB	Pulse Edge Control — This bit controls PWM2/PWM3 pair. 0 Normal operation 1 Allow one of PMFVAL2 and PMFVAL3 to activate the PWM pulse and the other to deactivate the pulse
3 PECA	Pulse Edge Control — This bit controls PWM0/PWM1 pair. 0 Normal operation 1 Allow one of PMFVAL0 and PMFVAL1 to activate the PWM pulse and the other to deactivate the pulse

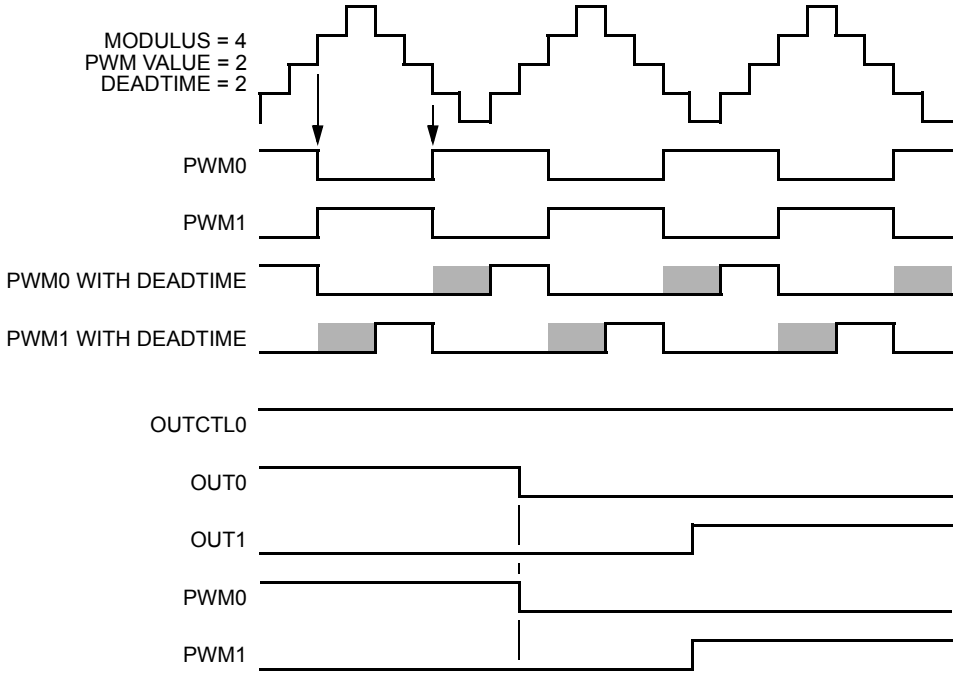


Figure 15-69. Clearing OUT0 with OUTCTL Set in Complementary Mode

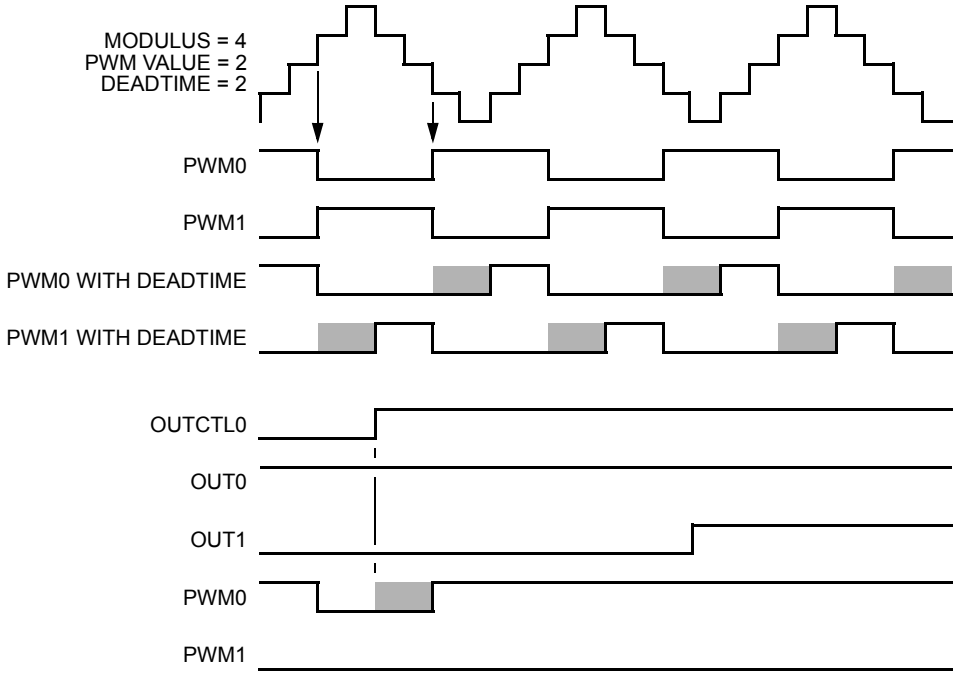


Figure 15-70. Setting OUTCTL with OUT0 Set in Complementary Mode

17.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

17.2.3 $\overline{SS}$ — Slave Select Pin

This pin is used to output the select signal from the SPI module to another peripheral with which a data transfer is to take place when it is configured as a master and it is used as an input to receive the slave select signal when the SPI is configured as slave.

17.2.4 SCK — Serial Clock Pin

In master mode, this is the synchronous output clock. In slave mode, this is the synchronous input clock.

17.3 Memory Map and Register Definition

This section provides a detailed description of address space and registers used by the SPI.

17.3.1 Module Memory Map

The memory map for the SPI is given in Figure 17-2. The address listed for each register is the sum of a base address and an address offset. The base address is defined at the SoC level and the address offset is defined at the module level. Reads from the reserved bits return zeros and writes to the reserved bits have no effect.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
	W								
0x0001 SPICR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
	W								
0x0002 SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
	W								
0x0003 SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
	W								
0x0004 SPIDRH	R	R15	R14	R13	R12	R11	R10	R9	R8
	W	T15	T14	T13	T12	T11	T10	T9	T8
0x0005 SPIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0
0x0006 Reserved	R								
	W								

= Unimplemented or Reserved

Figure 17-2. SPI Register Summary

As long as no more than one slave device drives the system slave's serial data output line, it is possible for several slaves to receive the same transmission from a master, although the master would not receive return information from all of the receiving slaves.

If the CPHA bit in SPI control register 1 is clear, odd numbered edges on the SCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

If the CPHA bit is set, even numbered edges on the SCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

When CPHA is set, the first edge is used to get the first data bit onto the serial data output pin. When CPHA is clear and the $\overline{SS}$ input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the nth[1] shift, the transfer is considered complete and the received data is transferred into the SPI data register. To indicate transfer is complete, the SPIF flag in the SPI status register is set.

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, MODFEN, SPC0, or BIDIROE with SPC0 set in slave mode will corrupt a transmission in progress and must be avoided.

17.4.3 Transmission Formats

During an SPI transmission, data is transmitted (shifted out serially) and received (shifted in serially) simultaneously. The serial clock (SCK) synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows selection of an individual slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. Optionally, on a master SPI device, the slave select line can be used to indicate multiple-master bus contention.

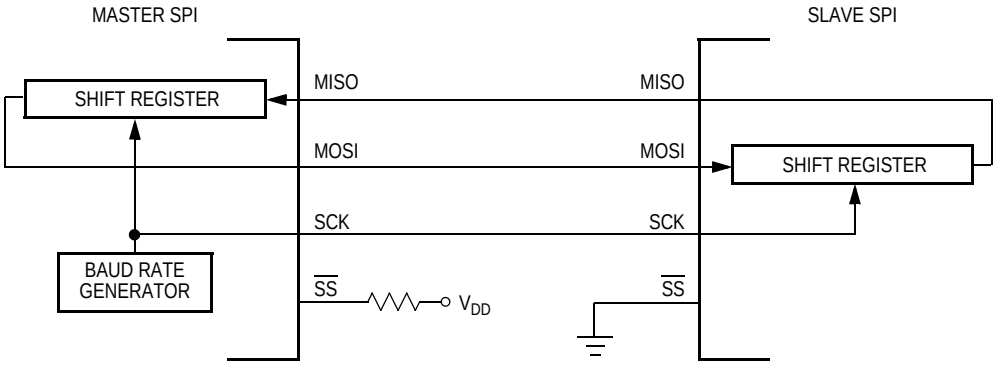


Figure 17-11. Master/Slave Transfer Block Diagram

17.4.3.1 Clock Phase and Polarity Controls

Using two bits in the SPI control register 1, software selects one of four combinations of serial clock phase and polarity.

1. n depends on the selected transfer width, please refer to Section 17.3.2.2, "SPI Control Register 2 (SPICR2)

18.3.2.9 GDU Boost Current Limit Register (GDUBCL)

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	GBCL[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-11. GDU Boost Current Limit Register (GDUBCL)

1. Read: Anytime
   Write: Anytime if GWP=0

Table 18-12. GDU Boost Current Limit Register Field Descriptions

Field	Description
GBCL[3:0]	GDU Boost Current Limit Register— These bits are used to adjust the boost coil current limit $I_{COIL0,16}$ on the BST pin. These bits cannot be modified after GWP bit is set. See GDU electrical parameters.

18.3.2.10 GDU Phase Mux Register (GDUPHMUX)

Module Base + 0x0009 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	GPHMX[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-12. GDU Phase Mux Register (GDUPHMUX)

1. Read: Anytime
   Write: Anytime

Table 18-13. GDU Phase Mux Register Field Descriptions

Field	Description
[1:0] GPHMUX	GDU Phase Multiplexer — These buffered bits are used to select the voltage which is routed to internal ADC channel.The value written to the GDUPHMUX register does not take effect until the LDOK bit is set and the next PWM reload cycle begins. Reading GDUPHMUX register reads the value in the buffer. It is not necessary the value which is currently used. 00 Pin HD selected , V_{HD} / 12 connected to ADC channel 01 Pin HS0 selected , V_{HS0} / 6 connected to ADC channel 10 Pin HS1 selected , V_{HS1} / 6 connected to ADC channel 11 Pin HS2 selected, V_{HS2} / 6 connected to ADC channel

Table 20-17. FSTAT Field Descriptions (continued)

Field	Description
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. The MGSTAT bits are cleared automatically at the start of the execution of a Flash command. See Section 20.4.7, “Flash Command Description,” and Section 20.6, “Initialization” for details.

20.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Offset Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 20-18. FERSTAT Field Descriptions

Field	Description
1 DFDF	**Double Bit Fault Detect Flag** — The setting of the DFDF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.(1) The DFDF flag is cleared by writing a 1 to DFDF. Writing a 0 to DFDF has no effect on DFDF.(2) 0 No double bit fault detected 1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running. See Section 20.4.3, “Flash Block Read Access” for details
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation. The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted while command running

1. In case of ECC errors the corresponding flag must be cleared for the proper setting of any further error, i.e. any new error will only be indicated properly when DFDF and/or SFDIF are clear at the time the error condition is detected.

2. There is a one cycle delay in storing the ECC DFDF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

Module Base + 0x00006

	7	6	5	4	3	2	1	0
R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
Reset	0	0	0	0	0	0	0	0

Figure 22-9. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLKAB0 to PCLKAB7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 22-11. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PCLKAB7	Pulse Width Channel 7 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 7, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 7, as shown in Table 22-6.
6 PCLKAB6	Pulse Width Channel 6 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 6, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 6, as shown in Table 22-6.
5 PCLKAB5	Pulse Width Channel 5 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 5, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 5, as shown in Table 22-5.
4 PCLKAB4	Pulse Width Channel 4 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 4, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 4, as shown in Table 22-5.
3 PCLKAB3	Pulse Width Channel 3 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 3, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 3, as shown in Table 22-6.
2 PCLKAB2	Pulse Width Channel 2 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 2, as shown in Table 22-6. 1 Clock A or SA is the clock source for PWM channel 2, as shown in Table 22-6.
1 PCLKAB1	Pulse Width Channel 1 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 1, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 1, as shown in Table 22-5.
0 PCLKAB0	Pulse Width Channel 0 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 0, as shown in Table 22-5. 1 Clock B or SB is the clock source for PWM channel 0, as shown in Table 22-5.

Table A-20. Pseudo Stop Current Characteristics

Conditions are: V_{SUP}=12V, API, COP & RTI enabled							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		T_J = 25°C ZVMC256 Other devices	I_{SUPPS}	 — —	 430 265	 660 300	µA

A.4 ADC Calibration Configuration

The reference voltage V_{BG} is measured under the conditions shown in Table A-21. The values stored in the IFR are the average of eight consecutive conversions at Tj=150 °C and eight consecutive conversions at Tj=-40 °C. The code is executed from RAM. The result is programmed to the IFR, otherwise there is no flash activity.

Table A-21. Measurement Conditions

Description	Symbol	Value	Unit
Regulator Supply Voltage at VSUP	V_{SUP}	5	V
Supply Voltage at VDDX and VDDA	$V_{DDX,A}$	5	V
ADC reference voltage high	V_{RH}	5	V
ADC reference voltage low	V_{RL}	0	V
ADC clock	f_{ATDCLK}	2	MHz
ADC sample time	t_{SMP}	4	ADC clock cycles
Bus clock frequency	f_{bus}	48	MHz
Junction temperature	T_j	-40 and 150	°C

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0529	PMFFQCB	R	LDFQB				HALFB	PRSCB		PWMRFB
		W								
0x052A	PMFCNTB	R	0	PMFCNTB						
		W								
0x052B	PMFCNTB	R	PMFCNTB							
		W								
0x052C	PMFMODB	R	0	PMFMODB						
		W								
0x052D	PMFMODB	R	PMFMODB							
		W								
0x052E	PMFDTMB	R	0	0	0	0	PMFDTMB			
		W								
0x052F	PMFDTMB	R	PMFDTMB							
		W								
0x0530	PMFENCC	R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
		W								
0x0531	PMFFQCC	R	LDFQC				HALFC	PRSCC		PWMRFC
		W								
0x0532	PMFCNTC	R	0	PMFCNTC						
		W								
0x0533	PMFCNTC	R	PMFCNTC							
		W								
0x0534	PMFMODC	R	0	PMFMODC						
		W								
0x0535	PMFMODC	R	PMFMODC							
		W								
0x0536	PMFDTMC	R	0	0	0	0	PMFDTMC			
		W								
0x0537	PMFDTMC	R	PMFDTMC							
		W								
0x0538	PMFDMP0	R	DMP05		DMP04		DMP03	DMP02	DMP01	DMP00
		W								
0x0539	PMFDMP1	R	DMP15		DMP14		DMP13	DMP12	DMP11	DMP10
		W								