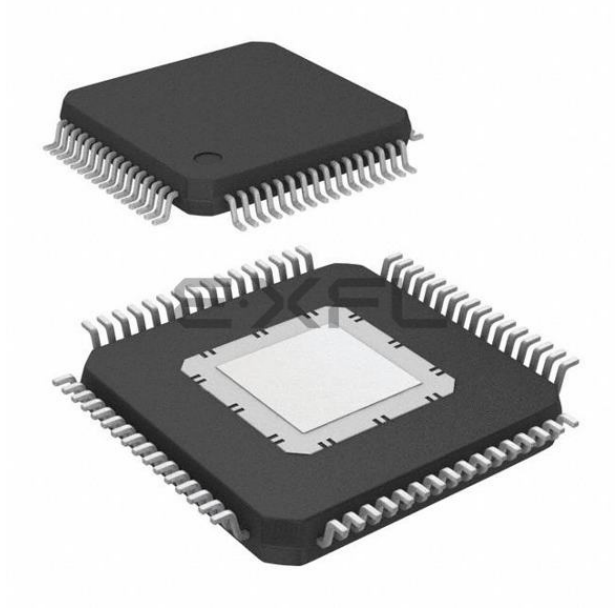

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Details	
Product Status	Active
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Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml12f3wkhr

1.7.2.3 MODC — Mode C Signal

The MODC signal is used as an MCU operating mode select during reset. The state of this signal is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The signal has an internal pull-up device.

1.7.2.4 PAD[15:0] / KWAD[15:0] — Port AD, Input Pins of ADC

These are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWAD). These signals can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are disabled.

1.7.2.5 PE[1:0] — Port E I/O Signals

PE[1:0] are general-purpose input or output signals. The signals can have a pull-down device, enabled by on a per pin basis. Out of reset the pull-down devices are enabled.

1.7.2.6 PL[0] — Port L Input Signal

PL[0] is a high voltage input port. The port can be configured as interrupt input with wake-up capability (KWL[0]). The input voltage is also scaled and mapped to an internal ADC channel.

1.7.2.7 PP[2:0] / KWP[2:0] — Port P I/O Signals

PP[2:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWP[2:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are disabled.

1.7.2.8 PS[5:0] / KWS[5:0] — Port S I/O Signals

PS[5:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWS[5:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull-up devices are enabled.

1.7.2.9 PT[3:0] — Port T I/O Signals

PT[3:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are disabled.

1.7.2.10 AN0_[7:0], AN1_[7:0]— ADC Input Signals

These are the analog inputs of the Analog-to-Digital Converters. These are mapped to PAD port pins. The number of analog input channels connected to PAD port pins is package option dependent.

1.7.2.11 VRH0_[2:0], VRL0_[1:0] — ADC0 Reference Signals

VRH0_[2:0] and VRL0_[1:0] are the reference voltage signals for the analog-to-digital converter ADC0.

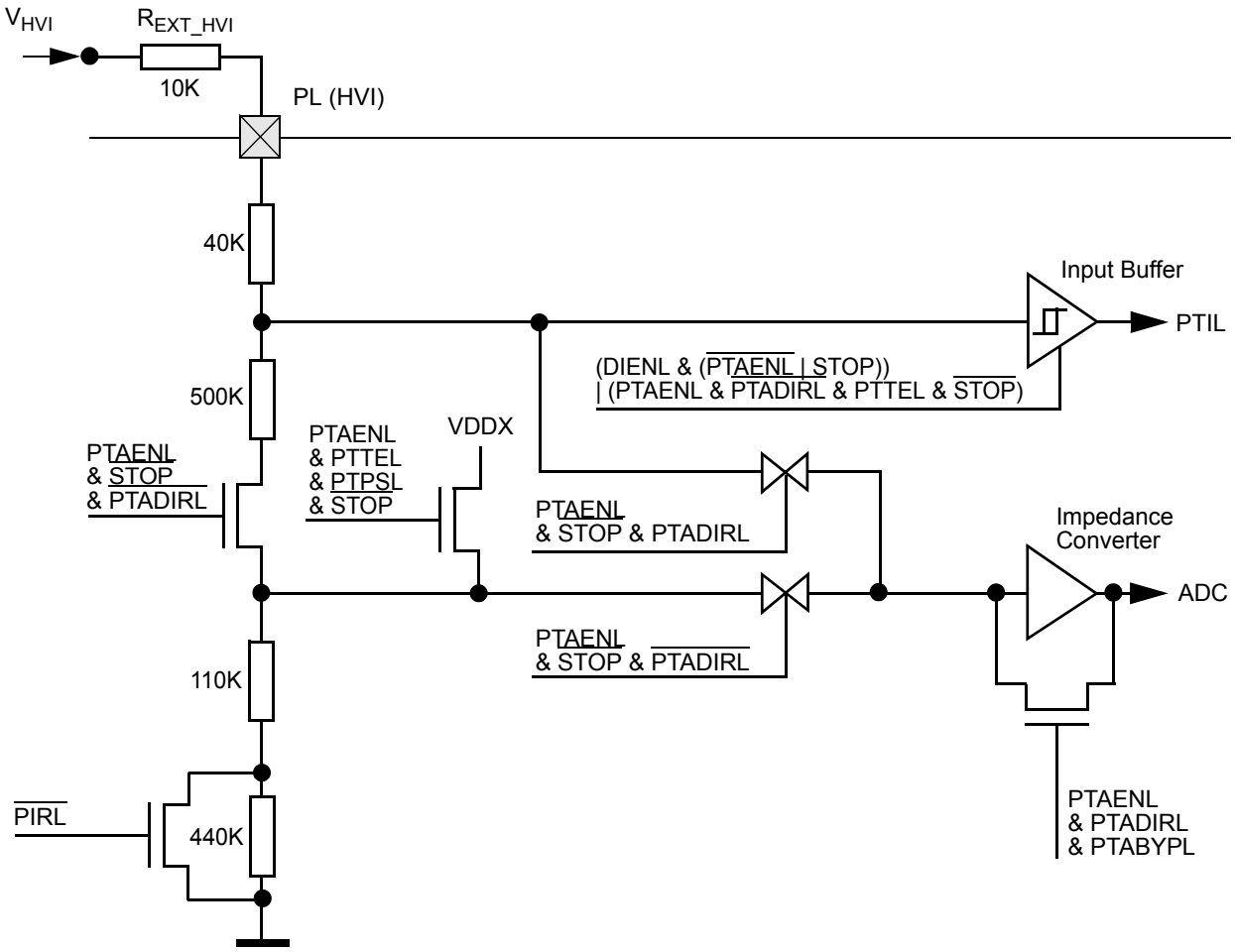


Figure 2-37. HVI Block Diagram

Voltages up to V_{HVI} can be applied to the HVI pin. Internal voltage dividers scale the input signals down to logic level. There are two modes, digital and analog, where these signals can be processed.

2.4.6.1 Digital Mode Operation

In digital mode (PTAENL=0) the input buffer is enabled if DIENL=1. The synchronized pin input state determined at threshold level V_{TH_HVI} can be read in register PTIL. Interrupt flag (PIFL) is set on input transitions if enabled (PIEL=1) and configured for the related edge polarity (PPSL). Wakeup from stop mode is supported.

2.4.6.2 Analog Mode Operation

In analog mode (PTAENL=1) the input buffer is forced off and the voltage applied to a selectable HVI pin can be measured on its related internal ADC channel(refer to device overview section for channel assignment). One of two input divider ratios ($Ratio_{H\_HVI}$, $Ratio_{L\_HVI}$) can be chosen (PIRL) on the analog

- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)
- Trace control
  - Tracing session triggered by state sequencer
  - Begin, End, and Mid alignment of tracing to trigger
- Four trace modes
  - Normal: change of flow (COF) PC information is stored (see Section 6.4.5.2.1) for change of flow definition.
  - Loop1: same as Normal but inhibits consecutive duplicate source address entries
  - Detail: address and data for all read/write access cycles are stored
  - Pure PC: All program counter addresses are stored.
- 2 Pin (data and clock) profiling interface
  - Output of code flow information

6.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

The DBG module can issue breakpoint requests to force the device to enter active BDM or an SWI ISR. The BDC BACKGROUND command is also handled by the DBG to force the device to enter active BDM. When the device enters active BDM through a BACKGROUND command with the DBG module armed, the DBG remains armed.

8.3.2.8 S12CPMU_UHV_V10_V6 Interrupt Enable Register (CPMUINT)

This register enables S12CPMU_UHV_V10_V6 interrupt requests.

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-13. S12CPMU_UHV_V10_V6 Interrupt Enable Register (CPMUINT)

Read: Anytime

Write: Anytime

Table 8-6. CPMUINT Field Descriptions

Field	Description
7 RTIE	Real Time Interrupt Enable Bit 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
4 LOCKIE	PLL Lock Interrupt Enable Bit 0 PLL LOCK interrupt requests are disabled. 1 Interrupt will be requested whenever LOCKIF is set.
1 OSCIE	Oscillator Corrupt Interrupt Enable Bit 0 Oscillator Corrupt interrupt requests are disabled. 1 Interrupt will be requested whenever OSCIF is set.

8.3.2.18 Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

The CPMUAPICTL register allows the configuration of the autonomous periodical interrupt features.

Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-24. Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

Read: Anytime

Write: Anytime

Table 8-19. CPMUAPICTL Field Descriptions

Field	Description
7 APICLK	**Autonomous Periodical Interrupt Clock Select Bit** — Selects the clock source for the API. Writable only if APIFE = 0. APICLK cannot be changed if APIFE is set by the same write operation. 0 Autonomous Clock (ACLK) used as source. 1 Bus Clock used as source.
4 APIES	**Autonomous Periodical Interrupt External Select Bit** — Selects the waveform at the external pin API_EXTCLK as shown in Figure 8-25. See device level specification for connectivity of API_EXTCLK pin. 0 If APIEA and APIFE are set, at the external pin API_EXTCLK periodic high pulses are visible at the end of every selected period with the size of half of the minimum period (APIR=0x0000 in Table 8-23). 1 If APIEA and APIFE are set, at the external pin API_EXTCLK a clock is visible with 2 times the selected API Period.
3 APIEA	**Autonomous Periodical Interrupt External Access Enable Bit** — If set, the waveform selected by bit APIES can be accessed externally. See device level specification for connectivity. 0 Waveform selected by APIES can not be accessed externally. 1 Waveform selected by APIES can be accessed externally, if APIFE is set.
2 APIFE	**Autonomous Periodical Interrupt Feature Enable Bit** — Enables the API feature and starts the API timer when set. 0 Autonomous periodical interrupt is disabled. 1 Autonomous periodical interrupt is enabled and timer starts running.
1 APIE	Autonomous Periodical Interrupt Enable Bit 0 API interrupt request is disabled. 1 API interrupt will be requested whenever APIF is set.
0 APIF	**Autonomous Periodical Interrupt Flag** — APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1.Writing a 0 has no effect. If enabled (APIE = 1), APIF causes an interrupt request. 0 API time-out has not yet occurred. 1 API time-out has occurred.

15.1.3 Block Diagram

Figure 15-1 provides an overview of the PMF module.

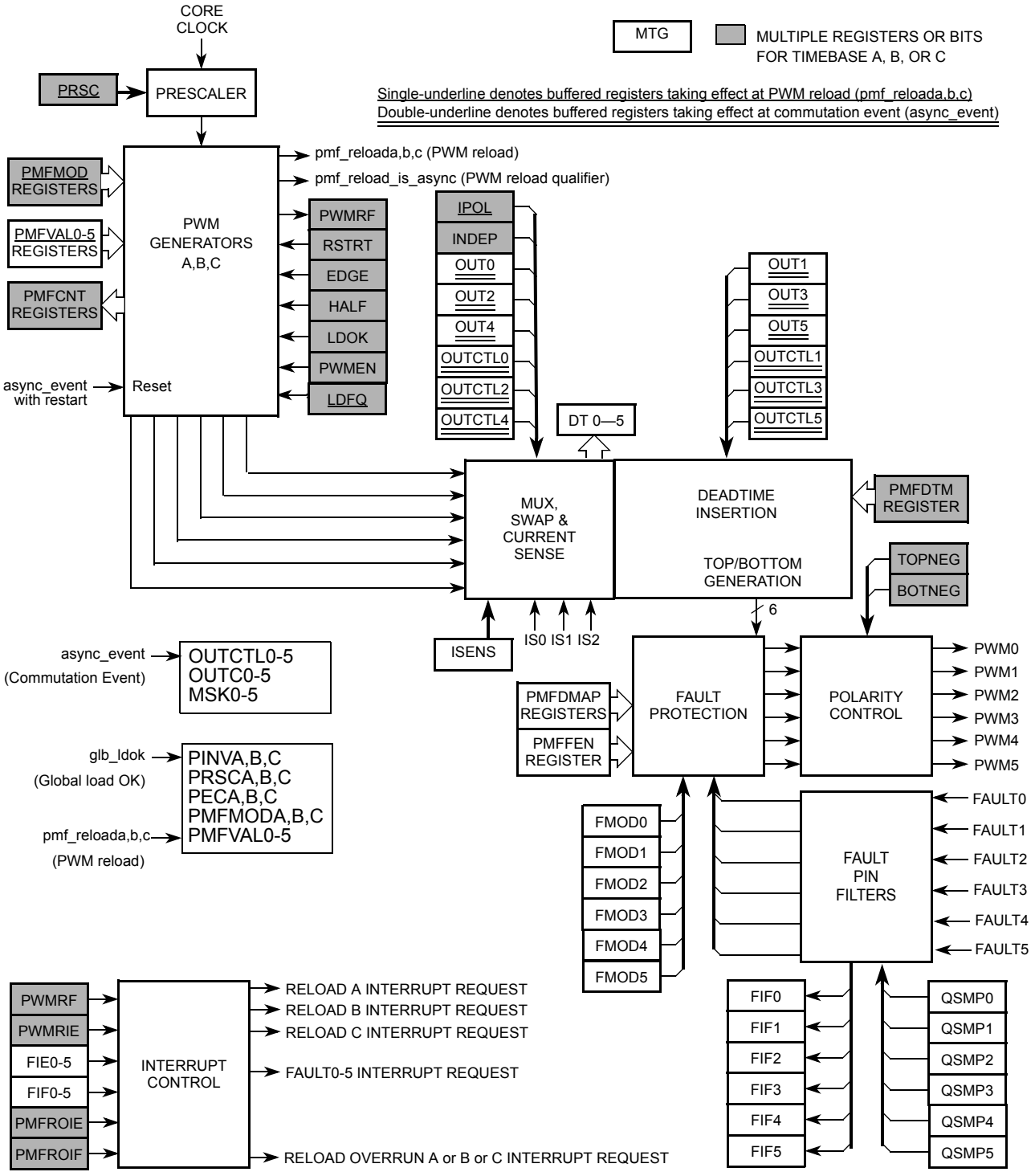


Figure 15-1. PMF Block Diagram

Table 15-31. PWM Reload Frequency B

LDFQB[3:0]	PWM Reload Frequency	LDFQ[3:0]	PWM Reload Frequency
0100	Every 5 PWM opportunities	1100	Every 13 PWM opportunities
0101	Every 6 PWM opportunities	1101	Every 14 PWM opportunities
0110	Every 7 PWM opportunities	1110	Every 15 PWM opportunities
0111	Every 8 PWM opportunities	1111	Every 16 PWM opportunities

Table 15-32. PWM Prescaler B

PRSCB[1:0]	Prescaler Value P_B	PWM Clock Frequency f_{PWM_B}
00	1	f_{core}
01	2	$f_{core}/2$
10	4	$f_{core}/4$
11	8	$f_{core}/8$

15.3.2.26 PMF Counter B Register (PMFCNTB)

Address: Module Base + 0x002A — Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFCNTB														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-31. PMF Counter B Register (PMFCNTB)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Never

This register displays the state of the 15-bit PWM B counter.

15.3.2.27 PMF Counter Modulo B Register (PMFMODB)

Address: Module Base + 0x002C — Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFMODB														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-32. PMF Counter Modulo B Register (PMFMODB)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set.Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

RXD: Receive Pin

SCI : Serial Communication Interface

TXD: Transmit Pin

16.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 16-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
  - Receive wakeup on active edge
  - Transmit collision detect supporting LIN
  - Break Detect supporting LIN
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

16.2 External Signal Description

The SCI module has a total of two external pins.

16.2.1 TXD — Transmit Pin

The TXD pin transmits SCI (standard or infrared) data. It will idle high in either mode and is high impedance anytime the transmitter is disabled.

16.2.2 RXD — Receive Pin

The RXD pin receives SCI (standard or infrared) data. An idle line is detected as a line high. This input is ignored when the receiver is disabled and should be terminated to a known voltage.

16.3 Memory Map and Register Definition

This section provides a detailed description of all the SCI registers.

16.3.1 Module Memory Map and Register Definition

The memory map for the SCI module is given below in Figure 16-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the SCI module and the address offset for each register.

Figure 16-17 shows two cases of break detect. In trace RXD_1 the break symbol starts with the start bit, while in RXD_2 the break starts in the middle of a transmission. If BRKDFE = 1, in RXD_1 case there will be no byte transferred to the receive buffer and the RDRF flag will not be modified. Also no framing error or parity error will be flagged from this transfer. In RXD_2 case, however the break signal starts later during the transmission. At the expected stop bit position the byte received so far will be transferred to the receive buffer, the receive data register full flag will be set, a framing error and if enabled and appropriate a parity error will be set. Once the break is detected the BRKDIF flag will be set.

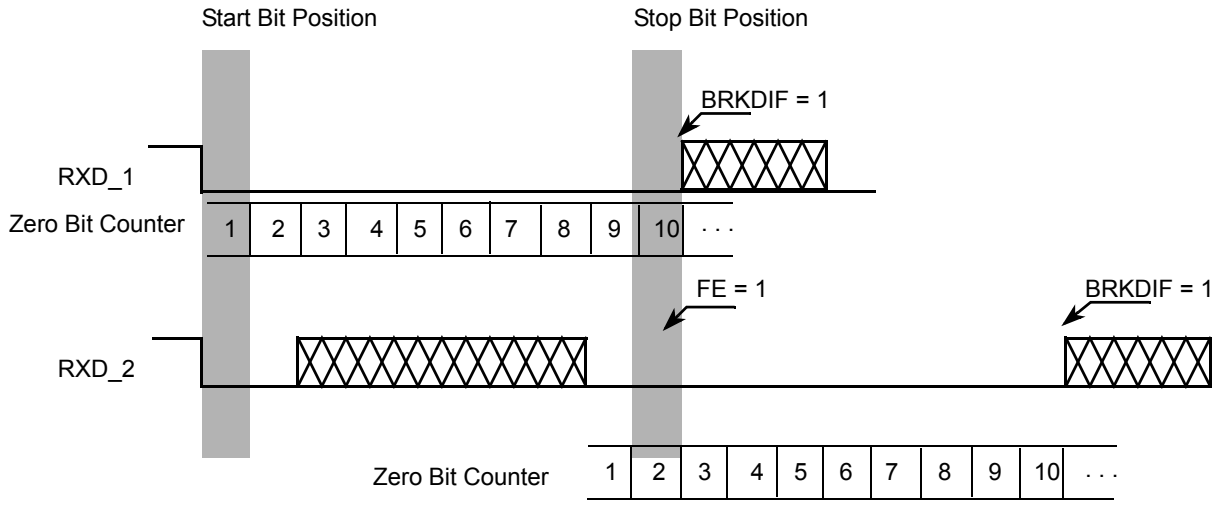


Figure 16-17. Break Detection if BRKDFE = 1 (M = 0)

16.4.5.4 Idle Characters

An idle character (or preamble) contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCICR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

16.5.3.1.6 RXEDGIF Description

The RXEDGIF interrupt is set when an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD pin is detected. Clear RXEDGIF by writing a “1” to the SCIASR1 SCI alternative status register 1.

16.5.3.1.7 BERRIF Description

The BERRIF interrupt is set when a mismatch between the transmitted and the received data in a single wire application like LIN was detected. Clear BERRIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if the bit error detect feature is disabled.

16.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

16.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

16.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

17.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

17.2.3 $\overline{SS}$ — Slave Select Pin

This pin is used to output the select signal from the SPI module to another peripheral with which a data transfer is to take place when it is configured as a master and it is used as an input to receive the slave select signal when the SPI is configured as slave.

17.2.4 SCK — Serial Clock Pin

In master mode, this is the synchronous output clock. In slave mode, this is the synchronous input clock.

17.3 Memory Map and Register Definition

This section provides a detailed description of address space and registers used by the SPI.

17.3.1 Module Memory Map

The memory map for the SPI is given in Figure 17-2. The address listed for each register is the sum of a base address and an address offset. The base address is defined at the SoC level and the address offset is defined at the module level. Reads from the reserved bits return zeros and writes to the reserved bits have no effect.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
	W								
0x0001 SPICR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
	W								
0x0002 SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
	W								
0x0003 SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
	W								
0x0004 SPIDRH	R	R15	R14	R13	R12	R11	R10	R9	R8
	W	T15	T14	T13	T12	T11	T10	T9	T8
0x0005 SPIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0
0x0006 Reserved	R								
	W								

= Unimplemented or Reserved

Figure 17-2. SPI Register Summary

17.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 17-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 17-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 17-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 17-10).

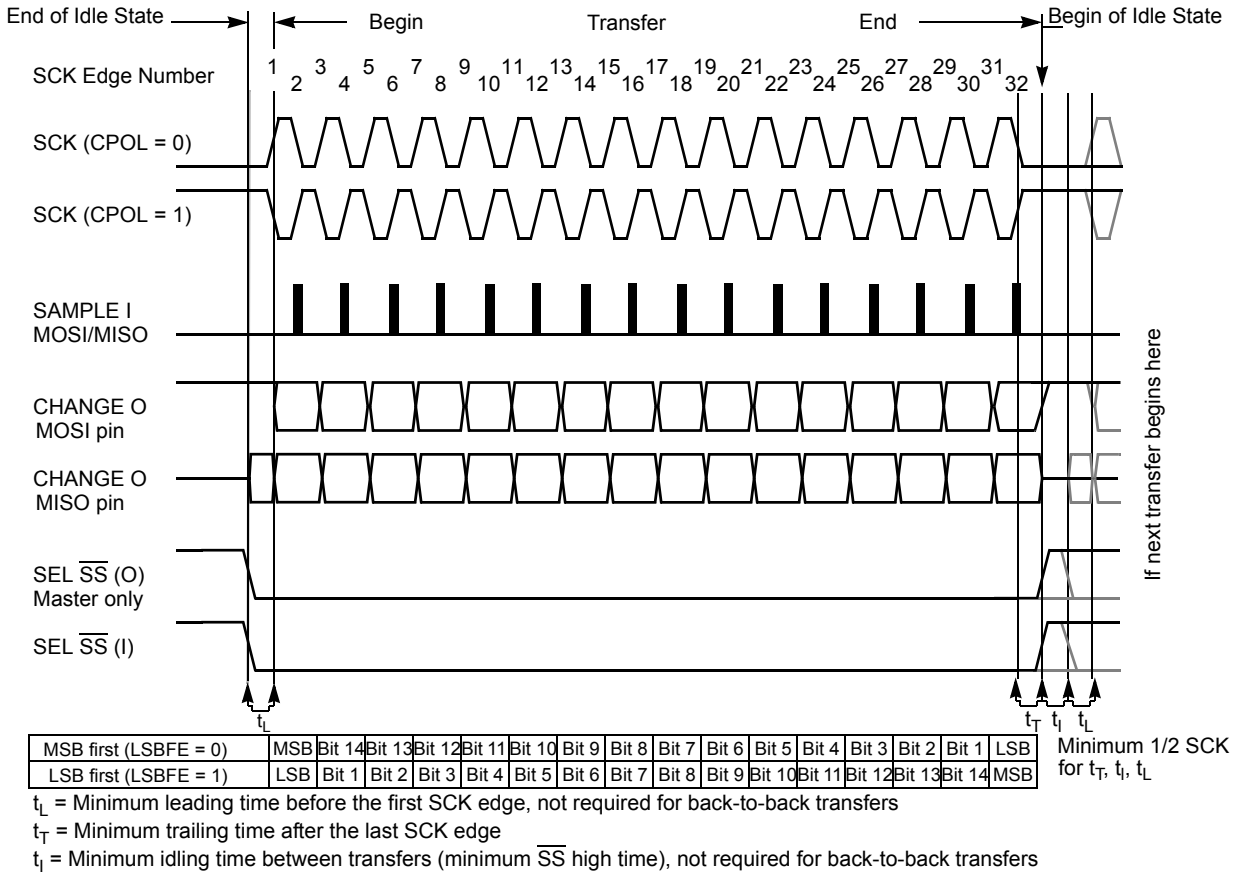


Figure 17-15. SPI Clock Format 1 (CPHA = 1), with 16-Bit Transfer Width selected (XFRW = 1)

The $\overline{SS}$ line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

- Back-to-back transfers in master mode

  In master mode, if a transmission has completed and new data is available in the SPI data register, this data is sent out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.

17.4.4 SPI Baud Rate Generation

Baud rate generation consists of a series of divider stages. Six bits in the SPI baud rate register (SPPR2, SPPR1, SPPR0, SPR2, SPR1, and SPR0) determine the divisor to the SPI module clock which results in the SPI baud rate.

The SPI clock rate is determined by the product of the value in the baud rate preselection bits (SPPR2–SPPR0) and the value in the baud rate selection bits (SPR2–SPR0). The module clock divisor equation is shown in Equation 17-3.

18.3.2.2 GDU Control Register (GDUCTR)

Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	GHHDLVL	GVLSLVL	GBKTIM2[3:0]				GBKTIM1[1:0]	
Reset	0	1	0	1	0	0	0	0

= Unimplemented

Figure 18-4. GDU Control Register (GDUCTR)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-4. GDUCTR Register Field Descriptions

Field	Description
7 GHHDLVL	GDU High HD Level Select — Selects the voltage threshold of the overvoltage detection on HD pin. This bit cannot be modified after GWP bit is set. 0 Voltage thresholds of the overvoltage detection on HD pin configured for V_{HVHDLA} and V_{HVHDLD} 1 Voltage thresholds of the overvoltage detection on HD pin configured for V_{HVHDHA} and V_{HVHDHD}
6 GVLSLVL (Not featured on GDUV4)	GDU VLS Level Select — Selects the voltage threshold of the undervoltage detection on VLS pin. This bit cannot be modified after GWP bit is set. 0 Voltage thresholds of the undervoltage detection on VLS pin configured for V_{LVLSLA} and V_{LVLSLD} 1 Voltage thresholds of the undervoltage detection on VLS pin configured for V_{LVLSHA} and V_{LVLSHD}
5-2 GBKTIM2[3:0]	GDU Blanking Time — These bits adjust the blanking time t_{BLANK} of the desaturation error comparators. The resulting blanking time t_{BLANK} can be calculated from the equation below. For GBKTIM2[3:0]=$F no desaturation errors are captured and the drivers are unprotected and the charge pump will not connect to the high-side drivers. These bits cannot be modified after GWP bit is set. $t_{BLANK} = [((GBKTIM2 + 1) \cdot 2^{GBKTIM1 + 1}) + 2] \cdot T_{BUS}$
1-0 GBKTIM1[1:0]	GDU Blanking Time — These bits adjust the blanking time t_{BLANK} of the desaturation error comparators. The resulting blanking time t_{BLANK} can be calculated from the equation in the field description above.These bits cannot be modified after GWP bit is set.

NOTE

The register bits GBKTIM1 and GBKTIM2 must be set to the required values before the PWM channel is activated. Once the PWM channel is activated, the value of GBKTIM1 & GBKTIM2 must not change. If a different blanking time is required, the PWM channel has to be turned off before new values to GBKTIM1 & GBKTIM2 are written.

18.3.2.17 GDU Control Register 1 (GDUCTR1)

Module Base + 0x0010 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GSRMOD1	GSRMOD0	0	0	0	0	0	TDEL
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-19. GDU Control Register 1 (GDUCTR1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-21. GDUCTR1 Register Field Descriptions

Field	Description
7 GSRMOD1	GDU Switched Reluctance Motor Mode 1 — This bit cannot be modified after GWP bit is set. This bit controls the routing of the LDx pins to the low-side desaturation comparators for switched reluctance motor. See Figure 18-23 0 HSx routed to low-side desaturation comparator 1 LDx routed to low-side desaturation comparator
6 GSRMOD0	GDU Switched Reluctance Motor Mode 0 — This bit cannot be modified after GWP bit is set. 0 BLDC mode. Don't allow HGx and LGx high at the same time. 1 SR mode. Allow HGx and LGx high at the same time.
0 TDEL	**t_{delon} / t_{deloff} Control** — This bit controls the parameters t_{delon} and t_{deloff}. It cannot be modified after GWP bit is set. This bit must be set to meet the min and max values for t_{delon} and t_{deloff} specified in the electrical specification. If this bit is cleared the values for t_{delon} and t_{deloff} are out of spec.

NOTE

GDU Control Register 1 GDUCTR1 availability is defined at device level.

18.5 Application Information

18.5.1 FET Pre-Driver Details

The basic concept of the high-side driver is shown in Figure 18-29. If the FET pre-driver is switched on the transistor T2 is driving the output HG. For on resistance R_{gduon} of transistor T2 refer to GDU electricals. The output current is limited to I_{OUT} which is derived from the reference current I_{REF}. The current source is controlled by the slew rate control bits GSRCHS[2:0]. If the FET pre-driver is switched off transistors T3 and T4 are switched on. For on resistance $R_{gduoffn}$ and $R_{gduoffp}$ of transistors T3 and T4 refer to GDU electricals.

The reference current I_{REF} is controlled by the slew rate control bits GSRCHS[2:0] :

- I_{REF} = 10uA + GSRCHS 10uA, [10uA, 20uA . . . 80uA]

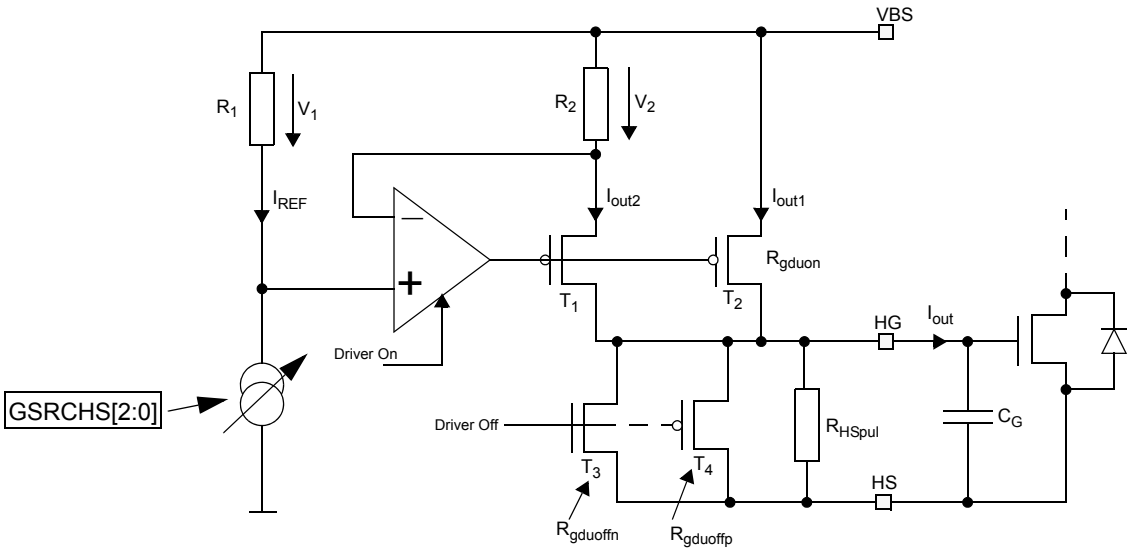
Assuming an ideal op-amp the voltage across R_1 is equal voltage across R_2 and I_{OUT2} is given by:

- $V_1 = V_2 = I_{REF} R_1 = I_{OUT2} R_2$
- $I_{OUT2} = I_{REF} (R_1/R_2)$

With the ratio of the transistor sizes of T_1 and T_2 k=450, and the ratio of the resistors R_1/R_2=36, and neglect the current through R_{HSpul} the output current I_{OUT} is:

- $I_{OUT1} = k\ I_{OUT2}$
- $I_{OUT} = I_{OUT1} + I_{OUT2} = I_{REF} (R_1/R_2) (1+k)$
- $I_{OUT} \sim I_{REF} (R_1/R_2)\ k$

Figure 18-29. FET Pre-Driver Concept for High-Side Driver



NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 LPDR	R	0	0	0	0	0	0	LPDR1	LPDR0
	W								
0x0001 LPCR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
	W								
0x0002 Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0003 LPSLRM	R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
	W								
0x0004 Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0005 LPSR	R	LPDT	0	0	0	0	0	0	0
	W								
0x0006 LPIE	R	LPDTIE	LPOCIE	0	0	0	0	0	0
	W								
0x0007 LPIF	R	LPDTIF	LPOCIF	0	0	0	0	0	0
	W								

Figure 19-2. Register Summary

Table 20-32. Allowed P-Flash and EEPROM Simultaneous Operations on a single hardblock

	EEPROM				
Program Flash	**Read**	**Margin Read[2]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read	OK[(1)]	OK	OK	OK	
Margin Read[(2)]					
Program					
Sector Erase					
Mass Erase[(3)]					OK

1. Strictly speaking, only one read of either the P-Flash or EEPROM can occur at any given instant, but the memory controller will transparently arbitrate P-Flash and EEPROM accesses giving uninterrupted read access whenever possible.

2. A 'Margin Read' is any read after executing the margin setting commands 'Set User Margin Level' or 'Set Field Margin Level' with anything but the 'normal' level specified. See the Note on margin settings in Section 20.4.7.12 and Section 20.4.7.13.

3. The 'Mass Erase' operations are commands 'Erase All Blocks' and 'Erase Flash Block'

20.4.7 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation may return invalid data resulting in an illegal access (as described on Section 20.4.6).

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 20.3.2.7).

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

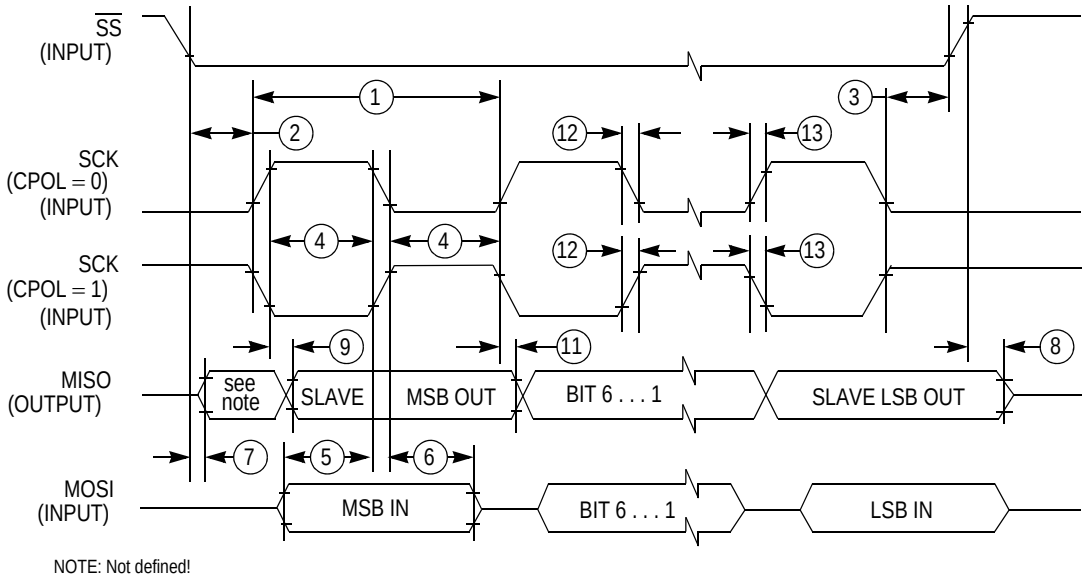


Figure I-6. SPI Slave Timing (CPHA=1)

Table I-2. SPI Slave Mode Timing Characteristics -40°C to 175°C

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1		SCK Frequency	f_{sck}	DC	—	1/4[1]	f_{bus}
1		SCK Period	t_{sck}	4	—	∞	t_{bus}
2		Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3		Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4		Clock (SCK) High or Low Time	t_{wsck}	$2t_{bus}$ - (t_{rfi} + t_{rfo})	—	—	ns
5		Data Setup Time (Inputs)	t_{su}	3	—	—	ns
6		Data Hold Time (Inputs)	t_{hi}	2	—	—	ns
7		Slave Access Time (time to data active)	t_a	—	—	28	ns
8		Slave MISO Disable Time	t_{dis}	—	—	26	ns
9a		Data Valid after SCK Edge (-40°C < T_j < 150°C)	t_{vsck}	—	—	$23 + 0.5 \cdot t_{bus}$ [2]	ns
9b		Data Valid after SCK Edge (150°C <T_j < 175°C)[1]	t_{vsck}	—	—	$25 + 0.5 \cdot t_{bus}$ [2]	ns
10a		Data Valid after $\overline{SS}$ fall (-40°C < T_j < 150°C)	t_{vss}	—	—	$23 + 0.5 \cdot t_{bus}$ [2]	ns
10b		Data Valid after $\overline{SS}$ fall (150°C < T_j < 175°C)[1]	t_{vss}	—	—	$25 + 0.5 \cdot t_{bus}$ [2]	ns
11		Data Hold Time (Outputs)	t_{ho}	22	—	—	ns
12		Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13		Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

1. f_{bus} max is 40MHz at temperatures above 150°C

2. $0.5t_{bus}$ added due to internal synchronization delay