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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-LQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml31f1mkfr

1.8.3 Device Level PMF Connectivity

Table 1-12. Mapping of PMF signals

PMF Connection	Usage
Channel0	High-Side Gate and Source Pins HG[0], HS[0]
Channel1	Low-Side Gate and Source Pins LG[0], LS[0]
Channel2	High-Side Gate and Source Pins HG[1], HS[1]
Channel3	Low-Side Gate and Source Pins LG[1], LS[1]
Channel4	High-Side Gate and Source Pins HG[2], HS[2]
Channel5	Low-Side Gate and Source Pins LG[2], LS[2]
FAULT5	External FAULT5 pin
FAULT4	HD Over voltage or GDU over current
FAULT3	VLS under voltage
FAULT2	GDU Desaturation[2] or GDU over current
FAULT1	GDU Desaturation[1] or GDU over current
FAULT0	GDU Desaturation[0] or GDU over current
IS2	GDU Phase Status[2]
IS1	GDU Phase Status[1]
IS0	GDU Phase Status[0]
async_event_edge_sel[1:0]	Tied to b11 (both edges active)

1.8.4 BDC Clock Source Connectivity

The BDC clock, BDCCLK, is mapped to the IRCCLK generated in the CPMU module.

The BDC clock, BDCFCLK is mapped to the device bus clock, generated in the CPMU module.

1.8.5 LINPHY Connectivity

The VLINSUP supply is device dependent.

On ZVML128, ZVMC128, ZVML64, ZVMC64 and ZVML32 devices with the maskset number 2N95G it is connected to VSUP

On all other devices it is connected to the device HD pin.

The LINPHY0 signals are mapped internally to SCI0. The receiver can be routed to TIM0 input capture channel3. These routing options are described in detail in the PIM section.

1.8.6 HVPHY Connectivity

The HVPHY signals (S12ZVM32 and S12ZVM16 derivatives only) are mapped internally to SCI0. The receiver can be routed to TIM0 input capture channel3.

2.3.3.6 Port Interrupt Enable Register

Address 0x028C PIEADH
0x028D PIEADL
0x02D6 PIES
0x0336 PIEL

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIEx7	PIEx6	PIEx5	PIEx4	PIEx3	PIEx2	PIEx1	PIEx0
Reset	0	0	0	0	0	0	0	0

Figure 2-17. Port Interrupt Enable Register

1. Read: Anytime
   Write: Anytime

This is a generic description of the standard port interrupt enable registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-22. Port Interrupt Enable Register Field Descriptions

Field	Description
7-0 PIEx7-0	**Port Interrupt Enable** — Activate pin interrupt (KWU) This bit enables or disables the edge sensitive pin interrupt on the associated pin. An interrupt can be generated if the pin is operating in input or output mode when in use with the general-purpose or related peripheral function. 1 Interrupt is enabled 0 Interrupt is disabled (interrupt flag masked)

2.3.3.7 Port Interrupt Flag Register

Address 0x028E PIFADH
0x028F PIFADL
0x02D7 PIFS
0x0337 PIFL

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIFx7	PIFx6	PIFx5	PIFx4	PIFx3	PIFx2	PIFx1	PIFx0
Reset	0	0	0	0	0	0	0	0

Figure 2-18. Port Interrupt Flag Register

1. Read: Anytime
   Write: Anytime, write 1 to clear

This is a generic description of the standard port interrupt flag registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

3.4.2 Illegal Accesses

The S12ZMMC module monitors all memory traffic for illegal accesses. See Table 3-9 for a complete list of all illegal accesses.

Table 3-9. Illegal memory accesses

		S12ZCPU	S12ZBDC	ADCs and PTU
Register space	Read access	ok	ok	illegal access
	Write access	ok	ok	illegal access
	Code execution	illegal access		
RAM	Read access	ok	ok	ok
	Write access	ok	ok	ok
	Code execution	ok		
EEPROM	Read access	ok(1)	ok[1]	ok[1]
	Write access	illegal access	illegal access	illegal access
	Code execution	ok[1]		
Reserved Space	Read access	ok	ok	illegal access
	Write access	only permitted in SS mode	ok	illegal access
	Code execution	illegal access		
Reserved Read-only Space	Read access	ok	ok	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		
NVM IFR	Read access	ok[1]	ok[1]	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		
Program NVM	Read access	ok[1]	ok[1]	ok[1]
	Write access	illegal access	illegal access	illegal access
	Code execution	ok[1]		
Unmapped Space	Read access	illegal access	illegal access	illegal access
	Write access	illegal access	illegal access	illegal access
	Code execution	illegal access		

1. Unsupported NVM accesses during NVM command execution (“collisions”), are treated as illegal accesses.

Illegal accesses are reported in several ways:

- All illegal accesses performed by the S12ZCPU trigger machine exceptions.
- All illegal accesses performed through the S12ZBDC interface, are captured in the ILLACC bit of the BDCCSRL register.

			Memory Address[2:0]						
Case	Access Address	Access Size	000	001	010	011	100	101	110
8	11	16-bit				DBGxD3	DBGxD0		
9	00	8-bit	DBGxD0						
10	01	8-bit		DBGxD1					
11	10	8-bit			DBGxD2				
12	11	8-bit				DBGxD3			
13	00	8-bit					DBGxD0		
				Denotes byte that is not accessed.					

For a match of a 32-bit access with data compare, the address comparator must be loaded with the address of the lowest accessed byte. For Case1 Table 6-44 this corresponds to 000, for Case2 it corresponds to 001. To compare all 32-bits, it is required that no bits are masked.

6.4.2.3 Data Bus Comparison NDB Dependency

The NDB control bit allows data bus comparators to be configured to either match on equivalence or on difference. This allows monitoring of a difference in the contents of an address location from an expected value.

When matching on an equivalence (NDB=0), each individual data bus bit position can be masked out by clearing the corresponding mask bit, so that it is ignored in the comparison. A match occurs when all data bus bits with corresponding mask bits set are equivalent. If all mask register bits are clear, then a match is based on the address bus only, the data bus is ignored.

When matching on a difference, mask bits can be cleared to ignore bit positions. A match occurs when any data bus bit with corresponding mask bit set is different. Clearing all mask bits, causes all bits to be ignored and prevents a match because no difference can be detected. In this case address bus equivalence does not cause a match. Bytes that are not accessed are ignored. Thus when monitoring a multi byte field for a difference, partial accesses of the field only return a match if a difference is detected in the accessed bytes.

Table 6-45. NDB and MASK bit dependency

NDB	DBGADM	Comment
0	0	Do not compare data bus bit.
0	1	Compare data bus bit. Match on equivalence.
1	0	Do not compare data bus bit.
1	1	Compare data bus bit. Match on difference.

6.4.2.4 Range Comparisons

Range comparisons are accurate to byte boundaries. Thus for data access comparisons a match occurs if at least one byte of the access is in the range (inside range) or outside the range (outside range). For opcode comparisons only the address of the first opcode byte is compared with the range.

TSINF provides information about a timestamp. Bit1 indicates if the byte is a TSINF byte.

Table 6-55. CINF Field Descriptions

Field	Description
7–6 CSZ	**Access Type Indicator** — This field indicates the CPU access size. 00 8-bit Access 01 16-bit Access 10 24-bit Access 11 32-bit Access
5 CRW	**Read/Write Indicator** — Indicates if the corresponding stored address corresponds to a read or write access. 0 Write Access 1 Read Access

Table 6-56. TSINF Field Descriptions

Field	Description
3 CTI	**Comparator Timestamp Indicator** — This bit indicates if the trace buffer entry corresponds to a comparator timestamp. 0 Trace buffer entry initiated by trace mode specification conditions or timestamp counter overflow 1 Trace buffer entry initiated by comparator D match
2 PC	**Program Counter Valid Indicator** — Indicates if the PC entry is valid on the timestamp line. 0 Trace buffer entry does not include PC value 1 Trace buffer entry includes PC value
0 TOVF	**Timestamp Overflow Indicator** — Indicates if the trace buffer entry corresponds to a timestamp overflow 0 Trace buffer entry not initiated by a timestamp overflow 1 Trace buffer entry initiated by a timestamp overflow

6.4.5.2.4 Pure PC Mode

In Pure PC Mode, the PC addresses of all opcodes loaded into the execution stage, including illegal opcodes, are stored.

Tracing from a single source, compression is implemented to increase the effective trace depth. A compressed entry consists of the lowest PC byte only. A full entry consists of all PC bytes. If the PC remains in the same 256 byte range, then a compressed entry is made, otherwise a full entry is made. The full entry is always the last entry of a record.

Each trace buffer line consists of 7 payload bytes, PLB0-6, containing full or compressed CPU PC addresses and 1 information byte to indicate the type of entry (compressed or base address) for each payload byte.

Each trace buffer line is filled from right to left. The final entry on each line is always a base address, used as a reference for the previous entries on the same line. Whilst tracing, a base address is typically stored

Table 8-12. RTI Frequency Divide Rates for RTDEC = 0

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF(1)	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷13)	OFF	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$
1110 (÷15)	OFF	$15x2^{10}$	$15x2^{11}$	$15x2^{12}$	$15x2^{13}$	$15x2^{14}$	$15x2^{15}$	$15x2^{16}$
1111 (÷16)	OFF	$16x2^{10}$	$16x2^{11}$	$16x2^{12}$	$16x2^{13}$	$16x2^{14}$	$16x2^{15}$	$16x2^{16}$

1. Denotes the default value out of reset.This value should be used to disable the RTI to ensure future backwards compatibility.

Table 8-28. TC trimming of the frequency of the IRC1M at ambient temperature

TCTRIM[4:0]	IRC1M Indicative relative TC variation	IRC1M indicative frequency drift for relative TC variation
00000	0 (nominal TC of the IRC)	0%
00001	-0.27%	-0.5%
00010	-0.54%	-0.9%
00011	-0.81%	-1.3%
00100	-1.08%	-1.7%
00101	-1.35%	-2.0%
00110	-1.63%	-2.2%
00111	-1.9%	-2.5%
01000	-2.20%	-3.0%
01001	-2.47%	-3.4%
01010	-2.77%	-3.9%
01011	-3.04	-4.3%
01100	-3.33%	-4.7%
01101	-3.6%	-5.1%
01110	-3.91%	-5.6%
01111	-4.18%	-5.9%
10000	0 (nominal TC of the IRC)	0%
10001	+0.27%	+0.5%
10010	+0.54%	+0.9%
10011	+0.81%	+1.3%
10100	+1.07%	+1.7%
10101	+1.34%	+2.0%
10110	+1.59%	+2.2%
10111	+1.86%	+2.5%
11000	+2.11%	+3.0%
11001	+2.38%	+3.4%
11010	+2.62%	+3.9%
11011	+2.89%	+4.3%
11100	+3.12%	+4.7%
11101	+3.39%	+5.1%
11110	+3.62%	+5.6%
11111	+3.89%	+5.9%

NOTE

Since the IRC1M frequency is not a linear function of the temperature, but more like a parabola, the above relative variation is only an indication and should be considered with care.

Table 9-3. ADCCTL_0 Field Descriptions (continued)

Field	Description
11-10 ACC_CFG[1:0]	ADCFLWCTL Register Access Configuration — These bits define if the register ADCFLWCTL is controlled via internal interface only or data bus only or both. See Table 9-4. for more details.
9 STR_SEQA	Control Of Conversion Result Storage and RSTAR_EIF flag setting at Sequence Abort or Restart Event — This bit controls conversion result storage and RSTAR_EIF flag setting when a Sequence Abort Event or Restart Event occurs as follows: If STR_SEQA = 1'b0 and if a: • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is not stored and the respective conversion complete flag is not set • Restart Event only is issued before the last conversion of a CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware If STR_SEQA = 1'b1 and if a: • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is stored and the respective conversion complete flag is set and Intermediate Result Information Register is updated. • Restart Event only occurs during the last conversion of a CSL and no Sequence Abort Event is in process (SEQA clear) does not set the RSTA_EIF error flag • Restart Event only is issued before the CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware
8 MOD_CFG	(Conversion Flow Control) Mode Configuration — This bit defines the conversion flow control after a Restart Event and after execution of the "End Of List" command type: - Restart Mode - Trigger Mode (For more details please see also section Section 9.6.3.2, "Introduction of the Programmer's Model and following.) 0 "Restart Mode" selected. 1 "Trigger Mode" selected.

Table 9-4. ADCFLWCTL Register Access Configurations

ACC_CFG[1]	ACC_CFG[0]	ADCFLWCTL Access Mode
0	0	None of the access paths is enabled (default / reset configuration)
0	1	Single Access Mode - Internal Interface (ADCFLWCTL access via internal interface only)
1	0	Single Access Mode - Data Bus (ADCFLWCTL access via data bus only)
1	1	Dual Access Mode (ADCFLWCTL register access via internal interface and data bus)

NOTE

Each conversion flow control bit (SEQA, RSTA, TRIG, LDOK) must be controlled by software or internal interface according to the requirements described in Section 9.6.3.2.4, "The two conversion flow control Mode Configurations and overview summary in Table 9-11.

Table 9-10. ADCFLWCTL Field Descriptions

Field	Description
7 SEQA	**Conversion Sequence Abort Event** — This bit indicates that a conversion sequence abort event is in progress. When this bit is set the ongoing conversion sequence and current CSL will be aborted at the next conversion boundary. This bit gets cleared when the ongoing conversion sequence is aborted and ADC is idle. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. Data Bus Control: This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. Writing a one to this bit does not clear it but causes an overrun if the bit has already been set. See Section 9.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. Internal Interface Control: This bit can be controlled via the internal interface Signal "Seq_Abort" if access control is configured accordingly via ACC_CFG[1:0]. After being set an additional request via the internal interface Signal "Seq_Abort" causes an overrun. See also conversion flow control in case of overrun situations. General: In both conversion flow control modes (Restart Mode and Trigger Mode) when bit RSTA gets set automatically bit SEQA gets set when the ADC has not reached one of the following scenarios: - A Sequence Abort request is about to be executed or has been executed. - "End Of List" command type has been executed or is about to be executed In case bit SEQA is set automatically the Restart error flag RSTA_EIF is set to indicate an unexpected Restart Request. 0 No conversion sequence abort request. 1 Conversion sequence abort request.
6 TRIG	**Conversion Sequence Trigger Bit** — This bit starts a conversion sequence if set and no conversion or conversion sequence is ongoing. This bit is cleared when the first conversion of a sequence starts to sample. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. Data Bus Control: This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. After being set this bit can not be cleared by writing a value of 1'b1 instead the error flag TRIG_EIF is set. See also Section 9.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. Internal Interface Control: This bit can be controlled via the internal interface Signal "Trigger" if access control is configured accordingly via ACC_CFG[1:0]. After being set an additional request via internal interface Signal "Trigger" causes the flag TRIG_EIF to be set. 0 No conversion sequence trigger. 1 Trigger to start conversion sequence.

9.5.2.15 ADC Command Register 0 (ADCCMD_0)

Module Base + 0x0014

	31	30	29	28	27	26	25	24
R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
W								
R	CMD_SEL		OPT[1:0](1)		INTFLG_SEL[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-18. ADC Command Register 0 (ADCCMD_0)

1. Only available on ADC12B_LBA V2 and V3 (see Table 9-2 for details)

Read: Anytime

Write: Only writable if bit SMOD_ACC is set
(see also Section 9.5.2.2, “ADC Control Register 1 (ADCCTL_1) bit SMOD_ACC description for more details)

Table 9-20. ADCCMD_0 Field Descriptions

Field	Description
31-30 CMD_SEL[1:0]	**Conversion Command Select Bits** — These bits define the type of current conversion described in Table 9-21.
	ADC12B_LBA V2 and V3 (includes OPT[1:0])
29-28 OPT[1:0]	**Option Bits** — These two option bits can be used to control a SoC level feature/function. These bits are used together with Option bits OPT[2:3]. Please refer to the device reference manual for details of the feature/functionality controlled by these bits
27-24 INTFLG_SEL[3:0]	**Conversion Interrupt Flag Select Bits** — These bits define which interrupt flag is set in the ADCIFH/L register at the end of current conversion.The interrupt flags ADCIF[15:1] are selected via binary coded bits INTFLG_SEL[3:0]. See also Table 9-22

NOTE

If bit SMOD_ACC is set modifying this register must be done carefully - only when no conversion and conversion sequence is ongoing.

Table 9-21. Conversion Command Type Select

CMD_SEL[1]	CMD_SEL[0]	Conversion Command Type Description
0	0	Normal Conversion
0	1	End Of Sequence (Wait for Trigger to execute next sequence or for a Restart)

9.5.2.24 ADC Command and Result Offset Register 1 (ADCCROFF1)

It is important to note that these bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).

Module Base + 0x0025

	7	6	5	4	3	2	1	0
R	0	CMDRES_OFF1[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-27. ADC Command and Result Offset Register 1 (ADCCROFF1)

Read: Anytime

Write: These bits are writable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-32. ADCCROFF1 Field Descriptions

Field	Description
6-0 CMDRES_OFF1[6:0]	**ADC Result Address Offset Value** — These bits represent the conversion command and result offset value relative to the conversion command base pointer address and result base pointer address in the memory map to refer to CSL_1 and RVL_1. It is used to calculate the address inside the system RAM to which the result at the end of the current conversion is stored to and the area (RAM or NVM) from which the conversion commands are loaded from. These bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).,These bits can only be modified if bit ADC_EN is clear. See also Section 9.6.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) and Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs) for more details.

11.3.2.13 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 11-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 11-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	Output Compare Pin Disconnect Bits 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

11.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 11-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 13-5. Synchronization Jump Width

SJW1	SJW0	Synchronization Jump Width
0	0	1 Tq clock cycle
0	1	2 Tq clock cycles
1	0	3 Tq clock cycles
1	1	4 Tq clock cycles

Table 13-6. Baud Rate Prescaler

BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	Prescaler value (P)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

13.3.2.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
Reset:	0	0	0	0	0	0	0	0

Figure 13-7. MSCAN Bus Timing Register 1 (CANBTR1)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-7. CANBTR1 Register Field Descriptions

Field	Description
7 SAMP	**Sampling** — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit(1). If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0).

Table 15-23. PMFROIE Descriptions

Field	Description
2 PMFROIEC	Reload Overrun Interrupt Enable C — 0 Reload Overrun Interrupt C disabled 1 Reload Overrun Interrupt C enabled
1 PMFROIEB	Reload Overrun Interrupt Enable B — 0 Reload Overrun Interrupt B disabled 1 Reload Overrun Interrupt B enabled
0 PMFROIEA	Reload Overrun Interrupt Enable A — 0 Reload Overrun Interrupt A disabled 1 Reload Overrun Interrupt A enabled

15.3.2.16 PMF Interrupt Flag Register (PMFROIF)

Address: Module Base + 0x001D

Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PMFROIFC	PMFROIFB	PMFROIFA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-19. PMF Interrupt Flag Register (PMFROIF)

1. Read: Anytime
   Write: Anytime. Write 1 to clear.

Table 15-24. PMFROIF Field Descriptions

Field	Description
2 PMFROIFC	Reload Overrun Interrupt Flag C — If a reload event occurs when the LDOKC or global load OK bit is not set then this flag will be set. 0 No Reload Overrun C occurred 1 Reload Overrun C occurred
1 PMFROIFB	Reload Overrun Interrupt Flag B — If a reload event occurs when the LDOKB or global load OK bit is not set then this flag will be set. 0 No Reload Overrun B occurred 1 Reload Overrun B occurred
0 PMFROIFA	Reload Overrun Interrupt Flag A — If PMFCFG2[REV1:REV0]=01 and a reload event occurs when the LDOKA or global load OK bit is not set then this flag will be set. If PMFCFG2[REV1:REV0]=10 and a reload event occurs when the LDOKB or global load OK bit is not set then this flag will be set. If PMFCFG2[REV1:REV0]=11 and a reload event occurs when the LDOKC or global load OK bit is not set then this flag will be set. If PMFCFG2[REV1:REV0]=00 no flag will be generated. 0 No Reload Overrun A occurred 1 Reload Overrun A occurred

Table 15-26. PMFFQCA Field Descriptions (continued)

Field	Description
0 PWMRFA	**PWM Reload Flag A** — This flag is set at the beginning of every reload cycle regardless of the state of the LDOKA bit or global load OK. Clear PWMRFA by reading PMFFQCA with PWMRFA set and then writing a logic one to the PWMRFA bit. If another reload occurs before the clearing sequence is complete, writing logic one to PWMRFA has no effect. 0 No new reload cycle since last PWMRFA clearing 1 New reload cycle since last PWMRFA clearing **Note:** Clearing PWMRFA satisfies pending PWMRFA CPU interrupt requests.

Table 15-27. PWM Reload Frequency A

LDFQA[3:0]	PWM Reload Frequency	LDFQ[3:0]	PWM Reload Frequency
0000	Every PWM opportunity	1000	Every 9 PWM opportunities
0001	Every 2 PWM opportunities	1001	Every 10 PWM opportunities
0010	Every 3 PWM opportunities	1010	Every 11 PWM opportunities
0011	Every 4 PWM opportunities	1011	Every 12 PWM opportunities
0100	Every 5 PWM opportunities	1100	Every 13 PWM opportunities
0101	Every 6 PWM opportunities	1101	Every 14 PWM opportunities
0110	Every 7 PWM opportunities	1110	Every 15 PWM opportunities
0111	Every 8 PWM opportunities	1111	Every 16 PWM opportunities

Table 15-28. PWM Prescaler A

PRSCA[1:0]	Prescaler Value P_A	PWM Clock Frequency f_{PWM_A}
00	1	f_{core}
01	2	$f_{core}/2$
10	4	$f_{core}/4$
11	8	$f_{core}/8$

15.3.2.21 PMF Counter A Register (PMFCNTA)

Address: Module Base + 0x0022 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFCNTA														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-26. PMF Counter A Register (PMFCNTA)

1. Read: Anytime
   Write: Never

This register displays the state of the 15-bit PWM A counter.

```
PMFCFG2[MSK5:MSK0]             = 0x0c; // Branch C<->A, mask B // 120°
PMFCFG3[PINVC,PINVB,PINVA]     = 0x1;  // Invert A

PMFCFG2[MSK5:MSK0]             = 0x30; // Branch B<->A, mask C // 180°
PMFCFG3[PINVC,PINVB,PINVA]     = 0x1;  // Invert A

PMFCFG2[MSK5:MSK0]             = 0x03; // Branch B<->C, mask A // 240°
PMFCFG3[PINVC,PINVB,PINVA]     = 0x4;  // Invert C

PMFCFG2[MSK5:MSK0]             = 0x0c; // Branch A<->C, mask B // 300°
PMFCFG3[PINVC,PINVB,PINVA]     = 0x4;  // Invert C

PMFCFG2[MSK5:MSK0]             = 0x30; // Branch A<->B, mask A // 360°
PMFCFG3[PINVC,PINVB,PINVA]     = 0x2;  // Invert B
```

Table 15-48. Bipolar Switching Sequence

Branch	Channel	0°	60°	120°	180°	240°	300°
A	PWM0	PWMgen	Masked	PWMgen		Masked	PWMgen
	PWM1	PWMgen	Masked	PWMgen		Masked	PWMgen
B	PWM2	PWMgen		Masked	PWMgen		Masked
	PWM3	PWMgen		Masked	PWMgen		Masked
C	PWM4	Masked	PWMgen		Masked	PWMgen	
	PWM5	Masked	PWMgen		Masked	PWMgen	

16.3.2.8 SCI Status Register 2 (SCISR2)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-11. SCI Status Register 2 (SCISR2)

Read: Anytime

Write: Anytime

Table 16-12. SCISR2 Field Descriptions

Field	Description
7 AMAP	**Alternative Map** — This bit controls which registers sharing the same address space are accessible. In the reset condition the SCI behaves as previous versions. Setting AMAP=1 allows the access to another set of control and status registers and hides the baud rate and SCI control Register 1. 0 The registers labelled SCIBDH (0x0000),SCIBDL (0x0001), SCICR1 (0x0002) are accessible 1 The registers labelled SCIASR1 (0x0000),SCIACR1 (0x0001), SCIACR2 (0x00002) are accessible
4 TXPOL	**Transmit Polarity** — This bit control the polarity of the transmitted data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
3 RXPOL	**Receive Polarity** — This bit control the polarity of the received data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
2 BRK13	**Break Transmit Character Length** — This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit. 0 Break character is 10 or 11 bit long 1 Break character is 13 or 14 bit long
1 TXDIR	**Transmitter Pin Data Direction in Single-Wire Mode** — This bit determines whether the TXD pin is going to be used as an input or output, in the single-wire mode of operation. This bit is only relevant in the single-wire mode of operation. 0 TXD pin to be used as an input in single-wire mode 1 TXD pin to be used as an output in single-wire mode
0 RAF	**Receiver Active Flag** — RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress 1 Reception in progress

16.5.3.1 Description of Interrupt Operation

The SCI only originates interrupt requests. The following is a description of how the SCI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent. The SCI only has a single interrupt line (SCI Interrupt Signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

16.5.3.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission.Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

16.5.3.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed. Transmission is completed when all bits including the stop bit (if transmitted) have been shifted out and no data is queued to be transmitted. No stop bit is transmitted when sending a break character and the TC flag is set (providing there is no more data queued for transmission) when the break character has been shifted out. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL).TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

16.5.3.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

16.5.3.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

16.5.3.1.5 IDLE Description

The IDLE interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. Once the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

Address & Name		7	6	5	4	3	2	1	0
0x0003 FPSTAT	R	FPOVRD	0	0	0	0	0	0	WSTATACK
	W								
0x0004 FCNFG	R	CCIE	0	ERSAREQ	IGNSF	WSTAT[1:0]		FDFD	FSFD
	W								
0x0005 FERCNFG	R	0	0	0	0	0	0	0	SFDIE
	W								
0x0006 FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
0x0007 FERSTAT	R	0	0	0	0	0	0	DFDF	SFDIF
	W								
0x0008 FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
	W								
0x0009 DFPROT(1)	R	DPOPEN	DPS6	DPS5	DPS4	DPS3	DPS2	DPS1	DPS0
	W								
0x000A FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								
0x000B FRSV1	R	0	0	0	0	0	0	0	0
	W								
0x000C FCCOB0HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000D FCCOB0LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x000E FCCOB1HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000F FCCOB1LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x0010 FCCOB2HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								

Figure 20-4. FTMRZ128K512 Register Summary (continued)

Appendix M
Detailed Register Address Map

Registers listed are a superset of all registers in the S12ZVM-Family.

The device overview section specifies module (version) assignment to individual devices.

M.1 0x0000–0x0003 Part ID

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	PARTID0	R	0	0	0	0	0	0	0	0
		W								
0x0001	PARTID1	R	0	0	0	1	Derivative Dependent (see Table 1-6)			
		W								
0x0002	PARTID2	R	0	0	0	0	0	0	0	0
		W								
0x0003	PARTID3	R	Revision Dependent							
		W								

M.2 0x0010–0x001F S12ZINT

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	IVBR	R	IVB_ADDR[15:8]							
		W								
0x0011		R	IVB_ADDR[7:1]							0
		W								
0x0012-0x0016	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0017	INT_CFADDR	R	0	INT_CFADDR[6:3]				0	0	0
		W								
0x0018	INT_CFDATA0	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x0019	INT_CFDATA1	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001A	INT_CFDATA2	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001B	INT_CFDATA3	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001C	INT_CFDATA4	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001D	INT_CFDATA5	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x001E	INT_CFDATA6	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								