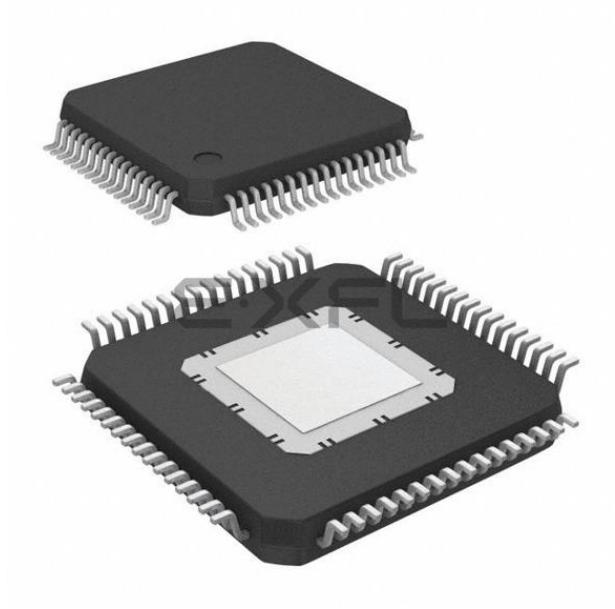

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml31f1mkh

Table 0-1. Revision History

Date	Revision	Description
22 MAY2014	1.4	Updated family derivative table for S12ZVML32, S12ZVM32 and S12ZVM16 devices Added 64KB, 32KB and 16KB derivative information to flash module chapter Added pin routing options for S12ZVM32 and S12ZVM16 devices Added HV Phy information for the S12ZVM32 and S12ZVM16 derivatives Updated Part ID assignment table and ordering information for S12ZVM32 and S12ZVM16 Corrected PLL VCO maximum frequency specification Changed V_{LVLSA} maximum from 7V to 6.9V Added electrical parameter for HD division ratio through the phase multiplexer Corrected preferred VRL reference from VRL_1 to VRL_0 Included NVM timing parameters for the S12ZVM32 and S12ZVM16 devices Added GDU S12ZVM32 and S12ZVM16 specific differences and electrical specifications Added references to f_{WSTAT} Added VDDX short circuit fall back current and temperature/input dependency specs.
22 SEP 2014	1.5	Removed incorrect references to PACLK in TIM chapter Improved clarity of routing options in PIM chapter. Updated S12ZVM- Family derivative table. Added 48LQFP thermal package parameters Extended LINPHY specification range minimum to 5V Updated BKGD pin I/O specification Specified ADC accuracy for a range of VDDA and VREF.
20 MAR 2015	2.0	Added ZVMC256 information Added mask set 2N95G information Added more detailed PTU minimum trigger spacing description Updated CPMU, PIM and GDU chapters for ZVMC256 Improved CPMU specification clarity (see CPMU revision history) Removed electrical parameter classification Added reset startup timing parameter Updated BATS parameters Extended BKGD V_{IL} condition from 3.15V to 3.13V Extended GDU operating range from 26V to 26.6V Temperature sensor output at 150C changed from 2.25V to 2.33V. Added GDU VBS current parameter Updated package thermal information for ZVM32 and ZVM16 parts Added VBG temperature and voltage dependency parameters Added device stop current at 105C.
22 APR 2015	2.1	Updated Stop and Wait current parameter values (I_{SUPS}, I_{SUPW}) Corrected 80LQFP-EP pin name from VSS2 to VSS1 Updated ZVMC256 VDDS regulator parameters. Changed PL0 ESD specification Minor corrections to PIM, PMF, SRAM and ADC chapters (see module revision histories)
27 APR 2015	2.2	Updated Stop current parameter values (I_{SUPS}) Updated LINPHY parameter range limit to 5.5V Added more information about VDDS1, VDDS2, SNPS1, SNPS2 to CPMU chapter. Reintroduced EPRES bit for GDU V4 Added 80LQFP-EP mechanical package information

the capacitor C_{BS} is first charged to VLS_OUT via an external diode (GDUV4) or internal transistor (GDUV5), when the low side driver is active Figure 1-20. When the high side driver switches on, the charge on this capacitor, supplies the FET-predriver via the VBSx pin. The C_{BS} capacitor can only be charged if the low side driver is active, so after a long period of inactivity of the low side driver, the C_{BS} capacitor becomes discharged. In this case, the low side driver must be switched on to charge C_{BS} before commencing high side driving. The time it takes to discharge the bootstrap capacitor C_{BS} can be calculated from the size of the bootstrap capacitor C_{BS} and the current on VBSx pin in the high side inactive phase.

The bootstrap capacitors must be precharged before turning on the high-side drivers for the first time. This can be done by using the PMF software output control mechanism:

```
PMFOUTC = 0x3F;                         // SW control on all outputs
PMFOUTB = 0x2A;                         // All high-sides off, all low-sides on
```

The PWM0 signals should be configured to start with turning on the low-side before the high-side drivers in order to assure precharged bootstraps. Therefore invert the PWM0 signals:

```
PMFCINV = 0x3F;                         // Invert all channels to precharge bootstraps
```

1.13.8.2.2 High Side Charge Pump

A charge pump voltage is used to supply the high side FET-predriver with enough current to maintain the gate source voltage. To generate this voltage an external charge pump is driven by the pin CP, switching between 0V and 11V. The pumped voltage is then applied to the pin VCP.

At 100% duty cycle operation the low-side turn on time is zero during a masked commutation cycle before the attempting to turn on the high side drivers. This can cause bootstrap charge to decay.

In order to speed-up the high-side gate voltage level directly after commutation, the software should drive the first PWM cycle with a duty cycle meeting an on-time of at least $t_{minpulse}$ for the low-side drivers and then switch back to 100% again.

The recommended procedure for BLDC applications is to use the manual correction method (PMFCCTL[ISENS]) as described below:

Set odd PMF values to alternative duty cycle. At commutation event when one of the three high-side drivers is turned on (every 120°) set the PMFCCTL[IPOLx] bits and clear them at the next PWM reload event.

Given unipolar switching mode:

```
// TIM OC0 ISR:
if ((PMFOUTC == 0x1c) || (PMFOUTC == 0x07) || (PMFOUTC == 0x31)) // all high-side turn-on sectors
         PMFCCTL = 0x17; // select odd PMF values

// PMF reload ISR:
         PMFCCTL = 0x10; // select even PMF values
```

The GDU high side drain voltage, pin HD, is supplied from VBAT through a reverse battery protection circuit. In a typical application the charge pump is used to switch on an external NMOS, N1, with source connected to VBAT, by generating a voltage of VBAT+VLS-(2xVdiode). In a reverse battery scenario, the external bipolar turns on, ensuring that the HD pin is isolated from VBAT by the external NMOS, N1.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0284	DDRADH	R	DDRADH7[2]	DDRADH6[2]	DDRADH5[2]	DDRADH4[2]	DDRADH3[2]	DDRADH2[2]	DDRADL1[2]	DDRADH0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	PERADH	R	PERADH7[2]	PERADH6[2]	PERADH5[2]	PERADH4[2]	PERADH3[2]	PERADH2[2]	PERADH1[2]	PERADH0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	PPSADH	R	PPSADH7[2]	PPSADH6[2]	PPSADH5[2]	PPSADH4[2]	PPSADH3[2]	PPSADH2[2]	PPSADH1[2]	PPSADH0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								
0x028A–0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	PIEADH	R	PIEADH7[2]	PIEADH6[2]	PIEADH5[2]	PIEADH4[2]	PIEADH3[2]	PIEADH2[2]	PIEADH1[2]	PIEADH0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								
0x028E	PIFADH	R	PIFADH7[2]	PIFADH6[2]	PIFADH5[2]	PIFADH4[2]	PIFADH3[2]	PIFADH2[2]	PIFADH1[2]	PIFADH0
		W								
0x028F	PIFADL	R	PIFADL7	PIFADL6	PIFADL5	PIFADL4	PIFADL3	PIFADL2	PIFADL1	PIFADL0
		W								
0x0290–0x0297	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0298	DIENADH	R	DIENADH7[2]	DIENADH6[2]	DIENADH5[2]	DIENADH4[2]	DIENADH3[2]	DIENADH2[2]	DIENADH1[2]	DIENADH0
		W								
0x0299	DIENADL	R	DIENADL7	DIENADL6	DIENADL5	DIENADL4	DIENADL3	DIENADL2	DIENADL1	DIENADL0
		W								

2.3.4.6 Port L Polarity Select Register (PPSL)

Address 0x0334 PPSL — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PPSL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-28. Port L Polarity Select Register (PPSL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-32. PPSL Register Field Descriptions

Field	Description
1-0 PPSL0	**Polarity Select** — This bit selects the polarity of the active interrupt edge on the associated HVI pin. 1 Rising edge selected 0 Falling edge selected

2.3.4.7 Port L ADC Bypass Register (PTABYPL)

Address 0x033A — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTABYPL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-29. Port L ADC Bypass Register (PTABYPL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-33. PTABYPL Register Field Descriptions

Field	Description
1-0 PTABYPL0	**Port L ADC Connection Bypass** — This bit bypasses and powers down the impedance converter stage in the signal path from the analog input pin to the ADC channel input. This bit takes effect only if using direct input connection to the ADC channel (PTADIRL=1). 1 Impedance converter bypassed 0 Impedance converter used

5.1.2 Features

The BDC includes these distinctive features:

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

5.1.3 Modes of Operation

S12 devices feature power modes (run, wait, and stop) and operating modes (normal single chip, special single chip). Furthermore, the operation of the BDC is dependent on the device security status.

5.1.3.1 BDC Modes

The BDC features module specific modes, namely disabled, enabled and active. These modes are dependent on the device security and operating mode. In active BDM the CPU ceases execution, to allow BDC system access to all internal resources including CPU internal registers.

5.1.3.2 Security and Operating mode Dependency

In device run mode the BDC dependency is as follows

- Normal modes, unsecure device
  General BDC operation available. The BDC is disabled out of reset.
- Normal modes, secure device
  BDC disabled. No BDC access possible.
- Special single chip mode, unsecure
  BDM active out of reset. All BDC commands are available.
- Special single chip mode, secure
  BDM active out of reset. Restricted command set available.

When operating in secure mode, BDC operation is restricted to allow checking and clearing security by mass erasing the on-chip flash memory. Secure operation prevents BDC access to on-chip memory other than mass erase. The BDC command set is restricted to those commands classified as Always-available.

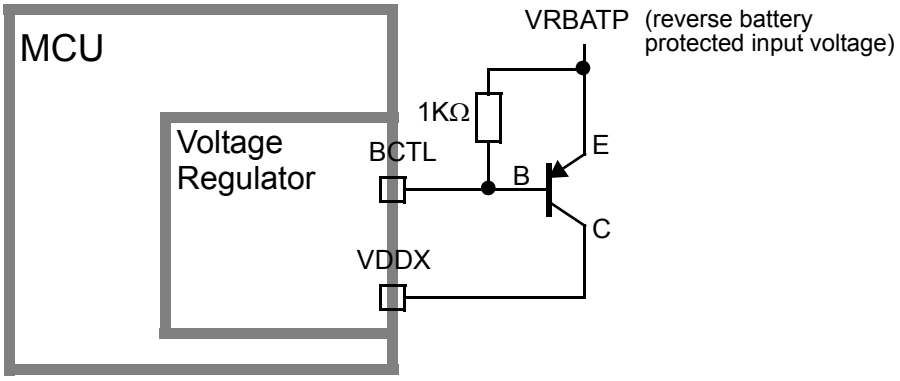

Figure 8-3. BCTL application example

8.2.10 BCTLC — Base Control Pin for external PNP for VDDC power domain

BCTLC is the ballast connection for the on chip voltage regulator for the VDDC power domain. It provides the base current of an external BJT (PNP) of the VDDC supply. An additional 1KΩ resistor between emitter and base of the BJT is required.

8.2.11 BCTLS1 — Base Control Pin for external PNP for VDDS1 power domain

BCTLS1 is the ballast connection for the on chip voltage regulator for the VDDS1 power domain. It provides the base current of an external BJT (PNP) of the VDDS1 supply. An additional 1KΩ resistor between emitter and base of the BJT is required.

Figure 8-4 shows an application example for the external BCTLS1 pin.

8.3.2.19 Autonomous Clock Trimming Register (CPMUACLKTR)

The CPMUACLKTR register configures the trimming of the Autonomous Clock (ACLK - trimmable internal RC-Oscillator) which can be selected as clock source for some CPMU features.

Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
W								
Reset	F	F	F	F	F	F	0	0

After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 8-26. Autonomous Clock Trimming Register (CPMUACLKTR)

Read: Anytime

Write: Anytime

Table 8-20. CPMUACLKTR Field Descriptions

Field	Description
7–2 ACLKTR[5:0]	**Autonomous Clock Period Trimming Bits** — See Table 8-21 for trimming effects. The ACLKTR[5:0] value represents a signed number influencing the ACLK period time.

Table 8-21. Trimming Effect of ACLKTR[5:0]

ACLKTR[5:0]	Decimal	ACLK frequency
100000	-32	lowest
100001	-31	increasing
....		
111111	-1	
000000	0	mid
000001	+1	increasing
....		
011110	+30	
011111	+31	highest

9.5.2.14 ADC End Of List Result Information Register (ADCEOLRI)

This register is cleared when bit ADC_SR is set or bit ADC_EN is clear.

Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-17. ADC End Of List Result Information Register (ADCEOLRI)

Read: Anytime

Write: Never

Table 9-19. ADCEOLRI Field Descriptions

Field	Description
7 CSL_EOL	**Active CSL When "End Of List" Command Type Executed** — This bit indicates the active (used) CSL when a "End Of List" command type has been executed and related data has been stored to RAM. 0 CSL_0 active when "End Of List" command type executed. 1 CSL_1 active when "End Of List" command type executed.
6 RVL_EOL	**Active RVL When "End Of List" Command Type Executed** — This bit indicates the active (used) RVL when a "End Of List" command type has been executed and related data has been stored to RAM. 0 RVL_0 active when "End Of List" command type executed. 1 RVL_1 active when "End Of List" command type executed.

NOTE

The conversion interrupt EOL_IF occurs and simultaneously the register ADCEOLRI is updated when the "End Of List" conversion command type has been processed and related data has been stored to RAM.

9.9.10 Fully Timing Controlled Conversion

As described previously, in “Trigger Mode” a Restart Event automatically causes a trigger. To have full and precise timing control of the beginning of any conversion/sequence the “Restart Mode” is available. In “Restart Mode” a Restart Event does not cause a Trigger automatically; instead, the Trigger must be issued separately and with correct timing, which means the Trigger is not allowed before the Restart Event (conversion command loading) is finished (bit RSTA=1’b0 again). The time required from Trigger until sampling phase starts is given (refer to Section 9.5.2.6, “ADC Conversion Flow Control Register (ADCFLWCTL), Timing considerations) and hence timing is fully controllable by the application. Additionally, if a Trigger occurs before a Restart Event is finished, this causes the TRIG_EIF flag being set. This allows detection of false flow control sequences.

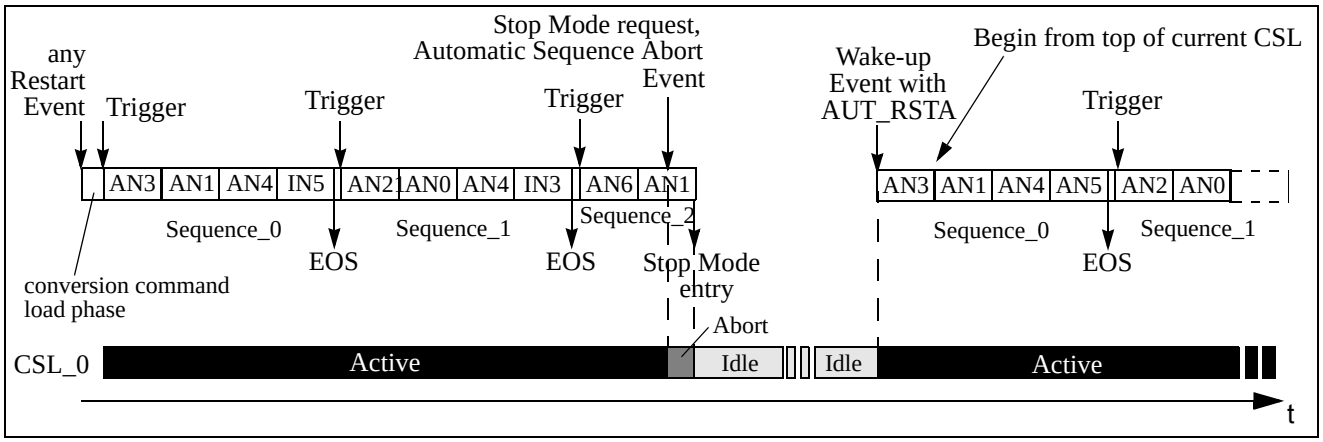

Figure 9-44. Conversion Flow Control Diagram — Fully Timing Controlled Conversion (with Stop Mode)

Unlike the Stop Mode entry shown in Figure 9-43 and Figure 9-44 it is recommended to issue the Stop Mode at sequence boundaries (when ADC is idle and no conversion/conversion sequence is ongoing).

Any of the Conversion flow control application use cases described above (Continuous, Triggered, or Fully Timing Controlled Conversion) can be used with CSL single buffer mode or with CSL double buffer mode. If using CSL double buffer mode, CSL swapping is performed by issuing a Restart Event with bit LDOK set.

Setting OCPDx to zero allows the internal register to drive the programmed state to OCx. This allows a glitch free switch over of port from general purpose I/O to timer output once the OCPDx bit is set to zero.

11.5 Resets

The reset state of each individual bit is listed within Section 11.3, “Memory Map and Register Definition” which details the registers and their bit fields

11.6 Interrupts

This section describes interrupts originated by the TIM16B4CV3 block. Table 11-18 lists the interrupts generated by the TIM16B4CV3 to communicate with the MCU.

Table 11-18. TIM16B4CV3 **Interrupts**

Interrupt	Offset	Vector	Priority	Source	Description
C[3:0]F	—	—	—	Timer Channel 3–0	Active high timer channel interrupts 3–0
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

The TIM16B4CV3 could use up to 5 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

11.6.1 Channel [3:0] Interrupt (C[3:0]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 0 interrupt. The TIM block only generates the interrupt and does not service it. Only bits related to implemented channels are valid.

11.6.2 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt. The TIM block only generates the interrupt and does not service it.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 CANCTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
	W								
0x0001 CANCTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
	W								
0x0002 CANBTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
	W								
0x0003 CANBTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
	W								
0x0004 CANRFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
	W								
0x0005 CANRIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
	W								
0x0006 CANTFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
	W								
0x0007 CANTIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
	W								
0x0008 CANTARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
	W								
0x0009 CANTAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
	W								
0x000A CANTBSEL	R	0	0	0	0	0	TX2	TX1	TX0
	W								
0x000B CANIDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
	W								
0x000C Reserved	R	0	0	0	0	0	0	0	0
	W								
0x000D CANMISC	R	0	0	0	0	0	0	0	BOHOLD
	W								

= Unimplemented or Reserved

Figure 13-3. MSCAN Register Summary

Table 15-25. PMFENCA Field Descriptions (continued)

Field	Description
1 LDOKA	**Load Okay A** — When MTG is clear, this bit allows loads of the PRSCA bits, the PMFMODA register, and the PMFVAL0-5 registers into a set of buffers. The buffered prescaler A divisor, PWM counter modulus A value, and all PWM pulse widths take effect at the next PWM reload. When MTG is set, this bit allows loads of the PRSCA bits, the PMFMODA register, and the PMFVAL0–1 registers into a set of buffers. The buffered prescaler divisor A, PWM counter modulus A value, and PWM0–1 pulse widths take effect at the next PWM reload. Set LDOKA by reading it when it is logic zero and then writing a logic one to it. LDOKA is automatically cleared after the new values are loaded, or can be manually cleared before a reload by writing a logic zero to it. Reset clears LDOKA. 0 Do not load new modulus A, prescaler A, and PWM0–1 (2–5 if MTG = 0) values 1 Load prescaler A, modulus A, and PWM0–1 (2–5 if MTG = 0) values **Note:** Do not set PWMENA bit before setting the LDOKA bit and do not clear the LDOKA bit at the same time as setting the PWMENA bit.
0 PWMRIEA	**PWM Reload Interrupt Enable A** — This bit enables the PWMRFA flag to generate CPU interrupt requests. 0 PWMRFA CPU interrupt requests disabled 1 PWMRFA CPU interrupt requests enabled

15.3.2.20 PMF Frequency Control A Register (PMFFQCA)

Address: Module Base + 0x0021 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	LDFQA				HALFA	PRSCA		PWMRFA
Reset	0	0	0	0	0	0	0	0

Figure 15-25. PMF Frequency Control A Register (PMFFQCA)

1. Read: Anytime
   Write: Anytime

Table 15-26. PMFFQCA Field Descriptions

Field	Description
7–4 LDFQA[3:0]	**Load Frequency A** — This field selects the PWM load frequency according to Table 15-27. See Section 15.4.12.3, “Load Frequency” for more details. **Note:** The LDFQA field takes effect when the current load cycle is complete, regardless of the state of the LDOKA bit or global load OK. Reading the LDFQA field reads the buffered value and not necessarily the value currently in effect.
3 HALFA	**Half Cycle Reload A** — This bit enables half-cycle reloads in center-aligned PWM mode. This bit has no effect on edge-aligned PWMs. It takes effect immediately. When set, reload opportunities occur also when the counter matches the modulus in addition to the start of the PWM period at count zero. See Section 15.4.12.3, “Load Frequency” for more details. 0 Half-cycle reloads disabled 1 Half-cycle reloads enabled
2–1 PRSCA[1:0]	**Prescaler A** — This buffered field selects the PWM clock frequency illustrated in Table 15-28. **Note:** Reading the PRSCA field reads the buffered value and not necessarily the value currently in effect. The PRSCA field takes effect at the beginning of the next PWM cycle and only when the LDOKA bit or global load OK is set.

Table 20-17. FSTAT Field Descriptions (continued)

Field	Description
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. The MGSTAT bits are cleared automatically at the start of the execution of a Flash command. See Section 20.4.7, “Flash Command Description,” and Section 20.6, “Initialization” for details.

20.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Offset Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 20-18. FERSTAT Field Descriptions

Field	Description
1 DFDF	**Double Bit Fault Detect Flag** — The setting of the DFDF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.(1) The DFDF flag is cleared by writing a 1 to DFDF. Writing a 0 to DFDF has no effect on DFDF.(2) 0 No double bit fault detected 1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running. See Section 20.4.3, “Flash Block Read Access” for details
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation. The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted while command running

1. In case of ECC errors the corresponding flag must be cleared for the proper setting of any further error, i.e. any new error will only be indicated properly when DFDF and/or SFDIF are clear at the time the error condition is detected.

2. There is a one cycle delay in storing the ECC DFDF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

SNPS2 pins. These pins are intended to interface to external components operating in the automotive battery range. They have nominal voltages above the standard 5V I/O voltage range.

A.1.2.3 Oscillator

If the designated EXTAL and XTAL pins are configured for external oscillator operation then these pins have a nominal voltage of 1.8 V.

A.1.2.4 TEST

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.

A.1.3 Current Injection

Power supply must maintain regulation within operating V_{DDX} or V_{DD} range during instantaneous and operating maximum current conditions. **Figure A-1.** shows a 5 V GPIO pad driver and the on chip voltage regulator with VDDX output. It shows also the power and ground pins VSUP, VDDX, VSSX and VSSA. Px represents any 5 V GPIO pin. Assume Px is configured as an input. The pad driver transistors P1 and N1 are switched off (high impedance). If the voltage V_{in} on Px is greater than V_{DDX} a positive injection current I_{in} will flow through diode D1 into VDDX node. If this injection current I_{in} is greater than I_{Load}, the internal power supply VDDX may go out of regulation. Ensure the external V_{DDX} load will shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming

Appendix C
ADC Electrical Specifications

NOTE: ADC1 is only tested to 10-bit accuracy in the 48LQFP-EP package options.

NOTE: VRL_0 is the preferred reference for low noise.

NOTE: (ZVMC256 only) When using VDDS2 or VDDS1 as the VRH reference, the reference is impacted by a drop of between 4mV and 15mV across the internal short circuit protection switch.

C.1 ADC Operating Characteristics

The Table C-1 shows conditions under which the ADC operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$.

This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table C-1. ADC Operating Characteristics

Supply voltage 4.5 V < V_{DDA} < 5.5 V, Junction Temperature From –40×°C To +175°C							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Reference potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$	 — —	 $V_{DDA}/2$ V_{DDA}	 V V
2		Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	-0.1	0	0.1	V
3		Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.1	0	0.1	V
4		Differential reference voltage[1]	V_{RH}-V_{RL}	3.13	5.0	5.5	V
5		ADC Clock Frequency (derived from bus clock via the prescaler).	f_{ATDCLK}	0.25	—	8.33	MHz
6		Buffer amplifier turn on time (delay after module start/recovery from Stop mode)	t_{REC}	—	—	1	μs
7		ADC disable time	$t_{DISABLE}$	—	—	3	bus clock cycles
8		ADC Conversion Period [2] 12 bit resolution: 10 bit resolution: 8 bit resolution:	 N_{CONV12} N_{CONV10} N_{CONV8}	 19 18 16	 — — —	 39 38 36	 ADC clock cycles

1. Full accuracy is not guaranteed when differential voltage is less than 4.50 V

2. The minimum time assumes a sample time of 4 ATD clock cycles; maximum time assumes a sample time of 24 ATD clock cycles.

M.2 0x0010–0x001F S12ZINT

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001F	INT_CFDATA7	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x029A–0x02BF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02C0	PTT	R	0	0	0	0	PTT3	PTT2	PTT1	PTT0
		W								
0x02C1	PTIT	R	0	0	0	0	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x02C2	DDRT	R	0	0	0	0	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x02C3	PERT	R	0	0	0	0	PERT3	PERT2	PERT1	PERT0
		W								
0x02C4	PPST	R	0	0	0	0	PPST3	PPST2	PPST1	PPST0
		W								
0x02C5–0x02CF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02D0	PTS	R	0	0	PTS5[(5)]	PTS4[5]	PTS3	PTS2	PTS1	PTS0
		W								
0x02D1	PTIS	R	0	0	PTIS5[5]	PTIS4[5]	PTIS3	PTIS2	PTIS1	PTIS0
		W								
0x02D2	DDRS	R	0	0	DDRS5[5]	DDRS4[5]	DDRS3	DDRS2	DDRS1	DDRS0
		W								
0x02D3	PERS	R	0	0	PERS5[5]	PERS4[5]	PERS3	PERS2	PERS1	PERS0
		W								
0x02D4	PPSS	R	0	0	PPSS5[5]	PPSS4[5]	PPSS3	PPSS2	PPSS1	PPSS0
		W								
0x02D5	Reserved	R	0	0	0	0	0	0	0	0
		W								

M.6 0x0380-0x039F FTMRZ128K512 (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0396	FCCOB5HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0397	FCCOB5LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								

M.7 0x03C0-0x03CF SRAM_ECC_32D7P

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x03C0	ECCSTAT	R	0	0	0	0	0	0	0	RDY
		W								
0x03C1	ECCIE	R	0	0	0	0	0	0	0	SBEEIE
		W								
0x03C2	ECCIF	R	0	0	0	0	0	0	0	SBEEIF
		W								
0x03C3 - 0x03C6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C7	ECCDPTRH	R	DPTR[23:16]							
		W								
0x03C8	ECCDPTRM	R	DPTR[15:8]							
		W								
0x03C9	ECCDPTRL	R	DPTR[7:1]							0
		W								
0x03CA - 0x03CB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03CC	ECCDDH	R	DDATA[15:8]							
		W								
0x03CD	ECCDDL	R	DDATA[7:0]							
		W								
0x03CE	ECCDE	R	0	0	DECC[5:0]					
		W								
0x03CF	ECCDCMD	R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
		W								

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0412	TIM1TC1H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0413	TIM1TC1L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0414– 0x042B	Reserved	R W								
0x042C	TIM1OCPD	R W							OCPD1	OCPD0
0x042D	Reserved	R W								
0x042E	TIM1PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x042F	Reserved	R W								

M.9 0x0480-0x04AF PWM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0480	PWME	R W	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
0x0481	PWMPOL	R W	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
0x0482	PWMCLK	R W	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
0x0483	PWMPRCLK	R W	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
0x0484	PWMCAE	R W	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
0x0485	PWMCTL	R W	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
0x0486	PWMCLKAB	R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
0x0487	RESERVED	R W	0	0	0	0	0	0	0	0
0x0488	PWMSCLA	R W	Bit 7	6	5	4	3	2	1	Bit 0

M.9 0x0480-0x04AF PWM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x049B	PWMPER7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049C	PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049D	PWMDTY1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049E	PWMDTY2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049F	PWMDTY32	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A0	PWMDTY42	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A1	PWMDTY52	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A2	PWMDTY62	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A3	PWMDTY72	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A4 - 0x04AF	RESERVED	R W	0	0	0	0	0	0	0	0

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0500	PMFCFG0	R W	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
0x0501	PMFCFG1	R W	0	ENCE	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
0x0502	PMFCFG2	R W	REV1	REV0	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
0x0503	PMFCFG3	R W	PMFWAI	PMFFRZ	0	VLMODE		PINVC	PINVB	PINVA
0x0504	PMFFEN	R W	0	FEN5	0	FEN4	FEN3	FEN2	FEN1	FEN0
0x0505	PMFFMOD	R W	0	FMOD5	0	FMOD4	FMOD3	FMOD2	FMOD1	FMOD0