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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	40MHz
Connectivity	LINbus, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-LQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml31f1wkf

- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)
- Trace control
  - Tracing session triggered by state sequencer
  - Begin, End, and Mid alignment of tracing to trigger
- Four trace modes
  - Normal: change of flow (COF) PC information is stored (see Section 6.4.5.2.1) for change of flow definition.
  - Loop1: same as Normal but inhibits consecutive duplicate source address entries
  - Detail: address and data for all read/write access cycles are stored
  - Pure PC: All program counter addresses are stored.
- 2 Pin (data and clock) profiling interface
  - Output of code flow information

6.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

The DBG module can issue breakpoint requests to force the device to enter active BDM or an SWI ISR. The BDC BACKGROUND command is also handled by the DBG to force the device to enter active BDM. When the device enters active BDM through a BACKGROUND command with the DBG module armed, the DBG remains armed.

8.1.4 S12CPMU_UHV_V10_V6 Block Diagram

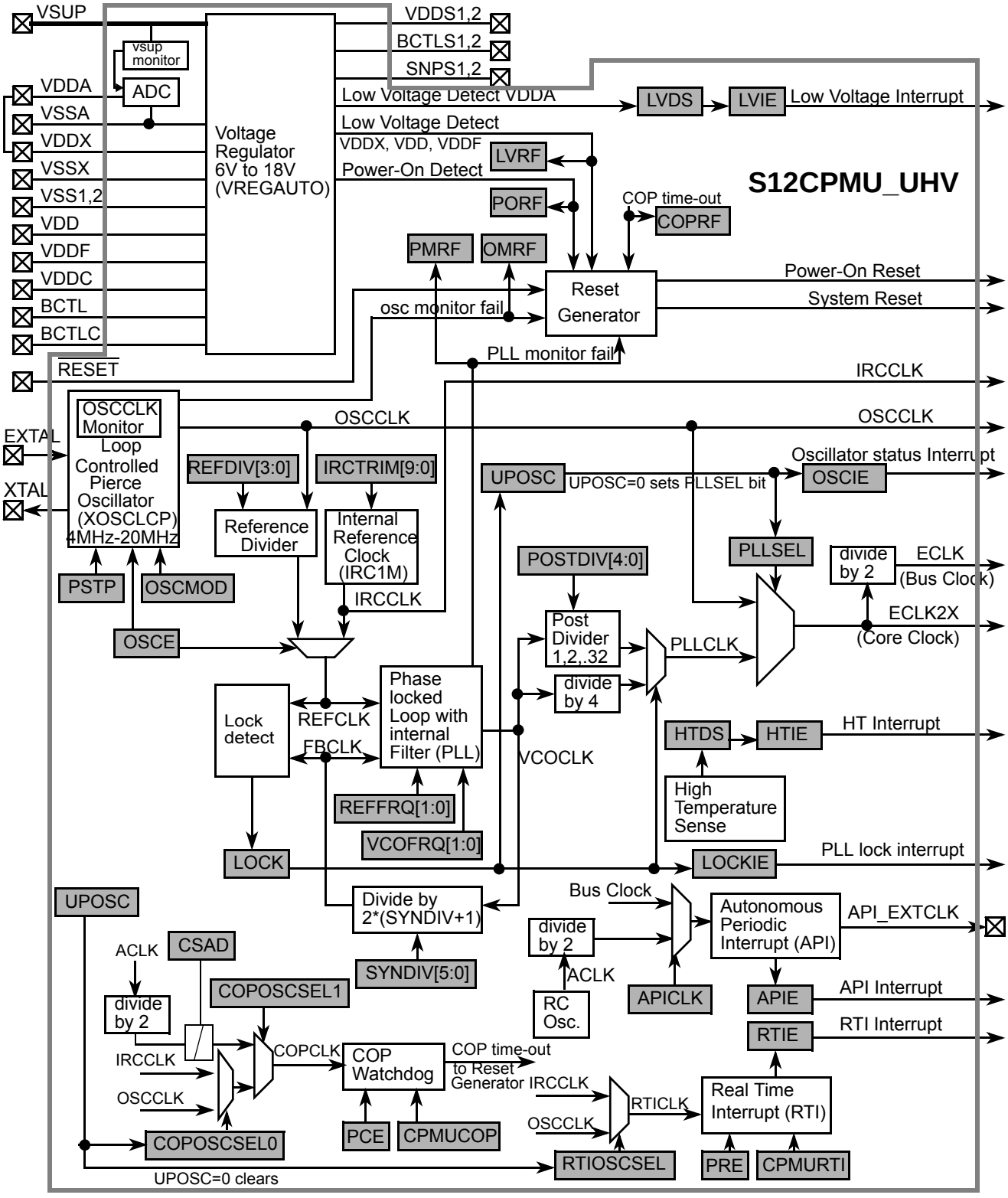

Figure 8-1. Block diagram of S12CPMU_UHV_V10_V6

8.5.4 PLL Clock Monitor Reset

In case of loss of PLL clock oscillation or the PLL clock frequency is below the failure assert frequency f_{PMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V10_V6 generates a PLL Clock Monitor Reset. In Full Stop Mode the PLL and the PLL clock monitor are disabled.

8.5.5 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus COP reset is generated.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit.

Depending on the COP configuration there might be a significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

Table 8-36 gives an overview of the COP condition (run, static) in Stop Mode depending on legal configuration and status bit settings:

Table 8-36. COP condition (run, static) in Stop Mode

COPOSCSEL1	CSAD	PSTP	PCE	COPOSCSEL0	OSCE	UPOSC	COP counter behavior in Stop Mode (clock source)
1	0	x	x	x	x	x	Run (ACLK)
1	1	x	x	x	x	x	Static (ACLK)
0	x	1	1	1	1	1	Run (OSCCLK)
0	x	1	1	0	0	x	Static (IRCCLK)
0	x	1	1	0	1	x	Static (IRCCLK)
0	x	1	0	0	x	x	Static (IRCCLK)
0	x	1	0	1	1	1	Static (OSCCLK)
0	x	0	1	1	1	1	Static (OSCCLK)
0	x	0	1	0	1	x	Static (IRCCLK)
0	x	0	1	0	0	0	Static (IRCCLK)
0	x	0	0	1	1	1	Satic (OSCCLK)
0	x	0	0	0	1	1	Static (IRCCLK)
0	x	0	0	0	1	0	Static (IRCCLK)
0	x	0	0	0	0	0	Static (IRCCLK)

9.5.2.6 ADC Conversion Flow Control Register (ADCFLWCTL)

Bit set and bit clear instructions should not be used to access this register.

When the ADC is enabled the bits of ADCFLWCTL register can be modified after a latency time of three Bus Clock cycles.
All bits are cleared if bit ADC_EN is clear or via ADC soft-reset.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-9. ADC Conversion Flow Control Register (ADCFLWCTL)

Read: Anytime

Write:

- Bits SEQA, TRIG, RSTA, LDOK can only be set if bit ADC_EN is set.
- Writing 1’b0 to any of these bits does not have an effect

Timing considerations (Trigger Event - channel sample start) depending on ADC mode configuration:

- Restart Mode
  When the Restart Event has been processed (initial command of current CSL is loaded) it takes two Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from the Trigger Event (bit TRIG set) until the select channel starts to sample.
  During a conversion sequence (back to back conversions) it takes five Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from current conversion period end until the newly selected channel is sampled in the following conversion period.
- Trigger Mode
  When a Restart Event occurs a Trigger Event is issued simultaneously. The time required to process the Restart Event is mainly defined by the internal read data bus availability and therefore can vary. In this mode the Trigger Event is processed immediately after the Restart Event is finished and both conversion flow control bits are cleared simultaneously. From de-assert of bit TRIG until sampling begins five Bus Clock cycles are required. Hence from occurrence of a Restart Event until channel sampling it takes five Bus Clock cycles plus an uncertainty of a few Bus Clock cycles.

For more details regarding the sample phase please refer to Section 9.6.2.2, “Sample and Hold Machine with Sample Buffer Amplifier.

Table 9-10. ADCFLWCTL Field Descriptions (continued)

Field	Description
5 RSTA	**Restart Event (Restart from Top of Command Sequence List)** — This bit indicates that a Restart Event is executed. The ADC loads the conversion command from top of the active Sequence Command List when no conversion or conversion sequence is ongoing. This bit is cleared when the first conversion command of the sequence from top of active Sequence Command List has been loaded into the ADCCMD register. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. Data Bus Control: This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. Writing a one to this bit does not clear it but causes an overrun if the bit has already been set. See also Section 9.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. Internal Interface Control: This bit can be controlled via the internal interface Signal "Restart" if access control is configured accordingly via ACC_CFG[1:0]. After being set an additional request via internal interface Signal "Restart" causes an overrun. See conversion flow control in case of overrun situations for more details. General: In conversion flow control mode "Trigger Mode" when bit RSTA gets set bit TRIG is set simultaneously if one of the following has been executed: - "End Of List" command type has been executed or is about to be executed - Sequence Abort Event 0 Continue with commands from active Sequence Command List. 1 Restart from top of active Sequence Command List.
4 LDOK	**Load OK for alternative Command Sequence List** — This bit indicates if the preparation of the alternative Sequence Command List is done and Command Sequence List must be swapped with the Restart Event. This bit is cleared when bit RSTA is set (Restart Event executed) and the Command Sequence List got swapped. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. This bit is forced to zero if bit CSL_BMOD is clear. Data Bus Control: This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. To set bit LDOK the bits LDOK and RSTA must be written simultaneously. After being set this bit can not be cleared by writing a value of 1'b1. See also Section 9.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. Internal Interface Control: This bit can be controlled via the internal interface Signal "LoadOK" and "Restart" if access control is configured accordingly via ACC_CFG[1:0]. With the assertion of Interface Signal "Restart" the interface Signal "LoadOK" is evaluated and bit LDOK set accordingly (bit LDOK set if Interface Signal "LoadOK" asserted when Interface Signal "Restart" asserts). General: Only in "Restart Mode" if a Restart Event occurs without bit LDOK being set the error flag LDOK_EIF is set except when the respective Restart Request occurred after or simultaneously with a Sequence Abort Request. The LDOK_EIF error flag is also not set in "Restart Mode" if the first Restart Event occurs after: - ADC got enabled - Exit from Stop Mode - ADC Soft-Reset 0 Load of alternative list done. 1 Load alternative list.

11.2 External Signal Description

The TIM16B4CV3 module has a selected number of external pins. Refer to device specification for exact number.

11.2.1 IOC3 - IOC0 — Input Capture and Output Compare Channel 3-0

Those pins serve as input capture or output compare for TIM16B4CV3 channel .

NOTE

For the description of interrupts see Section 11.6, “Interrupts”.

11.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

11.3.1 Module Memory Map

The memory map for the TIM16B4CV3 module is given below in Figure 11-3. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B4CV3 module and the address offset for each register.

11.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Only bits related to implemented channels are valid.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	RESERVED	RESERVED	RESERVED	RESERVED	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	RESERVED	RESERVED	RESERVED	RESERVED	FOC3	FOC2	FOC1	FOC0
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
	W								
0x0007 TTOV	R	RESERVED	RESERVED	RESERVED	RESERVED	TOV3	TOV2	TOV1	TOV0
	W								
0x0008 TCTL1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								

Figure 11-3. TIM16B4CV3 Register Summary (Sheet 1 of 2)

11.3.2.11 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-17. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 .

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 11-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

13.3.3.3 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.

Module Base + 0x00XC

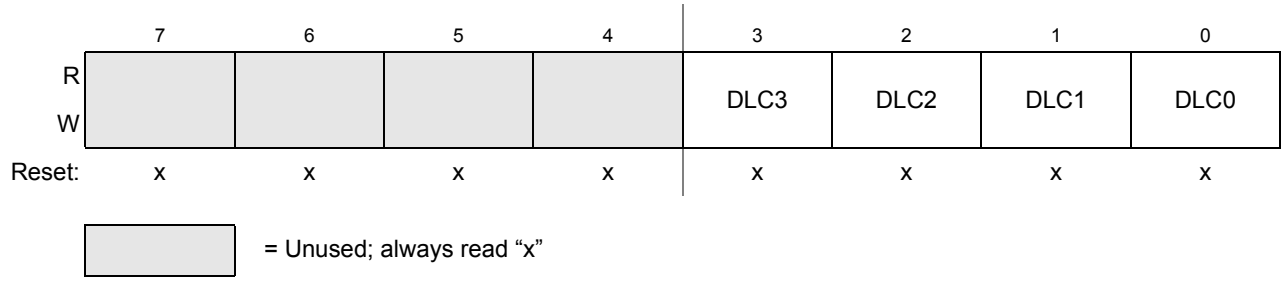

Figure 13-35. Data Length Register (DLR) — Extended Identifier Mapping

Table 13-33. DLR Register Field Descriptions

Field	Description
3-0 DLC[3:0]	**Data Length Code Bits** — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 13-34 shows the effect of setting the DLC bits.

Table 13-34. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

13.3.3.4 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.

15.2 Signal Descriptions

If the signals are not used exclusively internally, the PMF has external pins named PWM0–5, FAULT0–5, and $\overline{IS0}$–$\overline{IS2}$. Refer to device overview section.

15.2.1 PWM0–PWM5 Pins

PWM0–PWM5 are the output signals of the six PWM channels.

NOTE

On MCUs with an integrated gate drive unit the PWM outputs are connected internally to the GDU inputs. In these cases the PWM signals may optionally be available on pins for monitoring purposes. Refer to the device overview section for routing options and pin locations.

15.2.2 FAULT0–FAULT5 Pins

FAULT0–FAULT5 are input signals for disabling selected PWM outputs (FAULT0-3) or drive the outputs to a configurable active/inactive state (FAULT4-5).

NOTE

On MCUs with an integrated gate drive unit (GDU) either one or more FAULT inputs may be connected internally or/and available on an external pin. Refer to the device overview section for availability and pin locations.

15.2.3 $\overline{IS0}$–$\overline{IS2}$ Pins

$\overline{IS0}$–$\overline{IS2}$ are current status signals for top/bottom pulse width correction in complementary channel operation while deadtime is asserted.

NOTE

Refer to the device overview section for signal availability on pins.

15.2.4 Global Load OK Signal — glb_ldok

This device-internal PMF input signal is connected to the global load OK bit at integration level. For each of the three PWM generator time bases the use of the global load OK input can be enabled individually (GLDOKA,B,C).

15.2.5 Commutation Event Signal — async_event

This device-internal PMF input signal is connected to the source of the asynchronous event generator (preferably timer output compare channel) at integration level.

The commutation event input must be enabled to take effect (ENCE=1). When this bit is set the PMFOUTC, PMFOUT, and MSKx registers switch from non-buffered to async_event triggered double

Table 15-7. PMFCFG1 Field Descriptions (continued)

Field	Description
4 TOPNEGC	**Pair C Top-Side PWM Polarity** — This bit determines the polarity for Pair C top-side PWM (PWM4). This bit cannot be modified after the WP bit is set. 0 Positive PWM4 polarity 1 Negative PWM4 polarity
3 BOTNEGB	**Pair B Bottom-Side PWM Polarity** — This bit determines the polarity for Pair B bottom-side PWM (PWM3). This bit cannot be modified after the WP bit is set. 0 Positive PWM3 polarity 1 Negative PWM3 polarity
2 TOPNEGB	**Pair B Top-Side PWM Polarity** — This bit determines the polarity for Pair B top-side PWM (PWM2). This bit cannot be modified after the WP bit is set. 0 Positive PWM2 polarity 1 Negative PWM2 polarity
1 BOTNEGA	**Pair A Bottom-Side PWM Polarity** — This bit determines the polarity for Pair A bottom-side PWM (PWM1). This bit cannot be modified after the WP bit is set. 0 Positive PWM1 polarity 1 Negative PWM1 polarity
0 TOPNEGA	P**air A Top-Side PWM Polarity** — This bit determines the polarity for Pair A top-side PWM (PWM0). This bit cannot be modified after the WP bit is set. 0 Positive PWM0 polarity 1 Negative PWM0 polarity

15.3.2.3 PMF Configure 2 Register (PMFCFG2)

Address: Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	REV1	REV0	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
Reset	0	0	0	0	0	0	0	0

Figure 15-5. PMF Configure 2 Register (PMFCFG2)

1. Read: Anytime
   Write: Anytime except REV[1:0] which cannot be modified after the WP bit is set[1].

Table 15-8. PMFCFG2 Field Descriptions

Field	Description
7-6 REV[1:0]	Select timebase counter to output reload event on pmf_reloada These bits select if timebase generator A, B or C provides the reload event on output signal pmf_reloada. This register cannot be modified after the WP bit is set.(1) 00 Reload event generation disabled 01 PWM generator A generates reload event 10 PWM generator B generates reload event 11 PWM generator C generates reload event

Table 15-10. PMFFEN Field Descriptions

Field	Description
6,4-0 FEN[5:0]	Fault *m* Enable — This register cannot be modified after the WP bit is set. 0 FAULT*m* input is disabled 1 FAULT*m* input is enabled for fault protection *m* is 0, 1, 2, 3, 4 and 5

15.3.2.6 PMF Fault Mode Register (PMFFMOD)

Address: Module Base + 0x0005 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	FMOD5	0	FMOD4	FMOD3	FMOD2	FMOD1	FMOD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-8. PMF Fault Mode Register (PMFFMOD)

1. Read: Anytime
   Write: Anytime

Table 15-11. PMFFMOD Field Descriptions

Field	Description
6,4-0 FMOD[5:0]	**Fault *m* Pin Recovery Mode** — This bit selects automatic or manual recovery of FAULT*m* input faults. See Section 15.4.13.2, “Automatic Fault Recovery” and Section 15.4.13.3, “Manual Fault Recovery” for more details. 0 Manual fault recovery of FAULT*m* input faults 1 Automatic fault recovery of FAULT*m* input faults *m* is 0, 1, 2, 3, 4 and 5.

15.3.2.7 PMF Fault Interrupt Enable Register (PMFFIE)

Address: Module Base + 0x0006 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	FIE5	0	FIE4	FIE3	FIE2	FIE1	FIE0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-9. PMF Fault Interrupt Enable Register (PMFFIE)

1. Read: Anytime
   Write: Anytime

15.3.2.24 PMF Enable Control B Register (PMFENCB)

Address: Module Base + 0x0028 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PWMENB	GLDOKB	0	0	0	RSTRTB	LDOKB	PWMRIEB
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-29. PMF Enable Control B Register (PMFENCB)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set.GLDOKB and RSTRTB cannot be modified after the WP bit is set.

Table 15-29. PMFENCB Field Descriptions

Field	Description
7 PWMENB	**PWM Generator B Enable** — If MTG is clear, this bit reads zero and cannot be written. If MTG is set, this bit when set enables the PWM generator B and the PWM2 and PWM3 outputs. When PWMENB is clear, PWM generator B is disabled, and the PWM2 and PWM3 outputs are in their inactive states unless the corresponding OUTCTL bits are set. After setting this bit a reload event is generated at the beginning of the PWM cycle. 0 PWM generator B and PWM2–3 outputs disabled unless the respective OUTCTL bit is set 1 PWM generator B and PWM2–3 outputs enabled
6 GLDOKB	**Global Load Okay B** — When this bit is set, a PMF external global load OK defined on device level replaces the function of LDOKB. This bit cannot be modified after the WP bit is set. 0 LDOKB controls double reload of buffered registers 1 PMF external global load OK controls reload of double buffered registers
2 RSTRTB	**Restart Generator B** — When this bit is set, PWM generator B will be restarted at the next commutation event. This bit cannot be modified after the WP bit is set. 0 No PWM generator B restart at the next commutation event 1 PWM generator B restart at the next commutation event
1 LDOKB	**Load Okay B** — If MTG is clear, this bit reads zero and cannot be written. If MTG is set, this bit loads the PRSCB bits, the PMFMODB register and the PMFVAL2-3 registers into a set of buffers. The buffered prescaler divisor B, PWM counter modulus B value, PWM2–3 pulse widths take effect at the next PWM reload. Set LDOKB by reading it when it is logic zero and then writing a logic one to it. LDOKB is automatically cleared after the new values are loaded, or can be manually cleared before a reload by writing a logic zero to it. Reset clears LDOKB. 0 Do not load new modulus B, prescaler B, and PWM2–3 values 1 Load prescaler B, modulus B, and PWM2–3 values **Note:** Do not set PWMENB bit before setting the LDOKB bit and do not clear the LDOKB bit at the same time as setting the PWMENB bit.
0 PWMRIEB	**PWM Reload Interrupt Enable B** — If MTG is clear, this bit reads zero and cannot be written. If MTG is set, this bit enables the PWMRFB flag to generate CPU interrupt requests. 0 PWMRFB CPU interrupt requests disabled 1 PWMRFB CPU interrupt requests enabled

15.3.2.31 PMF Counter C Register (PMFCNTC)

Address: Module Base + 0x0032 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFCNTC														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-36. PMF Counter C Register (PMFCNTC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Never

This register displays the state of the 15-bit PWM C counter.

15.3.2.32 PMF Counter Modulo C Register (PMFMODC)

Address: Module Base + 0x0034 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PMFMODC														
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-37. PMF Counter Modulo C Register (PMFMODC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set. Do not write a modulus value of zero for center-aligned operation. Do not write a modulus of zero or one in edge-aligned mode.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods.

NOTE

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKC bit or global load OK is set and the next PWM load cycle begins. Reading PMFMODC returns the value in the buffer. It is not necessarily the value the PWM generator A is currently using.

15.3.2.33 PMF Deadtime C Register (PMFDTMC)

Address: Module Base + 0x0036 Access: User read/write(1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PMFDTMC											
W																
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Figure 15-38. PMF Deadtime C Register (PMFDTMC)

1. Read: Anytime. Returns zero if MTG is clear.
   Write: Anytime if MTG is set.This register cannot be modified after the WP bit is set.

1. The address bit identifies the frame as an address character. See Section 16.4.6.6, “Receiver Wakeup”.

16.4.4 Baud Rate Generation

A 16-bit modulus counter in the two baud rate generator derives the baud rate for both the receiver and the transmitter. The value from 0 to 65535 written to the SBR15:SBR0 bits determines the baud rate. The value from 0 to 4095 written to the SBR15:SBR4 bits determines the baud rate clock with SBR3:SBR0 for fine adjust. The SBR bits are in the SCI baud rate registers (SCIBDH and SCIBDL) for both transmit and receive baud generator. The baud rate clock is synchronized with the bus clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver has an acquisition rate of 16 samples per bit time.

Baud rate generation is subject to one source of error:

- Integer division of the bus clock may not give the exact target frequency.

Table 16-16 lists some examples of achieving target baud rates with a bus clock frequency of 25 MHz.

When IREN = 0 then,

SCI baud rate = SCI bus clock / (SCIBR[15:0])

Table 16-16. Baud Rates (Example: Bus Clock = 25 MHz)

Bits SBR[15:0]	Receiver(1) Clock (Hz)	Transmitter(2) Clock (Hz)	Target Baud Rate	Error (%)
109	3669724.8	229,357.8	230,400	.452
217	1843318.0	115,207.4	115,200	.006
651	614439.3	38,402.5	38,400	.006
1302	307219.7	19,201.2	19,200	.006
2604	153,609.8	9600.6	9,600	.006
5208	76,804.9	4800.3	4,800	.006
10417	38,398.8	2399.9	2,400	.003
20833	19,200.3	1200.02	1,200	.00
41667	9599.9	600.0	600	.00
65535	6103.6	381.5		

1. 16x faster then baud rate

2. divide 1/16 form transmit baud generator

18.3.2.13 GDU Phase Log Register (GDUPHL)

Module Base + 0x000C — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	GPHL[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-15. GDU Phase Log Register (GDUPHL)

1. Read: Anytime
   Write: never

Table 18-16. GDU Phase Log Register Field Descriptions

Field	Description
2:0 GPHL	GDU Phase Log Bits— If a desaturation error occurs the phase status bits GPHS[2:0] in register GDUSTAT are copied to this register. The GDUPHL register is cleared only on reset. See Section 18.4.5, “Desaturation Error

18.3.2.14 GDU Clock Control Register 2 (GDUCLK2)

Module Base + 0x000D — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	GCPCD[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-16. GDU Clock Control Register 2 (GDUCLK2)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-17. GDUCLK2 Register Field Descriptions

Field	Description
3-0 GCPCD[3:0]	GDU Charge Pump Clock Divider — These bits select the clock divider factor which is used to divide down the bus clock frequency f_{BUS} for the charge pump clock f_{CP}. See Table 18-18 for divider factors. These bits cannot be modified after GWP bit is set. See also Section 18.4.4, “Charge Pump

NOTE

The GCPCD bits must be set to the required value before GCPE bit is set. If a different charge pump clock frequency is required GCPE has to be cleared before new values to GCPCD bits are written.

20.3 Memory Map and Registers

This section describes the memory map and registers for the Flash module. Read data from unimplemented memory space in the Flash module is undefined. Write access to unimplemented or reserved memory space in the Flash module will be ignored by the Flash module.

Writing to the Flash registers while a Flash command is executing (that is indicated when the value of flag CCIF reads as ’0’) is not allowed. If such action is attempted, the result of the write operation will be unpredictable.

Writing to the Flash registers is allowed when the Flash is not busy executing commands (CCIF = 1) and during initialization right after reset, despite the value of flag CCIF in that case (refer to Section 20.6 for a complete description of the reset sequence).

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Table 20-3. FTMRZ Memory Map

Global Address (in Bytes)	Description
0x0_0000 – 0x0_0FFF	Register Space
0x10_0000 – 0x1F_4000	EEPROM memory range. Allocation is device dependent.
0x1F_4000 – 0x1F_FFFF	NVM Resource Area(1) (see Figure 20-3)
0x80_0000 – 0xFD_FFFF	P-Flash memory range (Hardblock 0S). Allocation is device dependent.
0xFE_0000 – 0xFF_FFFF	P-Flash memory range (Hardblock 0N). Allocation is device dependent.

1. See NVM Resource area description in Section 20.4.4

20.3.1 Module Memory Map

The P-Flash memory is located between global addresses 0x80_0000 and 0xFF_FFFF. The P-Flash is high aligned from 0xFF_FFFF. Thus, for example, a 128 KB P-Flash extends from 0xFF_FFFF to 0xFE_0000.

The flash configuration field is mapped to the same addresses independent of the P-Flash memory size, as shown in Figure 20-2.

The FPROT register, described in Section 20.3.2.9, can be set to protect regions in the Flash memory from accidental program or erase. Three separate memory regions, one growing upward from global address 0xFF_8000 in the Flash memory (called the lower region), one growing downward from global address 0xFF_FFFF in the Flash memory (called the higher region), and the remaining addresses in the Flash memory, can be activated for protection. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information

Table 20-9. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 20-10.
5–2 RNV[5:2]	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 20-11. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 20-10. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED(1)
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

Table 20-11. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED(1)
10	UNSECURED
11	SECURED

1. Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 20.5.

20.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to indicate the amount of parameters loaded into the FCCOB registers for Flash memory operations.

Offset Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CCOBIX[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

21.4.2.3 Reserved Register

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 21-4. Reserved Register

1. Read: Anytime
   Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only and is not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

21.4.2.4 CAN Physical Layer Status Register (CPSR)

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CPCHVH	CPCHVL	CPCLVH	CPCLVL	CPDT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 21-5. CAN Physical Layer Status Register (CPSR)

1. Read: Anytime
   Write: Never

Table 21-6. CPSR Register Field Descriptions

Field	Description
7 CPCHVH	CANH Voltage Failure High Status Bit This bit reflects the CANH voltage failure high monitor status. 0 Condition $V_{CANH} < V_{H5}$ 1 Condition $V_{CANH} \geq V_{H5}$
6 CPCHVL	CANH Voltage Failure Low Status Bit This bit reflects the CANH voltage failure low monitor status. 0 Condition $V_{CANH} > V_{H0}$ 1 Condition $V_{CANH} \leq V_{H0}$
5 CPCLVH	CANL Voltage Failure High Status Bit This bit reflects the CANL voltage failure high monitor status. 0 Condition $V_{CANL} < V_{L5}$ 1 Condition $V_{CANL} \geq V_{L5}$

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

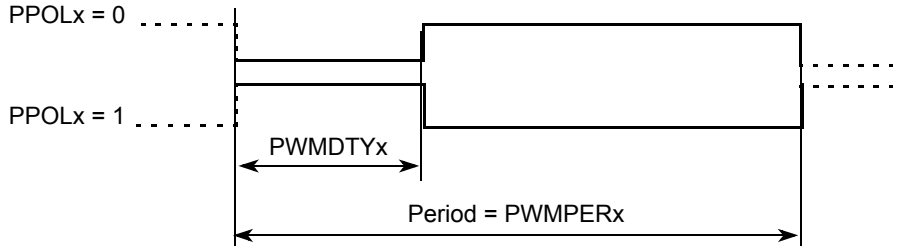

Figure 22-17. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)

    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)

    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = bus clock, where bus clock = 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/4 = 2.5 MHz

PWMx Period = 400 ns

PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 22-18.

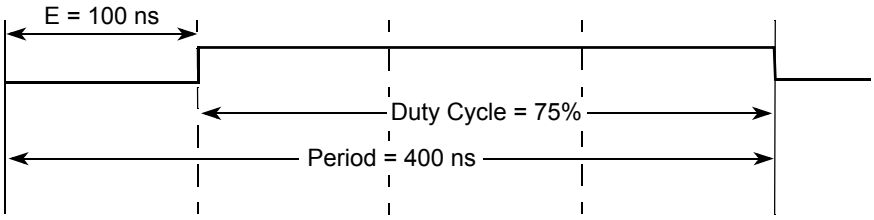

Figure 22-18. PWM Left Aligned Output Example Waveform