Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	40MHz
Connectivity	LINbus, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-LQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml31f1wkfr

Table 1-9. Pin Summary For 80-Pin Package Option (ZVMC256 Only) (Sheet 5 of 5)

Pin #	Pin Name	Function (Priority and routing options defined in PIM chapter)							Supply	Internal Pull Resistor	
		1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.		CTRL	Reset State
71	PS1	KWS1	TXD1	SCK0	PTUT1	CPDR0	TXCAN 0	IOC0_2	V_{DDX}	PERS/ PPSS	Up
72	PS0	KWS0	RXD1	$\overline{SS0}$	PTUT0	RXCAN 0	IOC0_1	—	V_{DDX}	PERS/ PPSS	Up
73	VDDF	—	—	—	—	—	—	—	V_{DDF}	—	—
74	VSS1	—	—	—	—	—	—	—	V_{DD}	—	—
75	VDD	—	—	—	—	—	—	—	V_{DD}	—	—
76	PP1	KWP1	PWM1_ 1	PWM0_ 1	IRQ	—	—	—	V_{DDX}	PPRP/ PPSP	Off
77	PP0/ EVDD1	KWP0	PWM1_ 5	ECLK	FAULT5	XIRQ	—	—	V_{DDX}	PPRP/ PPSP	Off
78	VDDX1	—	—	—	—	—	—	—	V_{DDX}	—	—
79	VSSX1	—	—	—	—	—	—	—	V_{DDX}	—	—
80	BKGD	MODC	—	—	—	—	—	—	V_{DDX}	—	Up

1.8 Internal Signal Mapping

This section specifies the mapping of inter-module signals at device level.

1.8.1 ADC Connectivity

1.8.1.1 ADC Reference Voltages

The ZVMC256 includes ADC12B_LBA V3 which features VRH_2, VRH_1, VRH_0 and VRL_0. On these devices for each ADC instance VRH_0 is mapped to VDDA, VRH_1 is mapped to VDDS1 and VRH_2 is mapped to VDDS2. VRL_0 is mapped to VSSA. Both VDDS1 and VDDS2 must be enabled by bits in the CPMUVREGCTL register before they can be used as references. When using VDDS1 or VDDS2 as VRH reference, the reference is impacted by a voltage drop across the internal short circuit protection switch. This is specified in Section C.1.1.5.

All other devices in the family include ADC12B_LBA V1, which features VRH_1, VRH_0, VRL_1 and VRL_0. On these devices, for both ADC instances, VRL_0 and VRL_1 are mapped to VSSA, whereby VRL_0 is the preferred reference for low noise. For both ADC instances VRH_1 is mapped to VDDA and VRH_0 is mapped to PAD8.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0284	DDRADH	R	DDRADH7[2]	DDRADH6[2]	DDRADH5[2]	DDRADH4[2]	DDRADH3[2]	DDRADH2[2]	DDRADL1[2]	DDRADH0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	PERADH	R	PERADH7[2]	PERADH6[2]	PERADH5[2]	PERADH4[2]	PERADH3[2]	PERADH2[2]	PERADH1[2]	PERADH0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	PPSADH	R	PPSADH7[2]	PPSADH6[2]	PPSADH5[2]	PPSADH4[2]	PPSADH3[2]	PPSADH2[2]	PPSADH1[2]	PPSADH0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								
0x028A–0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	PIEADH	R	PIEADH7[2]	PIEADH6[2]	PIEADH5[2]	PIEADH4[2]	PIEADH3[2]	PIEADH2[2]	PIEADH1[2]	PIEADH0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								
0x028E	PIFADH	R	PIFADH7[2]	PIFADH6[2]	PIFADH5[2]	PIFADH4[2]	PIFADH3[2]	PIFADH2[2]	PIFADH1[2]	PIFADH0
		W								
0x028F	PIFADL	R	PIFADL7	PIFADL6	PIFADL5	PIFADL4	PIFADL3	PIFADL2	PIFADL1	PIFADL0
		W								
0x0290–0x0297	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0298	DIENADH	R	DIENADH7[2]	DIENADH6[2]	DIENADH5[2]	DIENADH4[2]	DIENADH3[2]	DIENADH2[2]	DIENADH1[2]	DIENADH0
		W								
0x0299	DIENADL	R	DIENADL7	DIENADL6	DIENADL5	DIENADL4	DIENADL3	DIENADL2	DIENADL1	DIENADL0
		W								

at the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDC command, or the start of a SYNC request pulse.

5.5 Application Information

5.5.1 Clock Frequency Considerations

Read commands without status and without ACK must consider the frequency relationship between BDCSI and the internal core clock. If the core clock is slow, then the internal access may not have been carried out within the standard 16 BDCSI cycle delay period (DLY). The host must then extend the DLY period or clock frequencies accordingly. Taking internal clock domain synchronizers into account, the minimum number of BDCSI periods required for the DLY is expressed by:

$\#DLY > 3(f_{(BDCSI\ clock)} / f_{(core\ clock)}) + 4$

and the minimum core clock frequency with respect to BDCSI clock frequency is expressed by

Minimum $f_{(core\ clock)} = (3/(\#DLY\ cycles\ -4))f_{(BDCSI\ clock)}$

For the standard 16 period DLY this yields $f_{(core\ clock)} >= (1/4)f_{(BDCSI\ clock)}$

Table 6-41. DBGDAH, DBGDAM, DBGDAL Field Descriptions

Field	Description
15–0 DBGDA [15:0]	**Comparator Address Bits**[15:0]— These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.4 Functional Description

This section provides a complete functional description of the DBG module.

6.4.1 DBG Operation

The DBG module operation is enabled by setting ARM in DBGC1. When armed it supports storing of data in the trace buffer and can be used to generate breakpoints to the CPU. The DBG module is made up of comparators, control logic, the trace buffer, and the state sequencer, Figure 6-1.

The comparators monitor the bus activity of the CPU. Comparators can be configured to monitor opcode addresses (effectively the PC address) or data accesses. Comparators can be configured during data accesses to mask out individual data bus bits and to use R/W access qualification in the comparison. Comparators can be configured to monitor a range of addresses.

When configured for data access comparisons, the match is generated if the address (and optionally data) of a data access matches the comparator value.

Configured for monitoring opcode addresses, the match is generated when the associated opcode reaches the execution stage of the instruction queue, but before execution of that opcode.

When a match with a comparator register value occurs, the associated control logic can force the state sequencer to another state (see Figure 6-26).

The state sequencer can transition freely between the states 1, 2 and 3. On transition to Final State bus tracing can be triggered. On completion of tracing the state sequencer enters State0. If tracing is disabled or End aligned tracing is enabled then the state sequencer transitions immediately from Final State to State0. The transition to State0 generates breakpoints if breakpoints are enabled.

Independent of the comparators, state sequencer transitions can be forced by the external event input or by writing to the TRIG bit in the DBGC1 control register.

The trace buffer is visible through a 2-byte window in the register address map and can be read out using standard 16-bit word reads.

6.4.2 Comparator Modes

The DBG contains four comparators, A, B, C, and D. Each comparator compares the address stored in DBGXAH, DBGXAM, and DBGXAL with the PC (opcode addresses) or selected address bus (data

8.1.4 S12CPMU_UHV_V10_V6 Block Diagram

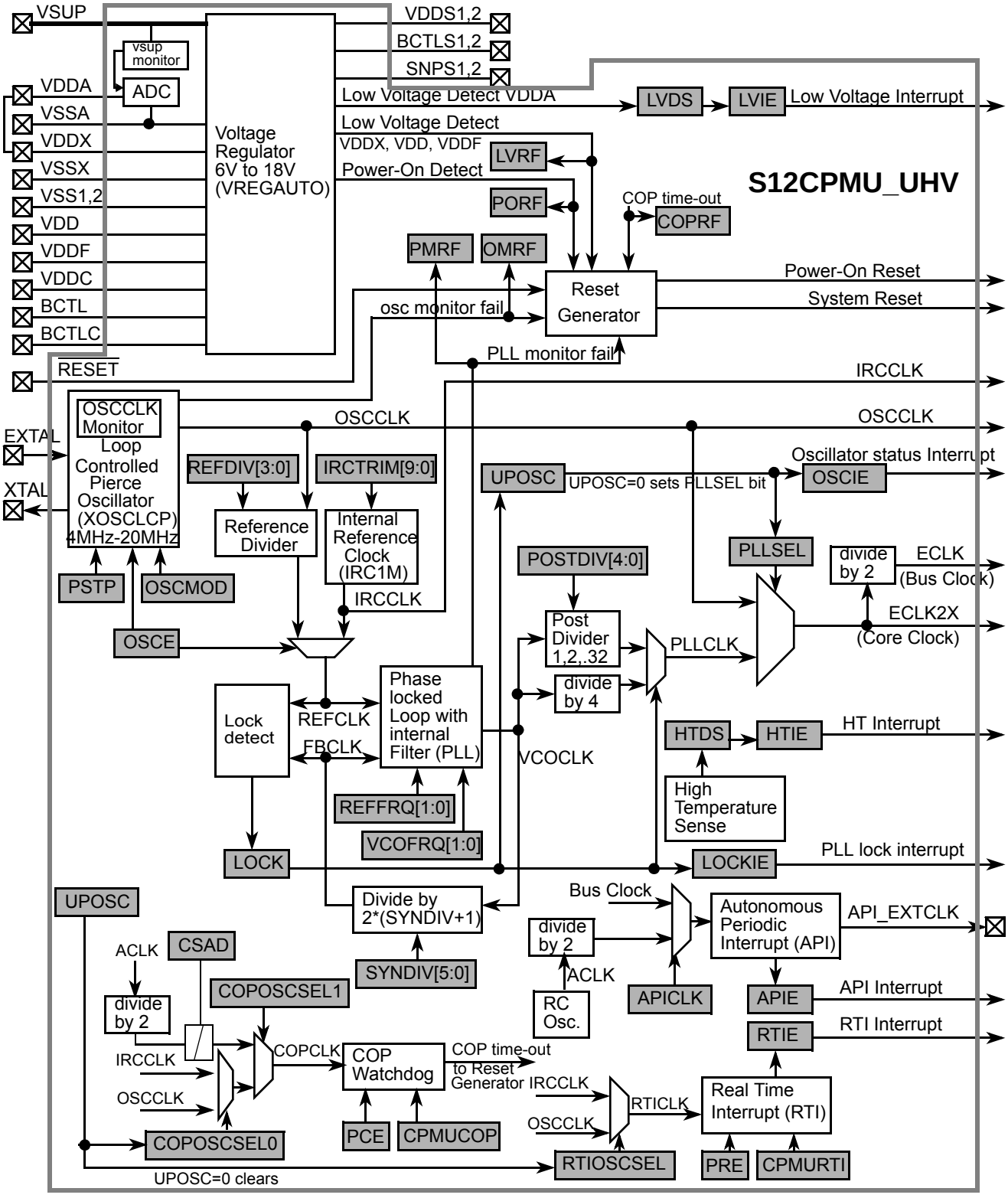


Figure 8-1. Block diagram of S12CPMU_UHV_V10_V6

8.3.2.6 S12CPMU_UHV_V10_V6 Post Divider Register (CPMUPOSTDIV)

The POSTDIV register controls the frequency ratio between the VCOCLK and the PLLCLK.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	0	0	0	POSTDIV[4:0]				
W								
Reset	0	0	0	0	0	0	1	1

= Unimplemented or Reserved

Figure 8-11. S12CPMU_UHV_V10_V6 Post Divider Register (CPMUPOSTDIV)

Read: Anytime

Write: If PLLSEL=1 write anytime, else write has no effect

If PLL is locked (LOCK=1) $f_{PLL} = \frac{f_{VCO}}{(POSTDIV + 1)}$

If PLL is not locked (LOCK=0) $f_{PLL} = \frac{f_{VCO}}{4}$

If PLL is selected (PLLSEL=1) $f_{bus} = \frac{f_{PLL}}{2}$

When changing the POSTDIV[4:0] value or PLL transitions to locked stated (lock=1), it takes up to 32 Bus Clock cycles until f_{PLL} is at the desired target frequency. This is because the post divider gradually changes (increases or decreases) f_{PLL} in order to avoid sudden load changes for the on-chip voltage regulator.

8.3.2.7 S12CPMU_UHV_V10_V6 Interrupt Flags Register (CPMUIFLG)

This register provides S12CPMU_UHV_V10_V6 status bits and interrupt flags.

8.6 Interrupts

The interrupt vectors requested by the S12CPMU_UHV_V10_V6 are listed in Table 8-37. Refer to MCU specification for related vector addresses and priorities.

Table 8-37. S12CPMU_UHV_V10_V6 Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
RTI time-out interrupt	I bit	CPMUINT (RTIE)
PLL lock interrupt	I bit	CPMUINT (LOCKIE)
Oscillator status interrupt	I bit	CPMUINT (OSCIE)
Low voltage interrupt	I bit	CPMULVCTL (LVIE)
VDDS integrity interrupt(1)	I bit	CPMULVCTL (VDDSIE)
High temperature interrupt	I bit	CPMUHTCTL (HTIE)
Autonomous Periodical Interrupt	I bit	CPMUAPICTL (APIE)

1. Only available in V10

8.6.1 Description of Interrupt Operation

8.6.1.1 Real Time Interrupt (RTI)

The clock source for the RTI is either IRCCLK or OSCCLK depending on the setting of the RTIOSCSEL bit. In Stop Mode with PSTP=1 (Pseudo Stop Mode), RTIOSCSEL=1 and PRE=1 the RTI continues to run, else the RTI counter halts in Stop Mode.

The RTI can be used to generate hardware interrupts at a fixed periodic rate. If enabled (by setting RTIE=1), this interrupt will occur at the rate selected by the CPMURTI register. At the end of the RTI time-out period the RTIF flag is set to one and a new RTI time-out period starts immediately.

A write to the CPMURTI register restarts the RTI time-out period.

8.6.1.2 PLL Lock Interrupt

The S12CPMU_UHV_V10_V6 generates a PLL Lock interrupt when the lock condition (LOCK status bit) of the PLL changes, either from a locked state to an unlocked state or vice versa. Lock interrupts are locally disabled by setting the LOCKIE bit to zero. The PLL Lock interrupt flag (LOCKIF) is set to1 when the lock condition has changed, and is cleared to 0 by writing a 1 to the LOCKIF bit.

8.6.1.3 Oscillator Status Interrupt

When the OSCE bit is 0, then UPOSC stays 0. When OSCE=1 the UPOSC bit is set after the LOCK bit is set.

9.9.7 Conversion flow control application information

The ADC12B_LBA provides various conversion control scenarios to the user accomplished by the following features.

The ADC conversion flow control can be realized via the data bus only, the internal interface only, or by both access methods. The method used is software configurable via bits ACC_CFG[1:0].

The conversion flow is controlled via the four conversion flow control bits: SEQA, TRIG, RSTA, and LDOK.

Two different conversion flow control modes can be configured: Trigger Mode or Restart Mode

Single or double buffer configuration of CSL and RVL.

9.9.7.1 Initial Start of a Command Sequence List

At the initial start of a Command Sequence List after device reset all entries for at least one of the two CSL must have been completed and data must be valid. Depending on if the CSL_0 or the CSL_1 should be executed at the initial start of a Command Sequence List the following conversion control sequence must be applied:

If CSL_0 should be executed at the initial conversion start after device reset:
A Restart Event and a Trigger Event must occur (depending to the selected conversion flow control mode the events must occur one after the other or simultaneously) which causes the ADC to start conversion with commands loaded from CSL_0.

If CSL_1 should be executed at the initial conversion start after device reset:
Bit LDOK must be set simultaneously with the Restart Event followed by a Trigger Event (depending on the selected conversion flow control mode the Trigger events must occur simultaneously or after the Restart Event is finished). As soon as the Trigger Event gets executed the ADC starts conversion with commands loaded from CSL_1.

As soon as a new valid Restart Event occurs the flow for ADC register load at conversion sequence start as described in Section 9.6.3.3, “ADC List Usage and Conversion/Conversion Sequence Flow Description applies.

9.9.7.2 Restart CSL execution with currently active CSL

To restart a Command Sequence List execution it is mandatory that the ADC is idle (no conversion or conversion sequence is ongoing).

If necessary, a possible ongoing conversion sequence can be aborted by the Sequence Abort Event (setting bit SEQA). As soon as bit SEQA is cleared by the ADC, the current conversion sequence has been aborted and the ADC is idle (no conversion sequence or conversion ongoing).

After a conversion sequence abort is executed it is mandatory to request a Restart Event (bit RSTA set). After the Restart Event is finished (bit RSTA is cleared), the ADC accepts a new Trigger Event (bit TRIG can be set) and begins conversion from the top of the currently active CSL. In conversion flow control

The comparator outputs BVLC and BVHC are forced to zero if the comparator is disabled (configuration bit BSUSE is cleared). If the software disables the comparator during a high or low Voltage condition (BVHC or BVLC active), then an additional interrupt is generated. To avoid this behavior the software must disable the interrupt generation before disabling the comparator.

The BATS interrupt vector is named in Table 10-6. Vector addresses and interrupt priorities are defined at MCU level.

The module internal interrupt sources are combined into one module interrupt signal.

Table 10-6. BATS Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
BATS Interrupt (BATI)	BATS Voltage Low Condition Interrupt (BVLI)	BVLIE = 1
	BATS Voltage High Condition Interrupt (BVHI)	BVHIE = 1

10.4.2.1 BATS Voltage Low Condition Interrupt (BVLI)

To use the Voltage Low Interrupt the Level Sensing must be enabled (BSUSE =1).

If measured when

a) V_{LBI1} selected with BVLS[1:0] = 0x0
$V_{measure} < V_{LBI1\_A}$ (falling edge) or $V_{measure} < V_{LBI1\_D}$ (rising edge)

or when

b) V_{LBI2} selected with BVLS[1:0] = 0x1 at pin VSUP
$V_{measure} < V_{LBI2\_A}$ (falling edge) or $V_{measure} < V_{LBI2\_D}$ (rising edge)

or when

c) V_{LBI3} selected with BVLS[1:0] = 0x2
$V_{measure} < V_{LBI3\_A}$ (falling edge) or $V_{measure} < V_{LBI3\_D}$ (rising edge)

or when

d) V_{LBI4} selected with BVLS[1:0] = 0x3
$V_{measure} < V_{LBI4\_A}$ (falling edge) or $V_{measure} < V_{LBI4\_D}$ (rising edge)

then BVLC is set. BVLC status bit indicates that a low voltage at pin VSUP is present. The Low Voltage Interrupt flag (BVLIF) is set to 1 when the Voltage Low Condition (BVLC) changes state . The Interrupt flag BVLIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVLIE the module requests an interrupt to MCU (BATI).

10.4.2.2 BATS Voltage High Condition Interrupt (BVHI)

To use the Voltage High Interrupt the Level Sensing must be enabled (BSUSE=1).

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000C	PMFOUTC	R	0	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0
		W								
0x000D	PMFOUTB	R	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
		W								
0x000E	PMFDTMS	R	0	0	DT5	DT4	DT3	DT2	DT1	DT0
		W								
0x000F	PMFCCTL	R	0	0	ISENS		0	IPOLC	IPOLB	IPOLA
		W								
0x0010	PMFVAL0	R	PMFVAL0							
		W								
0x0011	PMFVAL0	R	PMFVAL0							
		W								
0x0012	PMFVAL1	R	PMFVAL1							
		W								
0x0013	PMFVAL1	R	PMFVAL1							
		W								
0x0014	PMFVAL2	R	PMFVAL2							
		W								
0x0015	PMFVAL2	R	PMFVAL2							
		W								
0x0016	PMFVAL3	R	PMFVAL3							
		W								
0x0017	PMFVAL3	R	PMFVAL3							
		W								
0x0018	PMFVAL4	R	PMFVAL4							
		W								
0x0019	PMFVAL4	R	PMFVAL4							
		W								
0x001A	PMFVAL5	R	PMFVAL5							
		W								

= Unimplemented or Reserved

Figure 15-2. Quick Reference to PMF Registers (Sheet 2 of 5)

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001B	PMFVAL5	R W	PMFVAL5							
0x001C	PMFROIE	R	0	0	0	0	0	PMFROIEC	PMFROIEB	PMFROIEA
		W								
0x001D	PMFROIF	R	0	0	0	0	0	PMFROIFC	PMFROIFB	PMFROIFA
		W								
0x001E	PMFICCTL	R	0	0	PECC	PECB	PECA	ICCC	ICCB	ICCA
		W								
0x001F	PMFCINV	R	0	0	CINV5	CINV4	CINV3	CINV2	CINV1	CINV0
		W								
0x0020	PMFENCA	R	PWMENA	GLDOKA	0	0	0	RSTRTA	LDOKA	PWMRIEA
		W								
0x0021	PMFFQCA	R W	LDFQA				HALFA	PRSCA		PWMRFA
0x0022	PMFCNTA	R	0	PMFCNTA						
		W								
0x0023	PMFCNTA	R W	PMFCNTA							
0x0024	PMFMODA	R	0	PMFMODA						
		W								
0x0025	PMFMODA	R W	PMFMODA							
0x0026	PMFDTMA	R	0	0	0	0	PMFDTMA			
		W								
0x0027	PMFDTMA	R W	PMFDTMA							
0x0028	PMFENCB	R	PWMENB	GLDOKB	0	0	0	RSTRTB	LDOKB	PWMRIEB
		W								
0x0029	PMFFQCB	R W	LDFQB				HALFB	PRSCB		PWMRFB

= Unimplemented or Reserved

Figure 15-2. Quick Reference to PMF Registers (Sheet 3 of 5)

the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. Mode fault error doesn't occur in slave mode.

If a mode fault error occurs, the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So SCK, MISO, and MOSI pins are forced to be high impedance inputs to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for a SPI system configured in master mode, output enable of the MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to SPI control register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

NOTE

If a mode fault error occurs and a received data byte is pending in the receive shift register, this data byte will be lost.

17.4.7 Low Power Mode Options

17.4.7.1 SPI in Run Mode

In run mode with the SPI system enable (SPE) bit in the SPI control register clear, the SPI system is in a low-power, disabled state. SPI registers remain accessible, but clocks to the core of this module are disabled.

17.4.7.2 SPI in Wait Mode

SPI operation in wait mode depends upon the state of the SPISWAI bit in SPI control register 2.

- If SPISWAI is clear, the SPI operates normally when the CPU is in wait mode
- If SPISWAI is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
  - If SPISWAI is set and the SPI is configured for master, any transmission and reception in progress stops at wait mode entry. The transmission and reception resumes when the SPI exits wait mode.
  - If SPISWAI is set and the SPI is configured as a slave, any transmission and reception in progress continues if the SCK continues to be driven from the master. This keeps the slave synchronized to the master and the SCK.

    If the master transmits several bytes while the slave is in wait mode, the slave will continue to send out bytes consistent with the operation mode at the start of wait mode (i.e., if the slave is currently sending its SPIDR to the master, it will continue to send the same byte. Else if the slave is currently sending the last received byte from the master, it will continue to send each previous master byte).

18.3.2.17 GDU Control Register 1 (GDUCTR1)

Module Base + 0x0010 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	GSRMOD1	GSRMOD0	0	0	0	0	0	TDEL
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-19. GDU Control Register 1 (GDUCTR1)

1. Read: Anytime
   Write: Only if GWP=0

Table 18-21. GDUCTR1 Register Field Descriptions

Field	Description
7 GSRMOD1	GDU Switched Reluctance Motor Mode 1 — This bit cannot be modified after GWP bit is set. This bit controls the routing of the LDx pins to the low-side desaturation comparators for switched reluctance motor. See Figure 18-23 0 HSx routed to low-side desaturation comparator 1 LDx routed to low-side desaturation comparator
6 GSRMOD0	GDU Switched Reluctance Motor Mode 0 — This bit cannot be modified after GWP bit is set. 0 BLDC mode. Don't allow HGx and LGx high at the same time. 1 SR mode. Allow HGx and LGx high at the same time.
0 TDEL	**t_{delon} / t_{deloff} Control** — This bit controls the parameters t_{delon} and t_{deloff}. It cannot be modified after GWP bit is set. This bit must be set to meet the min and max values for t_{delon} and t_{deloff} specified in the electrical specification. If this bit is cleared the values for t_{delon} and t_{deloff} are out of spec.

NOTE

GDU Control Register 1 GDUCTR1 availability is defined at device level.

Table 20-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x1F_C000 – 0x1F_C007	8	Reserved
0x1F_C008 – 0x1F_C0B5	174	Reserved
0x1F_C0B6 – 0x1F_C0B7	2	Version ID[1]
0x1F_C0B8 – 0x1F_C0BF	8	Reserved
0x1F_C0C0 – 0x1F_C0FF	64	Program Once Field Refer to Section 20.4.7.6, “Program Once Command”

1. Used to track firmware patch versions, see Section 20.4.2

Table 20-6. Memory Controller Resource Fields (NVM Resource Area[1])

Global Address	Size (Bytes)	Description
0x1F_4000 – 0x1F_41FF	512	Reserved
0x1F_4200 – 0x1F_7FFF	15,872	Reserved
0x1F_8000 – 0x1F_97FF	6,144	Reserved
0x1F_9800 – 0x1F_BFFF	10,240	Reserved
0x1F_C000 – 0x1F_C0FF	256	P-Flash IFR (see Table 20-5)
0x1F_C100 – 0x1F_C1FF	256	Reserved.
0x1F_C200 – 0x1F_FFFF	15,872	Reserved.

1. See Section 20.4.4 for NVM Resources Area description.

Table 20-46. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 20-29)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.7.1 Erase All Pin

The functionality of the Erase All Blocks command is also available in an uncommanded fashion from the *soc_erase_all_req* input pin on the Flash module. Refer to the Reference Manual for information on control of *soc_erase_all_req*.

The erase-all function requires the clock divider register FCLKDIV (see Section 20.3.2.1) to be loaded before invoking this function using *soc_erase_all_req* input pin. The FCLKDIV configuration for this feature is described at device level. If FCLKDIV is not properly set the erase-all operation will not execute and the ACCERR flag in FSTAT register will set. After the execution of the erase-all function the FCLKDIV register will be reset and the value of register FCLKDIV must be loaded before launching any other command afterwards.

Before invoking the erase-all function using the *soc_erase_all_req* pin, the ACCERR and FPVIOL flags in the FSTAT register must be clear. When invoked from *soc_erase_all_req* the erase-all function will erase all P-Flash memory and EEPROM memory space regardless of the protection settings. If the post-erase verify passes, the routine will then release security by setting the SEC field of the FSEC register to the unsecure state (see Section 20.3.2.2). The security byte in the Flash Configuration Field will be programmed to the unsecure state (see Table 20-9). The status of the erase-all request is reflected in the ERSAREQ bit in the FCNFG register (see Section 20.3.2.5). The ERSAREQ bit in FCNFG will be cleared once the operation has completed and the normal FSTAT error reporting will be available as described inTable 20-47.

At the end of the erase-all sequence Protection will remain configured as it was before executing the erase-all function. If the application requires programming P-Flash and/or EEPROM after the erase-all function completes, the existing protection limits must be taken into account. If protection needs to be disabled the user may need to reset the system right after completing the erase-all function.

Table 20-47. Erase All Pin Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if command not available in current mode (see Table 20-29)
	MGSTAT1	Set if any errors have been encountered during the erase verify operation, or during the program verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the erase verify operation, or during the program verify operation

21.4.2.5 Reserved Register

Module Base + 0x0004 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 21-6. Reserved Register

1. Read: Anytime
   Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only and is not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

21.4.2.6 Reserved Register

Module Base + 0x0005 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 21-7. Reserved Register

1. Read: Anytime
   Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only and is not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

21.4.2.7 CAN Physical Layer Interrupt Enable Register (CPIE)

Module Base + 0x0006 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	CPVFIE	CPDTIE	0	0	CPOCIE
W								
Reset	0	0	0	0	0	0	0	0

Figure 21-8. CAN Physical Layer Interrupt Enable Register (CPIE)

1. Read: Anytime
   Write: Anytime

Table F-1. FTMRZ128K512 NVM Timing Characteristics (Junction Temperature From –40°C To +150°C)

Derivatives ZVML128, ZVMC128, ZVML64, ZVMC64, ZVML32									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	50	50	50	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	33760	t_{RD1ALL}	0.68	0.68	1.35	67.52	ms
4	Erase Verify Block (Pflash)	0	33320	t_{RD1BLK_P}	0.67	0.67	1.33	66.64	ms
5	Erase Verify Block (EEPROM)	0	823	t_{RD1BLK_D}	0.02	0.02	0.03	1.65	ms
6	Erase Verify P-Flash Section	0	505	t_{RD1SEC}	0.01	0.01	0.04	2.02	ms
7	Read Once	0	481	t_{RDONCE}	9.62	9.62	9.62	481.00	us
8	Program P-Flash (4 Word)	164	3077	t_{PGM_4}	0.22	0.23	0.41	12.51	ms
9	Program Once	164	3054	$t_{PGMONCE}$	0.22	0.23	0.23	3.26	ms
10	Erase All Blocks	100066	34223	t_{ERSALL}	95.99	100.75	101.43	193.53	ms
11	Erase Flash Block (Pflash)	100060	33681	t_{ERSBLK_P}	95.97	100.73	101.41	192.44	ms
12	Erase Flash Block (EEPROM)	100060	1154	t_{ERSBLK_D}	95.32	100.08	100.11	127.38	ms
13	Erase P-Flash Sector	20015	914	t_{ERSPG}	19.08	20.03	20.05	26.85	ms
14	Unsecure Flash	100066	34288	t_{UNSECU}	95.99	100.75	101.44	193.66	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	9.86	9.86	9.86	493.00	us
16	Set User Margin Level	0	427	t_{MLOADU}	8.54	8.54	8.54	427.00	us
17	Set Factory Margin Level	0	436	t_{MLOADF}	8.72	8.72	8.72	436.00	us
18	Erase Verify EEPROM Sector	0	583	$t_{DRD1SEC}$	0.01	0.01	0.05	2.33	ms
19	Program EEPROM (1 Word)	68	1657	t_{DPGM_1}	0.10	0.10	0.20	6.71	ms
20	Program EEPROM (2 Word)	136	2660	t_{DPGM_2}	0.18	0.19	0.35	10.81	ms
21	Program EEPROM (3 Word)	204	3663	t_{DPGM_3}	0.27	0.28	0.50	14.91	ms
22	Program EEPROM (4 Word)	272	4666	t_{DPGM_4}	0.35	0.37	0.65	19.00	ms
23	Erase EEPROM Sector	5015	810	t_{DERSPG}	4.79	5.03	20.34	38.85	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	9.50	9.50	9.50	475.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

Appendix I
SPI Electrical Specifications

This section provides electrical parametrics and ratings for the SPI.

In **Figure I-1.** the measurement conditions are listed.

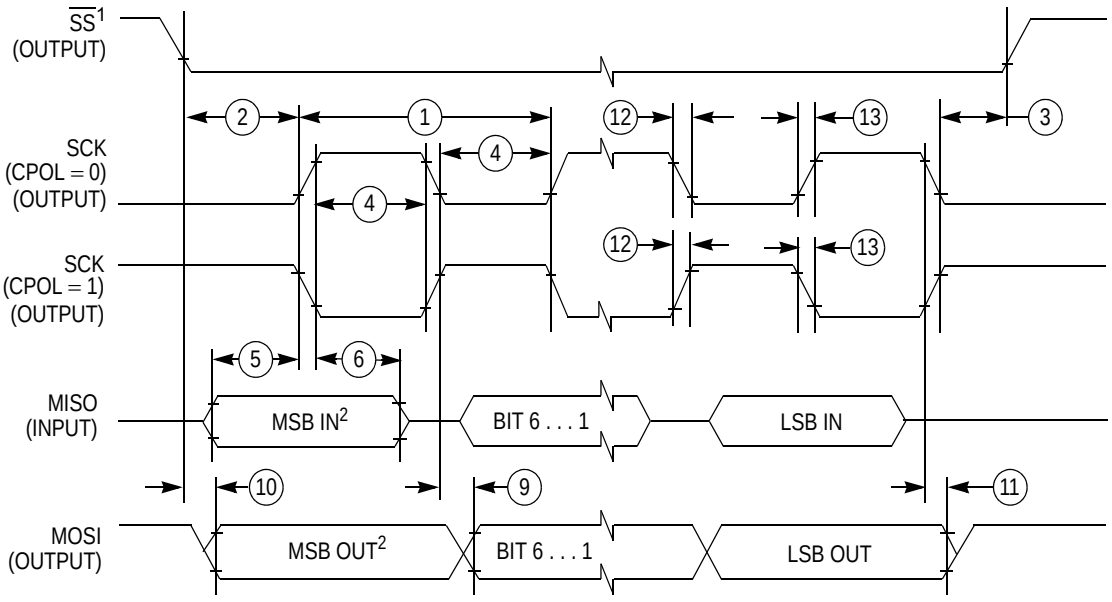
Figure I-1. Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}[(1)], on all outputs	50	pF
Thresholds for delay measurement points	(35% / 65%) VDDX	V

1. Timing specified for equal load on all SPI output pins. Avoid asymmetric load.

I.1 Master Mode

In **Figure I-2.** the timing diagram for master mode with transmission format CPHA=0 is depicted.



1. If enabled.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure I-2. SPI Master Timing (CPHA=0)

In **Figure I-3.** the timing diagram for master mode with transmission format CPHA=1 is depicted.

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x013C	DBGCDM0 (2)	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x013D	DBGCDM1 2	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013E	DBGCDM2 2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013F	DBGCDM3 2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								
0x0147	DBGDAL	R	DBGDA[7:0]							
		W								
0x0148-0x017F	Reserved	R	0	0	0	0	0	0	0	0
		W								

1. Only included on S12ZVM256

2. Not included on S12ZVM32 or S12ZVM16 devices