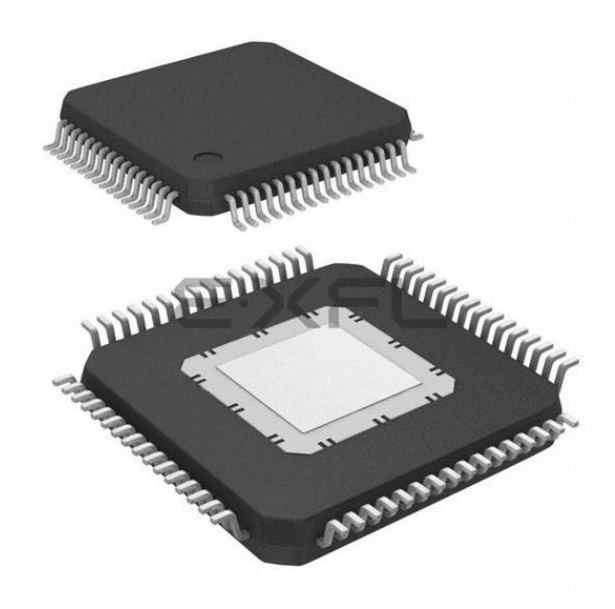

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	40MHz
Connectivity	LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml31f1wkh

The device supports the use of an external PNP to supplement the VDDX supply, for reducing on chip power dissipation. In this configuration, most of the current flowing from VRBATP to VDDX, flows through the external PNP, using the BCTL pin for PNP base current control. The configuration can be selected by register bits EXTXON and INTXON.

The maximum current that can be sourced by the voltage regulator without the external PNP is specified as IDDX, for different VSUP ranges, in the electrical parameter appendices. Depending on activity and external loading, an application current may exceed this specification limit. In such cases the external PNP configuration must be used.

A supply for the internal CANPHY is offered via device pins BCTLC and VDDC, whereby BCTLC provides the base current of an external PNP and VDDC is the CANPHY supply (output voltage of the external PNP). This configuration can be enabled by the register bit EXTCON.

Two separate 5V range supplies (VDDS1 and VDDS2) are provided for external (sensor) components. These supplies also use external PNP configurations, whereby the PNP base current is controlled by BCTLS1 and BCTLS2 for VDDS1 and VDDS2 respectively.

The VDDS1 and VDDS2 supplies feature sense inputs SNPS1 and SNPS2, to detect a short circuit or over current condition and subsequently limit the current to avoid damage.

For each ADC instantiation, the ADC register bit VRH_SEL maps the ADC reference VRH to VDDA or to a VDDS of a tracker regulator. The Figure 1-19 example only shows one ADC to VDDS connection.

1.13.8.1 Voltage Domain Monitoring

The BATS module monitors the voltage on the VSUP pin, providing status and flag bits, an interrupt and a connection to the ADC, for accurate measurement of the scaled VSUP level.

The POR circuit monitors the VDD and VDDA domains, ensuring a reset assertion until an adequate voltage level is attained. The LVR circuit monitors the VDD, VDDF and VDDX domains, generating a reset when the voltage in any of these domains drops below the specified assert level. The VDDX LVR monitor is disabled when the VREG is in reduced power mode. A low voltage interrupt circuit monitors the VDDA domain.

The GDU high side drain voltage, pin HD, is monitored within the GDU and mapped to an interrupt. A connection to the ADC is provided for accurate measurement of a scaled HD level.

1.13.8.2 FET-Predriver (GDU) Supplies

A dedicated low drop regulator is used to generate the VLS_OUT voltage from VSUP. The VLS_OUT voltage is used to supply the low side drivers and can be directly connected to the VLS inputs of each low side driver. For FET-predriver operation at lower VSUP levels, a boost circuit can be enabled by the GBOE register bit. The boost circuit requires Shottky diodes, a coil and capacitors, as shown in Figure 1-18. More detailed information is included in the GDU module description.

1.13.8.2.1 Bootstrap Precharge

The FET-predriver high side driver must provide a sufficient gate-source voltage and sufficient charge for the gate capacitance of the external FETs. A bootstrap circuit is used to provide sufficient charge, whereby

Port	Pin Name	ZVMC256	ZVMC128\64	ZVML128/64/32	ZVML31	ZVM32/16	Pin Function & Priority[1]	I/O	Description	Routing Register Bit	Pin Function after Reset
	PS0	✔					$\overline{SS0}$	I/O	SPI0 slave select	SPI0RR SPI0SSRR	
		✔	✔	✔	✔	✔	PTUT0	O	PTU trigger 0	—	
		✔			✔	✔	(IOC0_1)	I/O	TIM0 channel 1	T0C1RR T0IC1RR T0IC1RR0	
				✔	✔	✔	(LPRXD0)	O	LINPHY0/HVPHY0 receive output	S0L0RR2-0	
		✔	✔	✔			RXCAN0[2]	I	MSCAN0 receive	M0C0RR2-0	
		✔	✔	✔	✔	✔	RXD1	I	SCI1 receive	SCI1RR	
		✔	✔	✔	✔	✔	PTS[0]/ KWS[0]	I/O	General-purpose; with interrupt and wakeup	—	

1. Signals in parentheses denote alternative module routing pins.
2. Routing option for ZVMC256

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x00001D	INT_CFDATA5	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001E	INT_CFDATA6	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001F	INT_CFDATA7	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

= Unimplemented or Reserved

Figure 4-2. INT Register Summary

4.3.2.1 Interrupt Vector Base Register (IVBR)

Address: 0x000010

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	IVB_ADDR[15:1]															0
W																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Figure 4-3. Interrupt Vector Base Register (IVBR)

Read: Anytime

Write: Anytime

Table 4-4. IVBR Field Descriptions

Field	Description
15–1 IVB_ADDR [15:1]	**Interrupt Vector Base Address Bits** — These bits represent the upper 15 bits of all vector addresses. Out of reset these bits are set to 0xFFFE (i.e., vectors are located at 0xFFFE00–0xFFFFFF). **Note:** A system reset will initialize the interrupt vector base register with “0xFFFE” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the reset vector (0xFFFFFC–0xFFFFFF).

4.3.2.2 Interrupt Request Configuration Address Register (INT_CFADDR)

Address: 0x000017

	7	6	5	4	3	2	1	0
R	0	INT_CFADDR[6:3]				0	0	0
W								
Reset	0	0	0	0	1	0	0	0

= Unimplemented or Reserved

Figure 4-4. Interrupt Configuration Address Register (INT_CFADDR)

Read: Anytime

Table 6-17. DBGSCR1 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State1 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State1 following a match1.
5–4 C2SC[1:0]	Channel 2 State Control. These bits select the targeted next state whilst in State1 following a match2.
7–6 C3SC[1:0]	Channel 3 State Control. If EEVE !=10, these bits select the targeted next state whilst in State1 following a match3. If EEVE = 10, these bits select the targeted next state whilst in State1 following an external event.

Table 6-18. State1 Match State Sequencer Transitions

CxSC[1:0]	Function
00	Match has no effect
01	Match forces sequencer to State2
10	Match forces sequencer to State3
11	Match forces sequencer to Final State

In the case of simultaneous matches, the match on the higher channel number (3...0) has priority.

6.3.2.8 Debug State Control Register 2 (DBGSCR2)

Address: 0x0108

	7	6	5	4	3	2	1	0
R W	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
Reset	0	0	0	0	0	0	0	0

Figure 6-10. Debug State Control Register 2 (DBGSCR2)

Read: Anytime.

Write: If DBG is not armed and PTACT is clear.

The state control register 2 selects the targeted next state whilst in State2. The matches refer to the outputs of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.12”. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-19. DBGSCR2 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State2 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State2 following a match1.

Table 6-25. SSF[2:0] — State Sequence Flag Bit Encoding

SSF[2:0]	Current State
100	Final State
101,110,111	Reserved

6.3.2.12 Debug Comparator A Control Register (DBGACTL)

Address: 0x0110

	7	6	5	4	3	2	1	0
R	0	NDB	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-14. Debug Comparator A Control Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-26. DBGACTL Field Descriptions

Field	Description
6 NDB	**Not Data Bus** — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. This bit is ignored if the INST bit in the same register is set. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored when INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 6-27 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

6.3.2.20 Debug Comparator C Data Register (DBGCD)

Address: 0x0138, 0x0139, 0x013A, 0x013B

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-22. Debug Comparator C Data Register (DBGCD)

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

This register can be accessed with a byte resolution, whereby DBGCD0, DBGCD1, DBGCD2, DBGCD3 map to DBGCD[31:0] respectively.

XGATE data accesses have a maximum width of 16-bits and are mapped to DBGCD[15:0].

Table 6-37. DBGCD Field Descriptions

Field	Description
31–16 Bits[31:16] (DBGCD0, DBGCD1)	**Comparator Data Bits** — These bits control whether the comparator compares the data bus bits to a logic one or logic zero. The comparator data bits are only used in comparison if the corresponding data mask bit is logic 1. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one
15–0 Bits[15:0] (DBGCD2, DBGCD3)	**Comparator Data Bits** — These bits control whether the comparator compares the data bus bits to a logic one or logic zero. The comparator data bits are only used in comparison if the corresponding data mask bit is logic 1. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

6.3.2.21 Debug Comparator C Data Mask Register (DBGCDM)

Address: 0x013C, 0x013D, 0x013E, 0x013F

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-23. Debug Comparator C Data Mask Register (DBGCDM)

Read: Anytime.

Table 8-33. CPMUVDDS Field Descriptions (continued)

Field	Description
3 SCS2IF	**Short circuit VDDS2 Interrupt Flag** — SCS2IF is set to 1 when SCS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS2IF causes an interrupt request. 0 No change in SCS2 bit. 1 SCS2 bit has changed.
2 SCS1IF	**Short circuit VDDS1 Interrupt Flag** — SCS1IF is set to 1 when SCS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS1IF causes an interrupt request. 0 No change in SCS1 bit. 1 SCS1 bit has changed.
1 LVS2IF	**Low-Voltage VDDS2 Interrupt Flag** — LVS2IF is set to 1 when LVDS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS2IF causes an interrupt request. 0 No change in LVDS2 bit. 1 LVDS2 bit has changed.
0 LVS1IF	**Low-Voltage VDDS1 Interrupt Flag** — LVS1IF is set to 1 when LVDS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS1IF causes an interrupt request. 0 No change in LVDS1 bit. 1 LVDS1 bit has changed.

14.2.3 PTURE — PTUE Reload Event

If enabled (PTUREPE is set) this pin shows the internal reload event.

14.3 Memory Map and Register Definition

This section provides the detailed information of all registers for the PTU module.

14.3.1 Register Summary

Figure 14-2 shows the summary of all implemented registers inside the PTU module.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PTUE	R	0	PTUFRZ	0	0	0	0	TG1EN	TG0EN
	W								
0x0001 PTUC	R	0	0	0	0	0	0	0	PTULDOK
	W								
0x0002 PTUIEH	R	0	0	0	0	0	0	0	PTUROIE
	W								
0x0003 PTUIEL	R	TG1AEIE	TG1REIE	TG1TEIE	TG1DIE	TG0AEIE	TG0REIE	TG0TEIE	TG0DIE
	W								
0x0004 PTUIFH	R	0	0	0	0	0	0	PTUDEEF	PTUROIF
	W								
0x0005 PTUIFL	R	TG1AEIF	TG1REIF	TG1TEIF	TG1DIF	TG0AEIF	TG0REIF	TG0TEIF	TG0DIF
	W								
0x0006 TG0LIST	R	0	0	0	0	0	0	0	TG0LIST
	W								
0x0007 TG0TNUM	R	0	0	0	TG0TNUM[4:0]				
	W								
0x0008 TG0TVH	R	TG0TV[15:8]							
	W								

= Unimplemented

Figure 14-2. PTU Register Summary

Table 14-12. TG1LIST Register Field Descriptions

Field	Description
0 TG1LIST	Trigger Generator 1 List — This bit shows the number of the current used list. 0 Trigger generator 1 is using list 0 1 Trigger generator 1 is using list 1

Table 14-14. TG1TV Register Field Descriptions

Field	Description
TG1TV[15:0]	Trigger Generator 1 Next Trigger Value — This register contains the currently used trigger value to generate the next trigger. If the time base counter reach this value the next trigger event is generated. If the trigger generator reached the end of list (EOL) symbol then this value is visible inside this register. If the last generated trigger was trigger number 32 then the last used trigger value is visible inside this register. See also Figure 14-22.

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set.

Address: Module Base + 0x0009 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	QSMP3		QSMP2		QSMP1		QSMP0	
Reset	0	0	0	0	0	0	0	0

Figure 15-12. PMF Fault Qualifying Samples Register (PMFQSMP1)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set.

Table 15-14. PMFQSMP0-1 Field Descriptions

Field	Description
7–0 QSMP*m*[1:0]	**Fault *m* Qualifying Samples** — This field indicates the number of consecutive samples taken at the FAULT*m* input to determine if a fault is detected. The first sample is qualified after two bus cycles from the time the fault is present and each sample after that is taken every four core clock cycles. See Table 15-15. This register cannot be modified after the WP bit is set. *m* is 0, 1, 2, 3, 4 and 5.

Table 15-15. Qualifying Samples

QSMP*m*[1:0]	Number of Samples
00	1 sample(1)
01	5 samples
10	10 samples
11	15 samples

1. There is an asynchronous path from fault inputs FAULT3-0, FAULT4 if DMP*n*4=b10, and FAULT5 if DMP*n*5=b10 to disable PWMs immediately but the fault is qualified in two bus cycles.

15.3.2.10 PMF Output Control Register (PMFOUTC)

Address: Module Base + 0x000C Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-13. PMF Output Control Register (PMFOUTC)

1. Read: Anytime
   Write: Anytime

1. Read: Anytime
   Write: Only if GWP=0

Table 18-8. GDU Slew Rate Control Register Field Descriptions

Field	Description
6:4 GSRCHS[2:0]	GDU Slew Rate Control Bits High-Side FET Pre-Drivers — These bits control the slew rate on the HG[2:0] pins (see FET Pre-Driver Details) .These bits cannot be modified after GWP bit is set. 000 : slowest . . 111 : fastest
3:0 GSRCLS[2:0]	GDU Slew Rate Control Bits Low-Side FET Pre-Drivers — These bits control the slew rate on the LG[2:0] pins (see FET Pre-Driver Details). These bits cannot be modified after GWP bit is set. 000 : slowest . . 111 : fastest

Chapter 20
Flash Module (S12ZFTMRZ)

Table 20-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.03	12 Apr 2012	20.3	Corrected many typo. Changed caution note
V02.04	17 May 2012	20.3.2.6	- Removed flag DFDIE
V02.05	11 Jul 2012		- Added explanation about when MGSTAT[1:0] bits are cleared, Section 20.3.2.7 - Added note about possibility of reading P-Flash and EEPROM simultaneously, Section 20.4.6
V02.06	18 Mar 2013		- Standardized nomenclature in references to memory sizes
V02.07	24 May 2013		- Revised references to NVM Resource Area to improve readability
V02.8	12 Jun 2013		- Changed MLOADU Section 20.4.7.12 and MLOADF Section 20.4.7.13 **FCCOB1 to FCCOB2**
V02.9	15 Oct 2014		Created memory-size independent version of this module description

20.1 Introduction

The P-Flash (Program Flash) and EEPROM memory sizes are specified at device level (Reference Manual device overview chapter). The description in the following sections is valid for all P-Flash and EEPROM memory sizes.

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

> A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

21.4.2 Register Descriptions

This section describes all CAN Physical Layer registers and their individual bits.

21.4.2.1 Port CP Data Register (CPDR)

Module Base + 0x0000 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CPDR7	0	0	0	0	0	CPDR1	CPDR0
W								
Reset	1	0	0	0	0	0	1	1

Figure 21-2. Port CP Data Register (CPDR)

1. Read: Anytime
   Write: Anytime

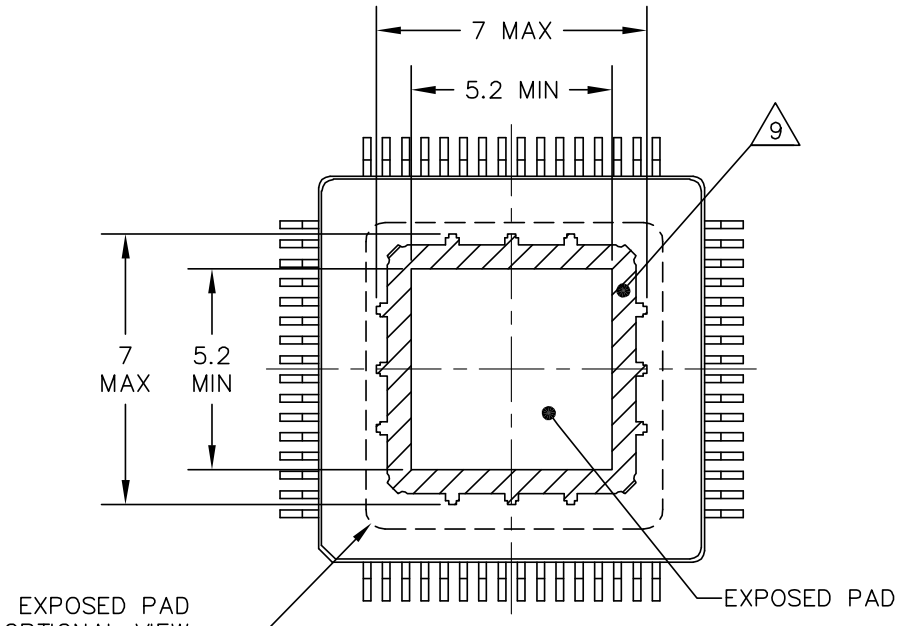
Table 21-4. CPDR Register Field Descriptions

Field	Description
7 CPDR7	Port CP Data Bit 7 Read-only bit. The synchronized CAN Physical Layer wake-up receiver output can be read at any time.
1 CPDR1	Port CP Data Bit 1 The CAN Physical Layer CPTXD input can be directly controlled through this register bit if routed here (see device-level specification). In this case the register bit value is driven to the pin. 0 CPTXD is driven low (dominant) 1 CPTXD is driven high (recessive)
0 CPDR0	Port CP Data Bit 0 Read-only bit. The synchronized CAN Physical Layer CPRXD output state can be read at any time.

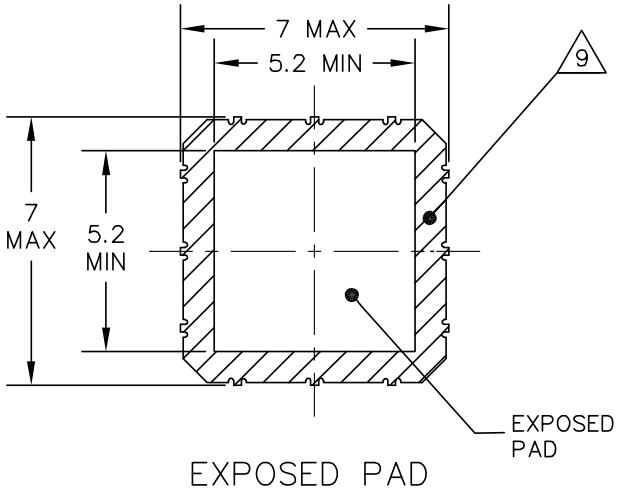
Table E-1. GDU Electrical Characteristics (Junction Temperature From –40°C To +175°C)

4.85V<=VDDX,VDDA<=5.15V						
33	Current Sense Amplifier output voltage range	V_{CSAout}	0	—	VDDA	V
34	Current Sense Amplifier open loop gain	AV_{CSA}	—	100000	—	—
35	Current Sense Amplifier common mode rejection ratio	$CMRR_{CSA}$	—	400	—	—
36	Current Sense Amplifier input offset	V_{CSAoff}	-15	—	15	mV
37	Max effective Current Sense Amplifier output resistance [0.1V .. VDDA - 0.2V]	R_{CSAout}	—	—	2	Ω
38	Min Current Sense Amplifier output current [0.1V .. VDDA - 0.2V](15)	I_{CSAout}	-750	—	750	μA
39	Current Sense Amplifier large signal settling time	t_{cslsst}	—	2.9	—	μs
40	Current Sense Amplifier unity gain bandwidth	GBW	—	1.9	—	MHz
41	Current Sense Amplifier input resistance	(16)	—	—	—	—
42	Over Current Comparator filter time constant(17)	τ_{OCC}	3	5	10	μs
43	Over Current Comparator threshold tolerance	V_{OCCtt}	-75	—	75	mV
44	HD input current when GDU is enabled	I_{HD}	—	130μ + V_{HD}/63K	—	A
45	VLS regulator minimum RDSon (VSUP >= 6V)	R_{VLSmin}	—	—	40	Ω
46	VCP to VBSx switch resistance	R_{VCPVBS}	—	600	1000	Ω
47	VBSx current whilst high side inactive	I_{VBS}	—	—	310	μA
48a	Desaturation comparator filter time constant fast (GDU V6 GDSFHS/GDSFLS=0) (GDU V4 high side) (GDU V4 low side on all mask sets except 3N95G)	τ_{desatf}	90	—	250	ns
48b	Desaturation comparator filter time constant slow (GDU V6 GDSFHS/GDSFLS=1) (GDU V4 mask set 3N95G low side)	τ_{desats}	240	—	670	ns
49a	LS desaturation comparator level, GDUV6, GDSLLS = 000 (18)	$V_{desatls}$	0.23	0.35	0.46	V
49b	LS desaturation comparator level, GDUV6, GDSLLS = 001(18)	$V_{desatls}$	0.355	0.5	0.645	V
49c	LS desaturation comparator level, GDUV6, GDSLLS = 010(18)	$V_{desatls}$	0.46	0.65	0.84	V
49d	LS desaturation comparator level, GDUV6, GDSLLS = 011(18)	$V_{desatls}$	0.575	0.8	1.035	V
49e	LS desaturation comparator level, GDUV6, GDSLLS = 100(18)	$V_{desatls}$	0.69	0.95	1.23	V
49f	LS desaturation comparator level, GDUV6, GDSLLS = 101(18)	$V_{desatls}$	0.81	1.1	1.41	V
49g	LS desaturation comparator level, GDUV6, GDSLLS = 110(18)	$V_{desatls}$	0.925	1.25	1.605	V
49h	LS desaturation comparator level, GDUV6, GDSLLS = 111(18)	$V_{desatls}$	1.03	1.4	1.81	V
50a	HS desaturation comparator level, GDUV6, GDSLHS = 000	$V_{desaths}$	V_{HD}-0.23	V_{HD}-0.35	V_{HD}-0.46	V
50b	HS desaturation comparator level, GDUV6, GDSLHS = 001	$V_{desaths}$	V_{HD}-0.355	V_{HD}-0.5	V_{HD}-0.645	V
50c	HS desaturation comparator level, GDUV6, GDSLHS = 010	$V_{desaths}$	V_{HD}-0.46	V_{HD}-0.65	V_{HD}-0.84	V
50d	HS desaturation comparator level, GDUV6, GDSLHS = 011	$V_{desaths}$	V_{HD}-0.575	V_{HD}-0.8	V_{HD}-1.035	V
50e	HS desaturation comparator level, GDUV6, GDSLHS = 100	$V_{desaths}$	V_{HD}-0.69	V_{HD}-0.95	V_{HD}-1.23	V
50f	HS desaturation comparator level, GDUV6, GDSLHS = 101	$V_{desaths}$	V_{HD}-0.81	V_{HD}-1.1	V_{HD}-1.41	V
50g	HS desaturation comparator level, GDUV6, GDSLHS = 110	$V_{desaths}$	V_{HD}-0.925	V_{HD}-1.25	V_{HD}-1.605	V
50h	HS desaturation comparator level, GDUV6, GDSLHS = 111	$V_{desaths}$	V_{HD}-1.03	V_{HD}-1.4	V_{HD}-1.81	V

1. Without using the boost option. The minimum level can be relaxed when the boost option is used. The lower limit is sensed on VLS, the upper limit is sensed on HD.
2. Without using the boost option. The minimum level can be relaxed when the boost option is used. The lower limit is sensed on VLS, the upper limit is sensed on HD. Operation beyond 20V is limited to 1 hour over lifetime of the device



VIEW J–J

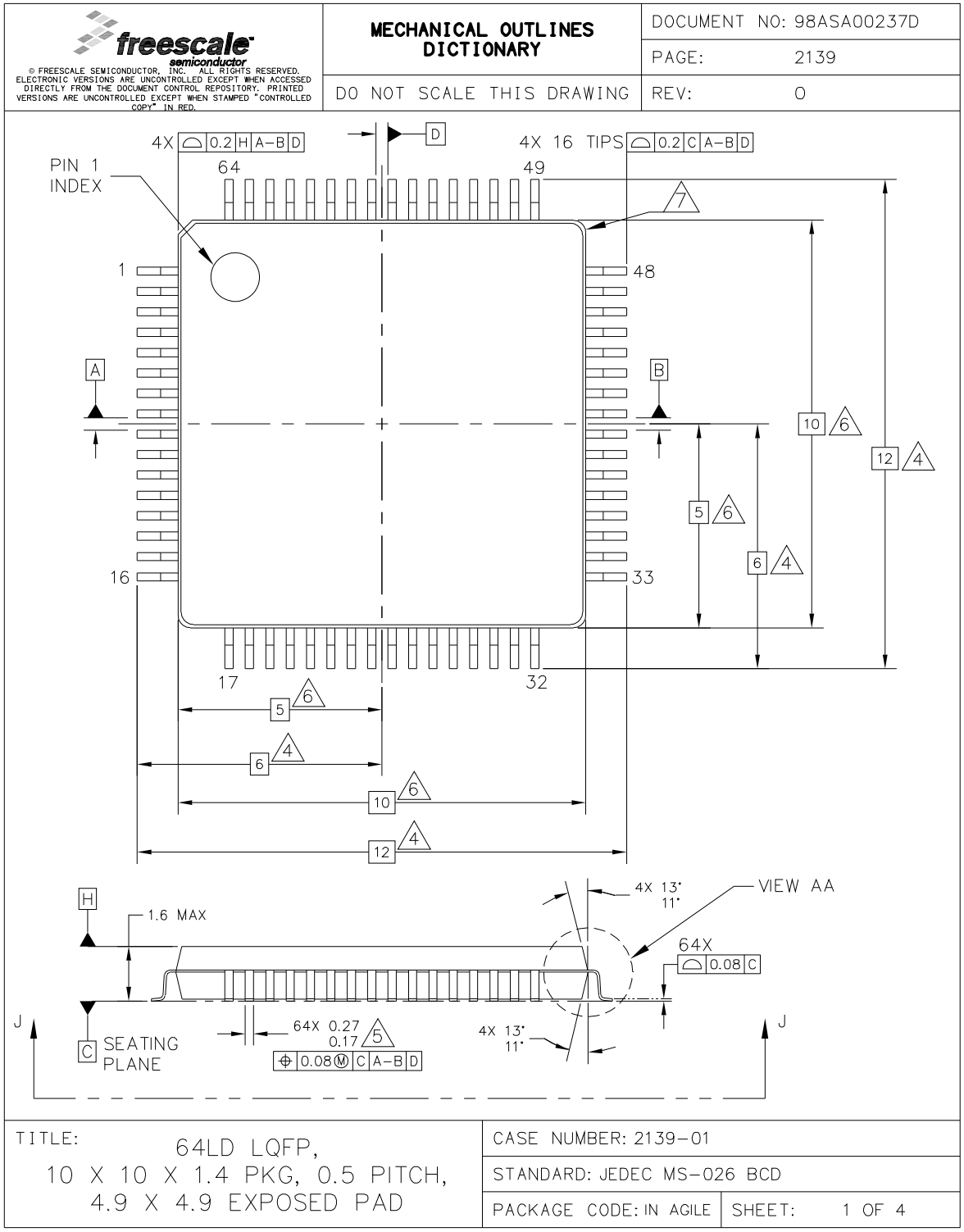


EXPOSED PAD
OPTIONAL VIEW

TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER:	1899-03
		STANDARD:	JEDEC MS-026 BCD
		SHEET:	2

K.3 64LQFP-EP Mechanical Information (mask sets 1N95G, 2N95G)

Figure K-3. 64LQFP-EP Mechanical Information (mask sets 1N95G, 2N95G)



M.2 0x0010–0x001F S12ZINT

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001F	INT_CFDATA7	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0261	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0262	PTIE	R	0	0	0	0	0	0	PTIE1	PTIE0
		W								
0x0263	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0264	DDRE	R	0	0	0	0	0	0	DDRE1	DDRE0
		W								
0x0265	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0266	PERE	R	0	0	0	0	0	0	PERE1	PERE0
		W								
0x0267	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0268	PPSE	R	0	0	0	0	0	0	PPSE1	PPSE0
		W								
0x0269–0x027F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0280	PTADH	R	PTADH7[2]	PTADH6[2]	PTADH5[2]	PTADH4[2]	PTADH3[2]	PTADH2[2]	PTADH1[2]	PTADH0
		W								
0x0281	PTADL	R	PTADL7	PTADL6	PTADL5	PTADL4	PTADL3	PTADL2	PTADL1	PTADL0
		W								
0x0282	PTIADH	R	PTIADH7[2]	PTIADH6[2]	PTIADH5[2]	PTIADH4[2]	PTIADH3[2]	PTIADH2[2]	PTIADH1[2]	PTIADH0
		W								
0x0283	PTIADL	R	PTIADL7	PTIADL6	PTIADL5	PTIADL4	PTIADL3	PTIADL2	PTIADL1	PTIADL0
		W								

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F8–0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	RDRP	R	0	0	0	0	0	0	0	RDRP0
		W								
0x02FE–0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL[2]	R	0	0	0	0	0	0	0	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL[2]	R	0	0	0	0	0	0	0	PTPSL0
		W								
0x0334	PPSL[2]	R	0	0	0	0	0	0	0	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL[2]	R	0	0	0	0	0	0	0	PIEL0
		W								
0x0337	PIFL[2]	R	0	0	0	0	0	0	0	PIFL0
		W								