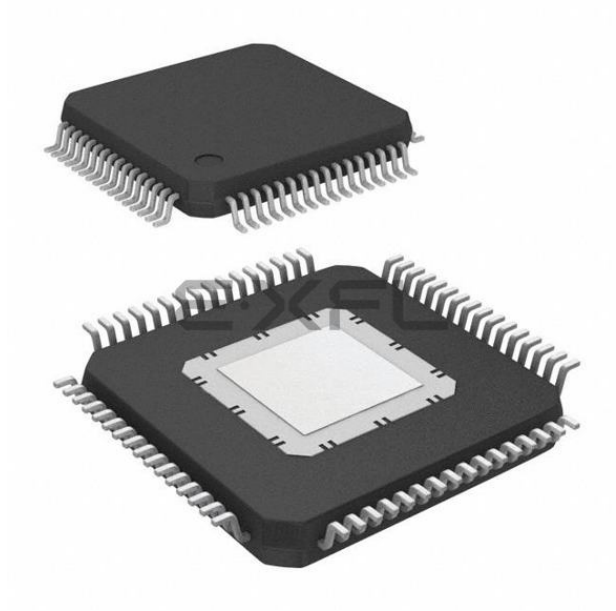

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Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f1mkh

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Detailed Register Address Map

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M.16 0x06C0-0x06DF CPMU . . . 988
M.17 0x06F0-0x06F7 BATS . . . 990

The exposed pad on the package bottom must be connected to a grounded contact pad on the PCB.

The LIN0 pin is mapped to the HV physical interface

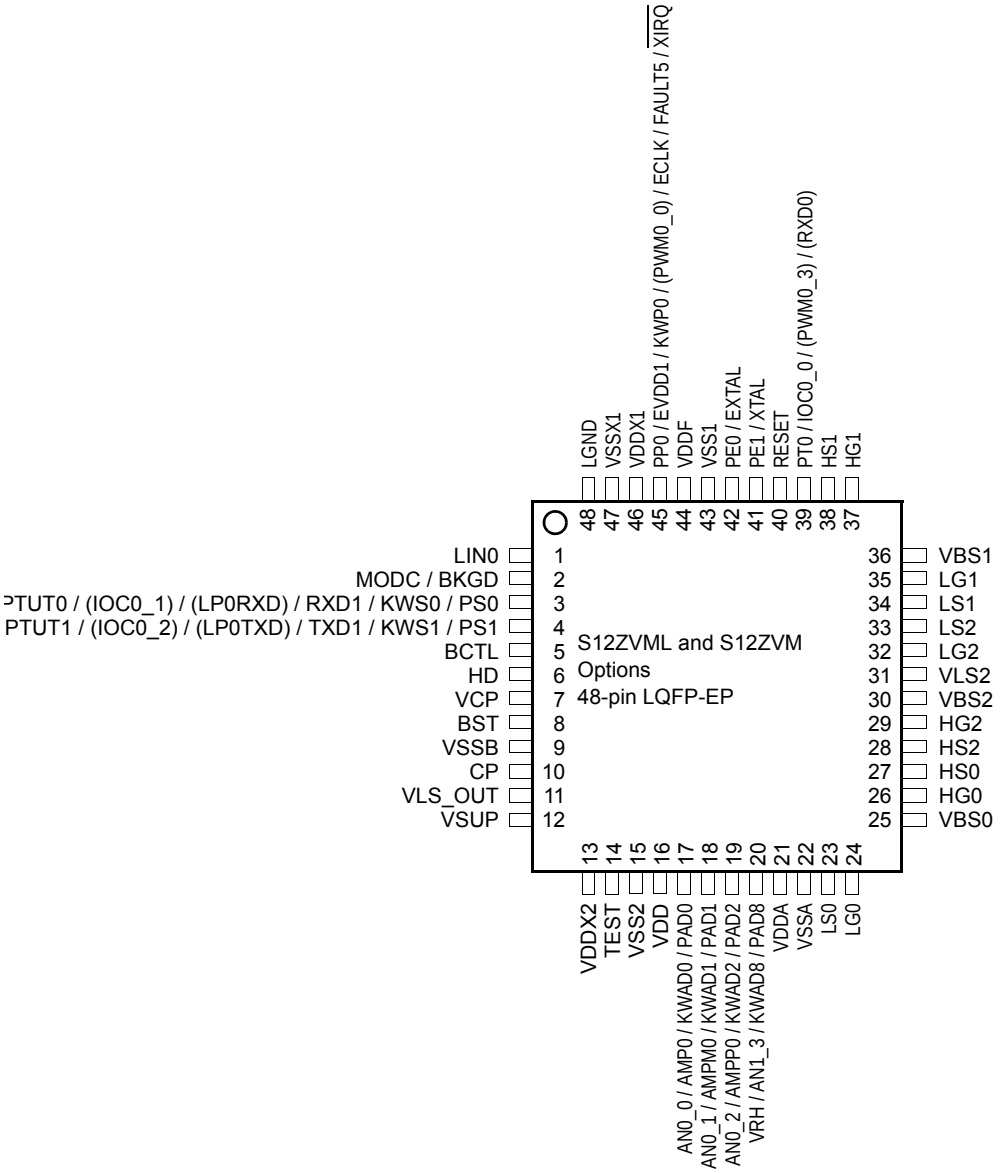
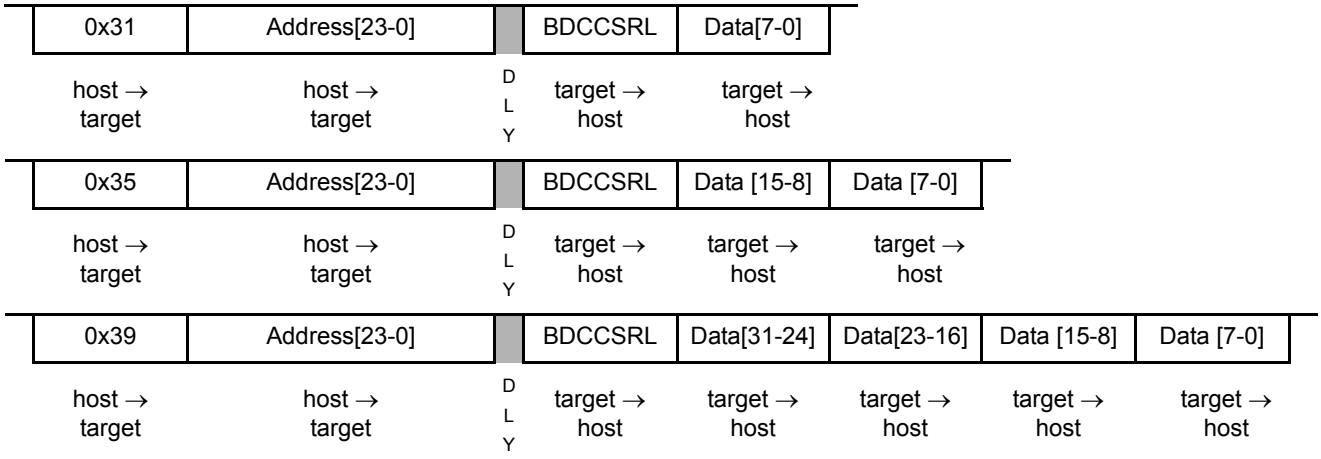


Figure 1-6. S12ZVM, S12ZVML Option 48-pin LQFP

READ_MEM.sz_WS

Read memory at the specified address with status **Non-intrusive**



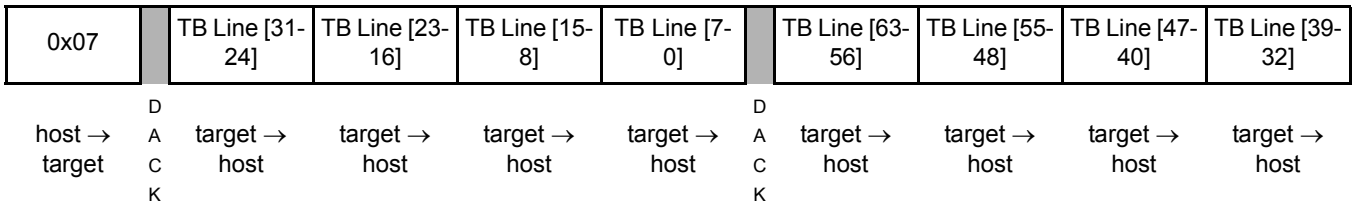
Read data at the specified memory address. The address is transmitted as three 8-bit packets (msb to lsb) immediately after the command.

The hardware forces low-order address bits to zero longword accesses to ensure these accesses are on 0-modulo-size alignments. Byte alignment details are described in Section 5.4.5.2”. If the with-status option is specified, the BDCCSR status byte is returned before the read data. This status byte reflects the state after the memory read was performed. If enabled, an ACK pulse is driven before the data bytes are transmitted.

The examples show the READ_MEM.B{_WS}, READ_MEM.W{_WS} and READ_MEM.L{_WS} commands.

5.4.4.12 READ_DBGTB

Read DBG trace buffer **Non-intrusive**



This command is only available on devices, where the DBG module includes a trace buffer. Attempted use of this command on devices without a traace buffer return 0x00.

Read 64 bits from the DBG trace buffer. Refer to the DBG module description for more detailed information. If enabled an ACK pulse is generated before each 32-bit longword is ready to be read by the host. After issuing the first ACK a timeout is still possible whilst accessing the second 32-bit longword, since this requires separate internal accesses. The first 32-bit longword corresponds to trace buffer line

7.2.2.3 ECC Interrupt Flag Register (ECCIF)

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIF
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime, write 1 to clear

Figure 7-4. ECC Interrupt Flag Register (ECCIF)

Table 7-4. ECCIF Field Description

Field	Description
0 SBEEIF	Single bit ECC Error Interrupt Flag — The flag is set to 1 when a single bit ECC error occurs. 0 No occurrences of single bit ECC error since the last clearing of the flag 1 Single bit ECC error has occured since the last clearing of the flag

9.5.2.23 ADC Command and Result Offset Register 0 (ADCCROFF0)

Module Base + 0x0024

	7	6	5	4	3	2	1	0
R	0	CMDRES_OFF0[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-26. ADC Command and Result Offset Register 0 (ADCCROFF0)

Read: Anytime

Write: NA

Table 9-31. ADCCROFF0 Field Descriptions

Field	Description
6-0 CMDRES_OFF0[6:0]	**ADC Command and Result Offset Value** — These read only bits represent the conversion command and result offset value relative to the conversion command base pointer address and result base pointer address in the memory map to refer to CSL_0 and RVL_0. It is used to calculate the address inside the system RAM to which the result at the end of the current conversion is stored to and the area (RAM or NVM) from which the conversion commands are loaded from. This is a zero offset (null offset) which can not be modified. These bits do not represent absolute addresses instead it is a sample offset (object size 16bit for RVL, object size 32bit for CSL). See also Section 9.6.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) and Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs) for more details.

Table 11-4. TSCR1 Field Descriptions (continued)

Field	Description
5 TSFRZ	Timer Stops While in Freeze Mode 0 Allows the timer counter to continue running while in freeze mode. 1 Disables the timer counter whenever the MCU is in freeze mode. This is useful for emulation. TSFRZ does not stop the pulse accumulator.
4 TFFCA	Timer Fast Flag Clear All 0 Allows the timer flag clearing to function normally. 1 For TFLG1(0x000E), a read from an input capture or a write to the output compare channel (0x0010–0x001F) causes the corresponding channel flag, CnF, to be cleared. For TFLG2 (0x000F), any access to the TCNT register (0x0004, 0x0005) clears the TOF flag. This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses.
3 PRNT	Precision Timer 0 Enables legacy timer. PR0, PR1, and PR2 bits of the TSCR2 register are used for timer counter prescaler selection. 1 Enables precision timer. All bits of the PTPSR register are used for Precision Timer Prescaler Selection, and all bits. This bit is writable only once out of reset.

11.3.2.5 Timer Toggle On Overflow Register 1 (TTOV)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	TOV3	TOV2	TOV1	TOV0
Reset	0	0	0	0	0	0	0	0

Figure 11-9. Timer Toggle On Overflow Register 1 (TTOV)

Read: Anytime

Write: Anytime

Table 11-5. TTOV Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 TOV[3:0]	**Toggle On Overflow Bits** — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.

13.5 Initialization/Application Information

13.5.1 MSCAN initialization

The procedure to initially start up the MSCAN module out of reset is as follows:

1. Assert CANE
2. Write to the configuration registers in initialization mode
3. Clear INITRQ to leave initialization mode

If the configuration of registers which are only writable in initialization mode shall be changed:

1. Bring the module into sleep mode by setting SLPRQ and awaiting SLPAK to assert after the CAN bus becomes idle.
2. Enter initialization mode: assert INITRQ and await INITAK
3. Write to the configuration registers in initialization mode
4. Clear INITRQ to leave initialization mode and continue

13.5.2 Bus-Off Recovery

The bus-off recovery is user configurable. The bus-off state can either be left automatically or on user request.

For reasons of backwards compatibility, the MSCAN defaults to automatic recovery after reset. In this case, the MSCAN will become error active again after counting 128 occurrences of 11 consecutive recessive bits on the CAN bus (see the Bosch CAN 2.0 A/B specification for details).

If the MSCAN is configured for user request (BORM set in MSCAN Control Register 1 (CANCTL1)), the recovery from bus-off starts after both independent events have become true:

- 128 occurrences of 11 consecutive recessive bits on the CAN bus have been monitored
- BOHOLD in MSCAN Miscellaneous Register (CANMISC) has been cleared by the user

These two events may occur in any order.

- Global Load OK support, to guarantee coherent update of all control loop modules
- Trigger values stored inside the global memory map, basically inside system memory
- Software generated reload event and Trigger event generation for debugging

14.1.2 Modes of Operation

The PTU module behaves as follows in the system power modes:

1. Run mode

   All PTU features are available.
2. Wait mode
   All PTU features are available.
3. Freeze Mode

   Depends on the PTUFRZ register bit setting the internal counter is stopped and no trigger events will be generated.
4. Stop mode

   The PTU is disabled and the internal counter is stopped; no trigger events will be generated. The content of the configuration register is unchanged.

14.3.2.9 Trigger Generator 0 Trigger Value (TG0TVH, TG0TVL)

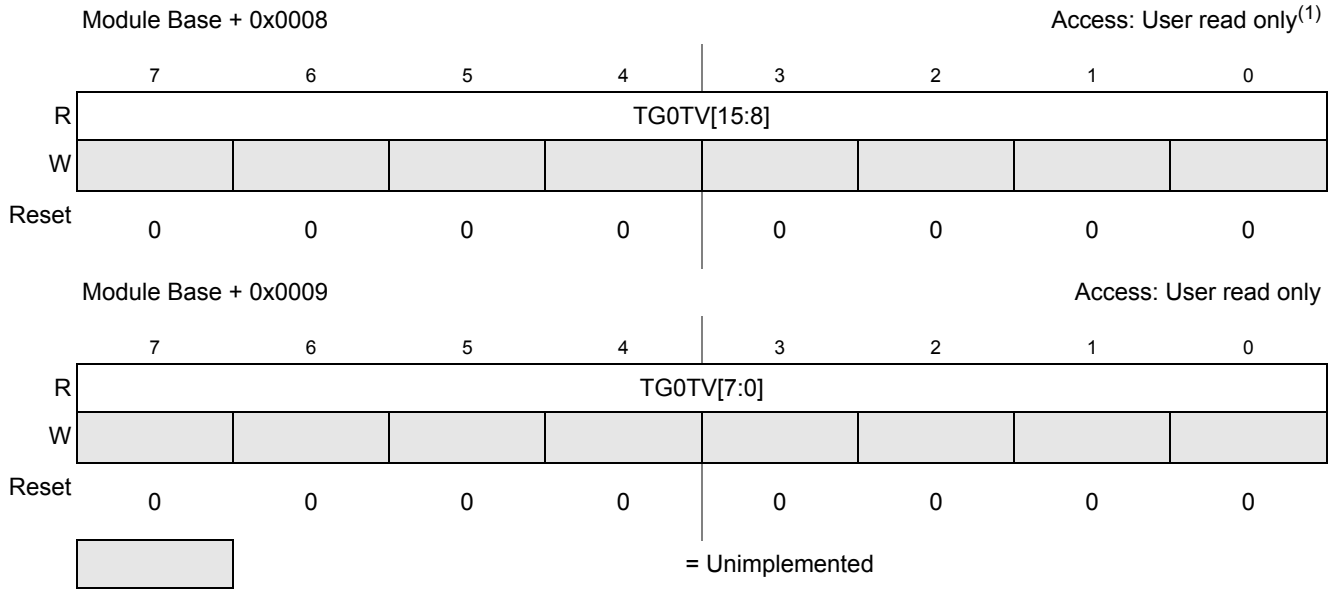


Figure 14-11. Trigger Generator 0 Trigger Value Register (TG0TVH, TG0TVL)

1. Read: Anytime
   Write: Never

Table 14-11. TG0TV Register Field Descriptions

Field	Description
TG0TV[15:0]	**Trigger Generator 0 Trigger Value** — This register contains the trigger value to generate the next trigger. If the time base counter reach this value the next trigger event is generated. If the trigger generator reached the end of list (EOL) symbol then this value is visible inside this register. If the last generated trigger was trigger number 32 then the last used trigger value is visible inside this register. See also Figure 14-22.

14.3.2.10 Trigger Generator 1 List Register (TG1LIST)

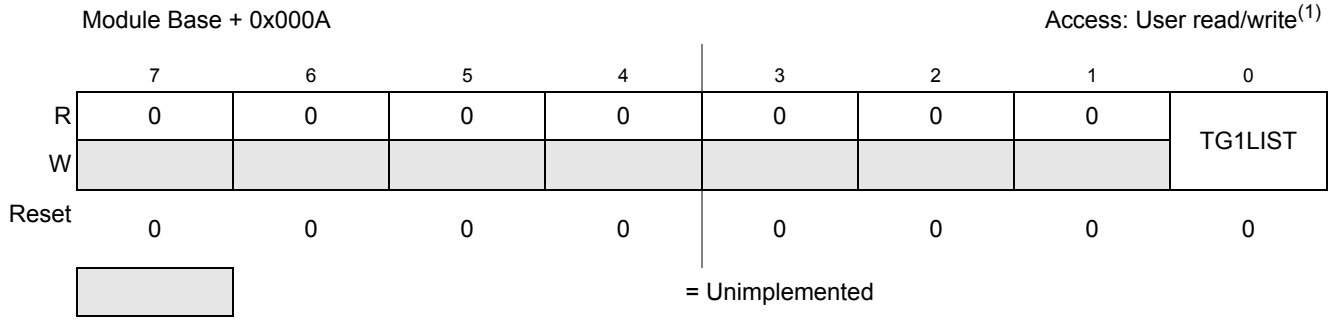


Figure 14-12. Trigger Generator 1 List Register (TG1LIST)

1. Read: Anytime
   Write: Anytime, if TG1EN bit is cleared

14.4.3 Reload mechanism

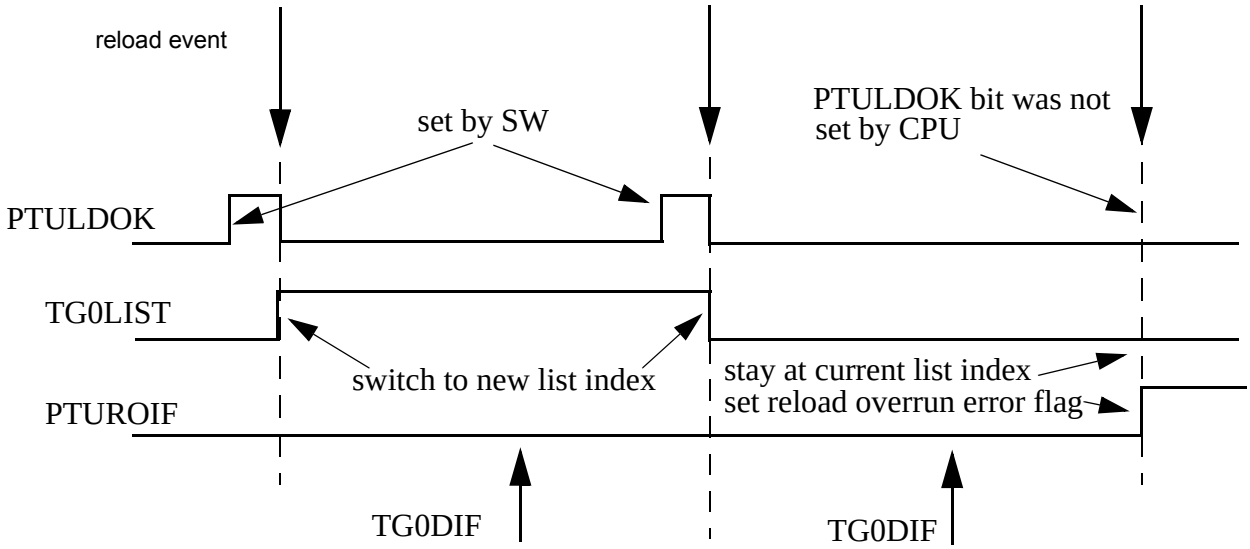
Each trigger generator uses two lists to load the trigger values from the memory. One list can be updated by the CPU while the other list is used to generate the trigger events. After enabling, the TG uses the lists in alternate order. When the update of alternate trigger list is done, the SW must set the PTULDOK bit. If the load OK bit is set at the time of reload event, the TG switches to the alternate list and loads the first trigger value from this trigger event list. The reload event clears the PTULDOK bit.

The TG0LIST and TG1LIST bits shows the currently use list number. These bits are writeable if the associated TG is disabled.

If the PTULDOK bit was not set before the reload event then the reload overrun error flag is set (PTUROIF)and both TGs do not switch to the alternative list. The current trigger list is used to load the trigger values. Figure 14-24 shows an example. The PTULDOK bit can be used by other modules as glb_ldok.

To reduce the used memory size, it is also possible to set TG0L0IDX equal to TG0L1IDX or to set TG1L0IDX equal to TG1L1IDX. In this case the trigger generator is using only one physical list of trigger events even if the trigger generator logic is switching between both pointers. The SW must make sure, that the CPU does not update the trigger list before the execution of the trigger list is done. The time window to update the trigger list starts at the trigger generator done interrupt flag (TGxDIF) and ends with the next reload event. Even if only one physical trigger event list is used the TGxLIST shows a swap between list 0 and 1 at every reload event with set PTULDOK bit.

Figure 14-24. TG0 Reload behavior with local PTULDOK



14.4.4 Async reload event

If the reload and reload_is_async are active at the same time then an async reload event happens. The PTU behavior on an async reload event is the same like on the reload event described in Section 14.4.3, “Reload

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x002A	PMFCNTB	R	0	PMFCNTB						
		W								
0x002B	PMFCNTB	R	PMFCNTB							
		W								
0x002C	PMFMODB	R	0	PMFMODB						
		W								
0x002D	PMFMODB	R	PMFMODB							
		W								
0x002E	PMFDTMB	R	0	0	0	0	PMFDTMB			
		W								
0x002F	PMFDTMB	R	PMFDTMB							
		W								
0x0030	PMFENCC	R	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC
		W								
0x0031	PMFFQCC	R	LDFQC				HALFC	PRSCC		PWMRFC
		W								

= Unimplemented or Reserved

Figure 15-2. Quick Reference to PMF Registers (Sheet 4 of 5)

The complementary channel operation is for driving top and bottom transistors in a motor drive circuit, such as the one in Figure 15-49.

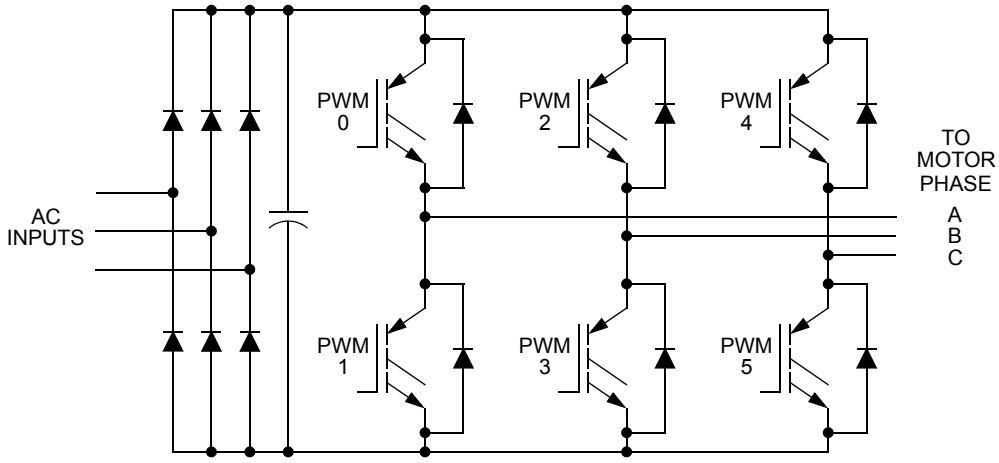


Figure 15-49. Typical 3-Phase AC Motor Drive

In complementary channel operation following additional features exist:

- Deadtime insertion
- Separate top and bottom pulse width correction via current status inputs or software
- Three variants of PWM output:
  - — Asymmetric in center-aligned mode
  - — Variable edge placement in edge-aligned mode
  - — Double switching in center-aligned mode

15.4.5 Deadtime Generators

While in complementary operation, each PWM pair can be used to drive top/bottom transistors, as shown in Figure 15-50. Ideally, the PWM pairs are an inversion of each other. When the top PWM channel is active, the bottom PWM channel is inactive, and vice versa.

NOTE

To avoid a short-circuit on the DC bus and endangering the transistor, there must be no overlap of conducting intervals between the top and bottom transistor. But the transistor's characteristics make its switching-off time longer than switching-on time. To avoid the conducting overlap of the top and bottom transistors, deadtime needs to be inserted in the switching period.

Deadtime generators automatically insert software-selectable activation delays into each pair of PWM outputs. The deadtime register (PMFDTMx) specifies the number of PWM clock cycles to use for deadtime delay. Every time the deadtime generator inputs changes state, deadtime is inserted. Deadtime forces both PWM outputs in the pair to the inactive state.

A method of correcting this, adding to or subtracting from the PWM value used, is discussed next.

18.5.3 Calculation of Bootstrap Capacitor

The size of the bootstrap capacitor C_{BS} depends on the total gate charge Q_G needed to turn on the power FET used in the application. If the bootstrap capacitor is too small there can be a large voltage drop due to charge sharing between bootstrap capacitor C_{BS} and the total gate capacitance of the power FET C_G. The resulting voltage on the gate of the power FET can be calculated as follow:

Eqn. 18-1

$$V_G = \frac{Q_{BS}}{C_{BS} + C_G} = \frac{V_{BS}}{1 + \frac{C_G}{C_{BS}}}$$

For example if $C_{BS} = 20\ C_G$ then the resulting gate voltage is $V_G = 0.95\ V_{BS}$.

18.5.4 On Chip GDU t_{delon} and t_{deloff} Measurement

The S12ZVM256 provides the capability to measure the GDU t_{delon} and t_{deloff} delays of the high-side and low-side drivers with the on chip timer. The timing diagram Figure 18-32 shows the basic concept. The high-side and low-side drivers provide the feedback signals hs0_fb and ls0_fb which indicate that the drivers are turned on or off. The feedback signals and the related pwm signals are used to generate the gdu_del_on_off output signal. (see Figure 18-32) This signal can be routed to TIM1 input capture channel IOC1_0 for pulse width measurement.

Following below are the steps to do the delay measurement:

- 1. Route gdu_del_on_off signal to TIM1 IOC1_0 in PIM routing register MODRR2.T1ICORR
- 2. Setup TIM1 IOC1_0 for pulse width measurement
- 3. Use software control of PWM output feature PMFOUTC and PMFOUTB to assert PWM0
- 4. Store measured pulse width (t_{delon} of high-side driver 0) in RAM
- 5. Use software control of PWM output feature PMFOUTC and PMFOUTB to deassert PWM0
- 6. Store measured pulse width (t_{deloff} of high-side driver 0) in RAM
- repeat 3 to 6 for all PWM channels

A stronger external pullup resistor might be necessary to sustain communication speeds up to 250 kbit/s. The signal on the LIN pin and the LPRxD signal might not be symmetrical for high baud rates with high loads on the bus.

Please note that if the bit time is smaller than the parameter t_{OCLIM} (please refer to electricals), then no overcurrent is reported nor does an overcurrent shutdown occur. However, the current limitation is always engaged in case of a failure.

19.4.3 Modes

Figure 19-11 shows the possible mode transitions depending on control bits, stop mode, and error conditions.

19.4.3.1 Shutdown Mode

The LIN/HV Physical Layer is fully disabled. No wake-up functionality is available. The internal pullup resistor is high ohmic only (330 kΩ) to maintain the LIN pin in the recessive state. LPTxD is not monitored in this mode for a TxD-dominant timeout. All the registers are accessible.

Setting LPE causes the module to leave the shutdown mode and to enter the normal mode or receive only mode (if RXONLY bit is set).

Clearing LPE causes the module to leave the normal or receive only modes and go back to shutdown mode.

19.4.3.2 Normal Mode

The full functionality is available. Both receiver and transmitter are enabled. The internal pullup resistor can be chosen to be high ohmic (330 kΩ) if LPPUE = 0, or LIN compliant (34 kΩ) if LPPUE = 1.

If RXONLY is set, the module leaves normal mode to enter receive only mode.

If the MCU enters stop mode, the LIN/HV Physical Layer enters standby mode.

19.4.3.3 Receive Only Mode

Entering this mode disables the transmitter and immediately stops any on-going transmission. LPTxD is not monitored in this mode for a TxD-dominant timeout.

The receiver is running in full performance mode in all cases.

To return to normal mode, the RXONLY bit must be cleared.

If the device enters stop mode, the module leaves receive only mode to enter standby mode.

19.4.3.4 Standby Mode with Wake-Up Feature

The transmitter of the LIN/HV Physical Layer is disabled and the receiver enters a low power mode.

NOTE

Before entering standby mode, please ensure that no transmission is ongoing.

Table 20-51. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied see Table 20-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 20-52. Unsecure Flash Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 20-53. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 20-29)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 20-10). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 20-

20.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0xFF_FE00-0xFF_FE07). If the KEYEN[1:0] bits are in the enabled state (see Section 20.3.2.2), the Verify Backdoor Access Key command (see Section 20.4.7.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 20-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 20.3.2.2), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Section 20.4.7.11
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0xFF_FE0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0xFF_FE00-0xFF_FE07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF_FE00-0xFF_FE07 in the Flash configuration field.

20.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

A secured MCU can be unsecured in special single chip mode using an automated procedure described in Section 20.4.7.7.1, “Erase All Pin”.

20.5.3 Mode and Security Effects on Flash Command Availability

The availability of Flash module commands depends on the MCU operating mode and security state as shown in Table 20-29.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0006 PWMCLKAB [1]	R	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
	W								
0x0007 RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x0008 PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0009 PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x000A RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x000B RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x000C PWMCNT0 [2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000D PWMCNT1[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000E PWMCNT2[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000F PWMCNT3[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0010 PWMCNT4[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0011 PWMCNT5[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0012 PWMCNT6[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0013 PWMCNT7[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

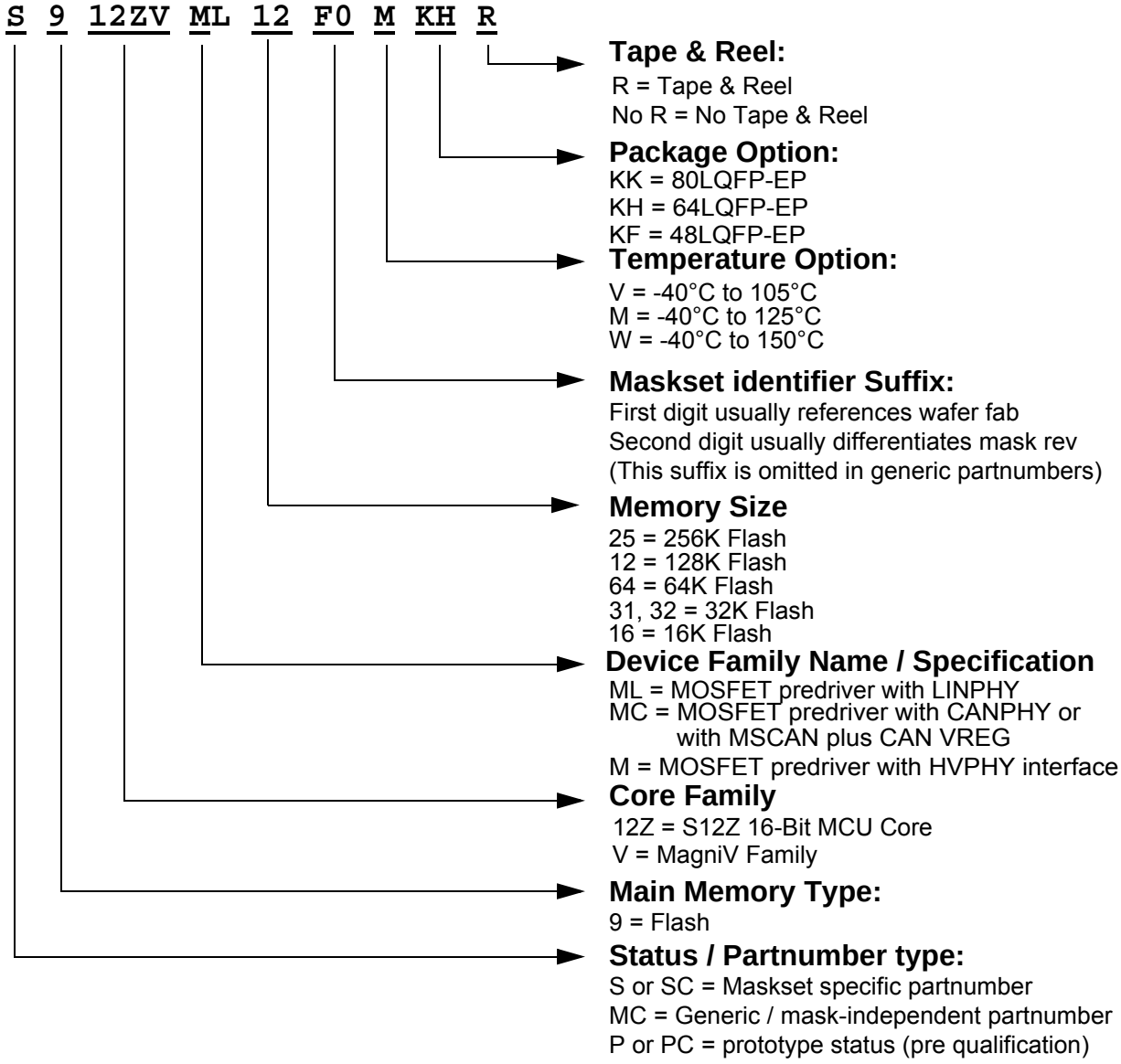
Figure 22-2. The scalable PWM Register Summary (Sheet 2 of 4)

Appendix L
Ordering Information

Customers can choose either the mask-specific partnumber or the generic, mask-independent partnumber. Ordering a mask-specific partnumber enables the customer to specify which particular maskset they receive whereas ordering the generic partnumber means that the currently preferred maskset (which may change over time) is shipped. In either case, the marking on the device always shows the generic, mask-independent partnumber and the mask set number. The below figure illustrates the structure of a typical mask-specific ordering number.

NOTES

Not every combination is offered. Table 1.2.1 lists available derivatives.
The mask identifier suffix and the Tape & Reel suffix are always both omitted from the partnumber which is actually marked on the device.



M.2 0x0010–0x001F S12ZINT

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001F	INT_CFDATA7	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								