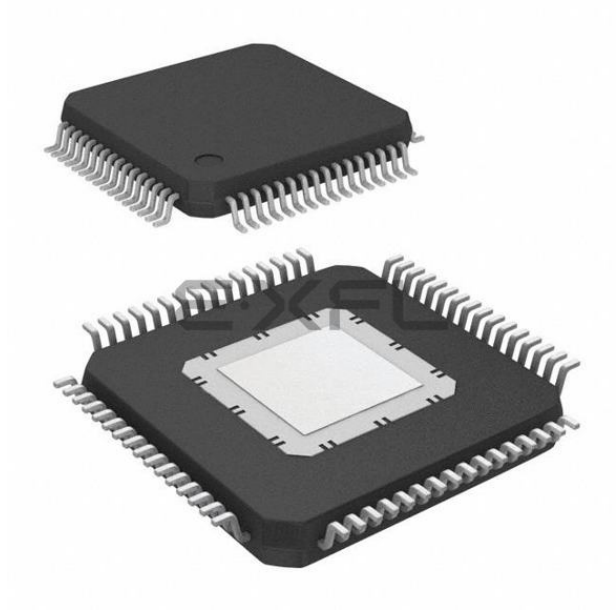

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Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f1mkhr

Table 1-8. Pin Summary For 64-Pin and 48-Pin Package Options (Sheet 2 of 4)

LQFP Option				Function (Priority and device dependencies specified in PIM chapter)					Power Supply	Internal Pull Resistor	
64 M/ ML	64 MC	48	Pin	1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
20	20	16	VDD	—	—	—	—	—	V_{DD}	—	—
21	21	17	PAD0	KWAD0	AN0_0	AMP0	—	—	V_{DDA}	PERADL /PPSADL	Off
22	22	18	PAD1	KWAD1	AN0_1	AMPM0	—	—	V_{DDA}	PERADL /PPSADL	Off
23	23	19	PAD2	KWAD2	AN0_2	AMPP0	—	—	V_{DDA}	PERADL /PPSADL	Off
24	24	—	PAD3	KWAD3	AN0_3	—	—	—	V_{DDA}	PERADL /PPSADL	Off
25	25	—	PAD4	KWAD4	AN0_4	—	—	—	V_{DDA}	PERADL /PPSADL	Off
26	26	—	PAD5	KWAD5	AN1_0	AMP1	—	—	V_{DDA}	PERADL /PPSADL	Off
27	27	—	PAD6	KWAD6	AN1_1	AMPM1	SS0	—	V_{DDA}	PERADL /PPSADL	Off
28	28	—	PAD7	KWAD7	AN1_2	AMPP1	—	—	V_{DDA}	PERADL /PPSADL	Off
29	29	20	PAD8	KWAD8	AN1_3	VRH0_0	VRH1_0	—	V_{DDA}	PERADH/PPSADH	Off
30	30	21	VDDA	VRH0_1	VRH1_1	—	—	—	V_{DDA}	—	—
31	31	22	VSSA	VRL0_ [1:0]	VRL1_ [1:0]	—	—	—	V_{DDA}	—	—
32	32	23	LS0	—	—	—	—	—	—	—	—
33	33	24	LG0	—	—	—	—	—	—	—	—
34	34	—	VLS0	—	—	—	—	—	—	—	—
35	35	25	VBS0	—	—	—	—	—	—	—	—

Table 2-20. Pull Device Enable Register Field Descriptions

Field	Description
7-0 PERx7-0	**Pull Enable** — Activate pull device on input pin This bit controls whether a pull device on the associated port input or open-drain output pin is active. If a pin is used as push-pull output this bit has no effect. The polarity is selected by the related polarity select register bit. On open-drain output pins only a pullup device can be enabled. 1 Pull device enabled 0 Pull device disabled

2.3.3.5 Polarity Select Register

Address 0x0268 PPSE
0x0288 PPSADH
0x0289 PPSADL
0x02C4 PPST
0x02D4 PPSS

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PPSx7	PPSx6	PPSx5	PPSx4	PPSx3	PPSx2	PPSx1	PPSx0
Reset								
Ports E:	0	0	0	0	0	0	1	1
Others:	0	0	0	0	0	0	0	0

Figure 2-16. Polarity Select Register

1. Read: Anytime
Write: Anytime

This is a generic description of the standard polarity select registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-21. Polarity Select Register Field Descriptions

Field	Description
7-0 PPSx7-0	**Pull Polarity Select** — Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. If a port has interrupt functionality this bit also selects the polarity of the active edge. If MSCAN is active a pullup device can be activated on the RXCAN input; attempting to select a pulldown disables the pull-device. 1 Pulldown device selected; rising edge selected 0 Pullup device selected; falling edge selected

Table 2-27. Port P Polarity Select Register Field Descriptions

Field	Description
2-1 PPSP	**See Section 2.3.3.5, “Polarity Select Register”**
0 PPSP	**Pull Polarity Select** — Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. This bit also selects the polarity of the active interrupt edge. This bit selects if a high or a low level on FAULT5 generates a fault event in PMF. 1 Pulldown device selected; rising edge selected; active-high level selected on FAULT5 input 0 Pullup device selected; falling edge selected; active-low level selected on FAULT5 input

2.3.4.2 Port P Interrupt Enable Register (PIEP)

Read: Anytime

Address 0x02F6 PIEP — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIE1	0	0	0	0	PIEP2	PIEP1	PIEP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-24. Port P Interrupt Enable Register

1. Read: Anytime
   Write: Anytime

Table 2-28. Port P Interrupt Enable Register Field Descriptions

Field	Description
7 OCIE1	**Over-Current Interrupt Enable register** — This bit enables or disables the over-current interrupt on PP0. 1 PP0 over-current interrupt enabled 0 PP0 over-current interrupt disabled (interrupt flag masked)
2-0 PIEP2-0	**See Section 2.3.3.6, “Port Interrupt Enable Register”**

- One non-maskable unimplemented page2 op-code trap
- One non-maskable software interrupt (SWI)
- One non-maskable system call interrupt (SYS)
- One non-maskable machine exception vector request
- One spurious interrupt vector request
- One system reset vector request

Each of the I-bit maskable interrupt requests can be assigned to one of seven priority levels supporting a flexible priority scheme. The priority scheme can be used to implement nested interrupt capability where interrupts from a lower level are automatically blocked if a higher level interrupt is being processed.

4.1.1 Glossary

The following terms and abbreviations are used in the document.

Table 4-2. Terminology

Term	Meaning
CCW	Condition Code Register (in the S12Z CPU)
DMA	Direct Memory Access
INT	Interrupt
IPL	Interrupt Processing Level
ISR	Interrupt Service Routine
MCU	Micro-Controller Unit
$\overline{\text{IRQ}}$	refers to the interrupt request associated with the $\overline{\text{IRQ}}$ pin
$\overline{\text{XIRQ}}$	refers to the interrupt request associated with the $\overline{\text{XIRQ}}$ pin

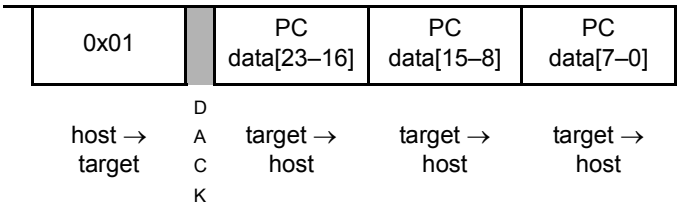
4.1.2 Features

- Interrupt vector base register (IVBR)
- One system reset vector (at address 0xFFFFFC).
- One non-maskable unimplemented page1 op-code trap (SPARE) vector (at address vector base[1] + 0x0001F8).
- One non-maskable unimplemented page2 op-code trap (TRAP) vector (at address vector base[1] + 0x0001F4).
- One non-maskable software interrupt request (SWI) vector (at address vector base[1] + 0x0001F0).
- One non-maskable system call interrupt request (SYS) vector (at address vector base[1] + 0x00001EC).
- One non-maskable machine exception vector request (at address vector base[1] + 0x0001E8).
- One spurious interrupt vector (at address vector base[1] + 0x0001DC).
- One X-bit maskable interrupt vector request associated with $\overline{\text{XIRQ}}$ (at address vector base[1] + 0x0001D8).

1. The vector base is a 24-bit address which is accumulated from the contents of the interrupt vector base register (IVBR, used as the upper 15 bits of the address) and 0x000 (used as the lower 9 bits of the address).

5.4.4.15 SYNC_PC

Sample current PC **Non-intrusive**



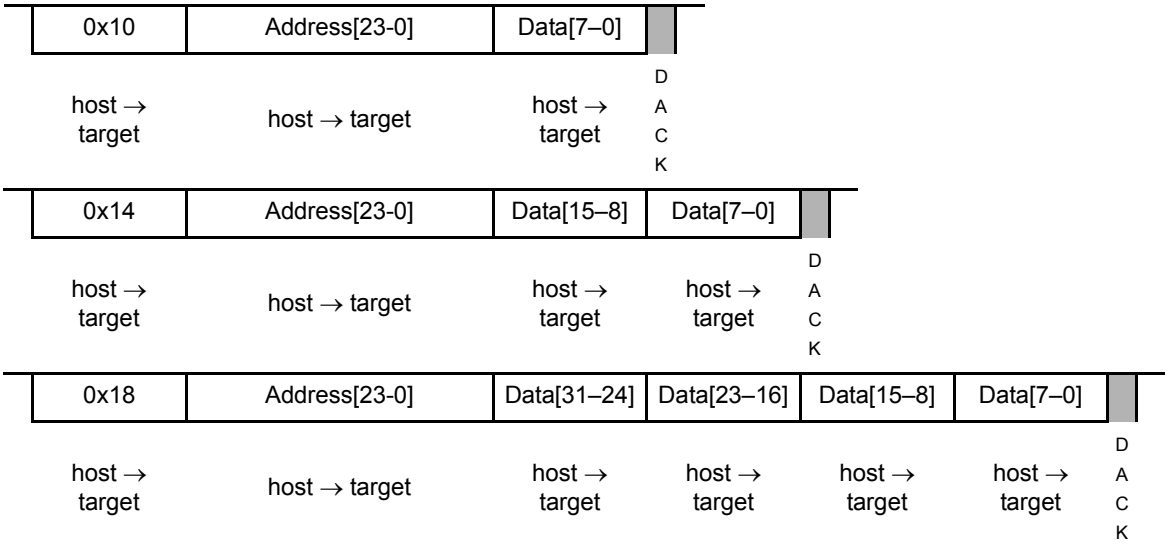
This command returns the 24-bit CPU PC value to the host. Unsuccessful SYNC_PC accesses return 0xEE for each byte. If enabled, an ACK pulse is driven before the data bytes are transmitted. The value of 0xEE is returned if a timeout occurs, whereby NORESP is set. This can occur if the CPU is executing the WAI instruction, or the STOP instruction with BDCCIS clear, or if a CPU access is delayed by EWAIT. If the CPU is executing the STOP instruction and BDCCIS is set, then SYNC_PC returns the PC address of the instruction following STOP in the code listing.

This command can be used to dynamically access the PC for performance monitoring as the execution of this command is considerably less intrusive to the real-time operation of an application than a BACKGROUND/read-PC/GO command sequence. Whilst the BDC is not in active BDM, SYNC_PC returns the PC address of the instruction currently being executed by the CPU. In active BDM, SYNC_PC returns the address of the next instruction to be executed on returning from active BDM. Thus following a write to the PC in active BDM, a SYNC_PC returns that written value.

5.4.4.16 WRITE_MEM.sz, WRITE_MEM.sz_WS

WRITE_MEM.sz

Write memory at the specified address **Non-intrusive**



6.3.2.18 Debug Comparator C Control Register (DBGCCTL)

Address: 0x0130

	7	6	5	4	3	2	1	0
R	0	NDB	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-20. Debug Comparator C Control Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-34. DBGCCTL Field Descriptions

Field	Description
6 NDB	**Not Data Bus** — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. This bit is ignored if the INST bit in the same register is set. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is not used if INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 6-35 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 6-35. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match

1. If the CDCM field selects range mode comparisons, then DBGCCTL bits configure the comparison, DBGDCTL is ignored.

Table 6-40 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 6-40. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

6.3.2.23 Debug Comparator D Address Register (DBGDAH, DBGDAM, DBGDAL)

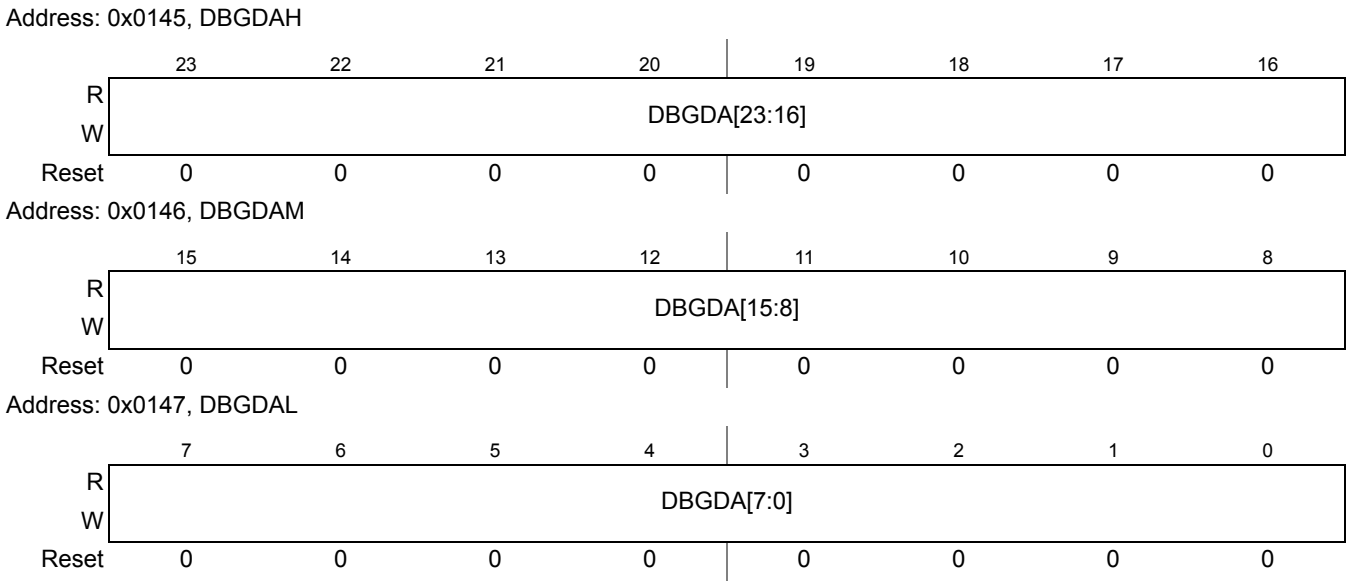


Figure 6-25. Debug Comparator D Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-41. DBGDAH, DBGDAM, DBGDAL Field Descriptions

Field	Description
23–16 DBGDA [23:16]	**Comparator Address Bits [23:16]—** These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

Table 6-53. Detail Mode Trace Buffer Format with Timestamp

Mode	8-Byte Wide Trace Buffer Line							
	7	6	5	4	3	2	1	0
CPU Detail	CDATA31	CDATA21	CDATA11	CDATA01	CINF1	CADRH1	CADRM1	CADRL1
	Timestamp	Timestamp	Reserved	Reserved	TSINF1	CPCH1	CPCM1	CPCL1
	CDATA32	CDATA22	CDATA12	CDATA02	CINF2	CADRH2	CADRM2	CADRL2
	CDATA33	CDATA23	CDATA13	CDATA03	CINF3	CADRH3	CADRM3	CADRL3
	Timestamp	Timestamp	Reserved	Reserved	TSINF3	CPCH3	CPCM3	CPCL3

Detail Mode data entries store the bytes aligned to the address of the MSB accessed (Byte1 Table 6-54). Thus accesses split across 32-bit boundaries are wrapped around.

Table 6-54. Detail Mode Data Byte Alignment

Access Address	Access Size	CDATA31	CDATA21	CDATA11	CDATA01
00	32-bit	Byte1	Byte2	Byte3	Byte4
01	32-bit	Byte4	Byte1	Byte2	Byte3
10	32-bit	Byte3	Byte4	Byte1	Byte2
11	32-bit	Byte2	Byte3	Byte4	Byte1
00	24-bit	Byte1	Byte2	Byte3	
01	24-bit		Byte1	Byte2	Byte3
10	24-bit	Byte3		Byte1	Byte2
11	24-bit	Byte2	Byte3		Byte1
00	16-bit	Byte1	Byte2		
01	16-bit		Byte1	Byte2	
10	16-bit			Byte1	Byte2
11	16-bit	Byte2			Byte1
00	8-bit	Byte1			
01	8-bit		Byte1		
10	8-bit			Byte1	
11	8-bit				Byte1
			Denotes byte that is not accessed.		

Information Bytes

BYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CINF	CSZ		CRW	0	0	0	0	0
TSINF	0	0	0	0	CTI	PC	1	TOVF

Figure 6-28. Information Bytes CINF and XINF

When tracing in Detail Mode, CINF provides information about the type of CPU access being made.

7.2.2.3 ECC Interrupt Flag Register (ECCIF)

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIF
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime, write 1 to clear

Figure 7-4. ECC Interrupt Flag Register (ECCIF)

Table 7-4. ECCIF Field Description

Field	Description
0 SBEEIF	Single bit ECC Error Interrupt Flag — The flag is set to 1 when a single bit ECC error occurs. 0 No occurrences of single bit ECC error since the last clearing of the flag 1 Single bit ECC error has occured since the last clearing of the flag

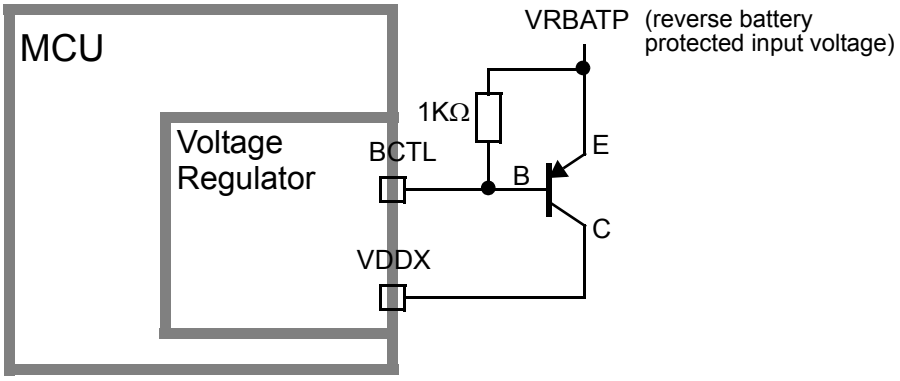


Figure 8-3. BCTL application example

8.2.10 BCTLC — Base Control Pin for external PNP for VDDC power domain

BCTLC is the ballast connection for the on chip voltage regulator for the VDDC power domain. It provides the base current of an external BJT (PNP) of the VDDC supply. An additional 1KΩ resistor between emitter and base of the BJT is required.

8.2.11 BCTLS1 — Base Control Pin for external PNP for VDDS1 power domain

BCTLS1 is the ballast connection for the on chip voltage regulator for the VDDS1 power domain. It provides the base current of an external BJT (PNP) of the VDDS1 supply. An additional 1KΩ resistor between emitter and base of the BJT is required.

Figure 8-4 shows an application example for the external BCTLS1 pin.

To generate a reload event or trigger event independent from the PWM status the debug register bits PTUFRE or TGxFTE can be used. A write one to this bits will generate the associated event.This behavior is not available during stop or freeze mode.

Table 15-8. PMFCFG2 Field Descriptions (continued)

Field	Description
5–0 MSK[5:0]	Mask PWM*n* — **Note:** MSK*n* are buffered if ENCE is set. The value written does not take effect until the next commutation cycle begins. Reading MSK*n* returns the value in the buffer and not necessarily the value the output control is currently using. 0 PWM*n* is unmasked 1 PWM*n* is masked and the channel is set to a value of 0 percent duty cycle *n* is 0. 1. 2. 3. 4. and 5.

1. only valid for module version V4

When using the TOPNEG/BOTNEG bits and the MSK*n* bits at the same time, when in complementary mode, it is possible to have both PMF channel outputs of a channel pair set to one.

15.3.2.4 PMF Configure 3 Register (PMFCFG3)

Address: Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PMFWAI	PMFFRZ	0	VLMODE		PINVC	PINVB	PINVA
W								
Reset	0	0	0	0	0	0	0	0

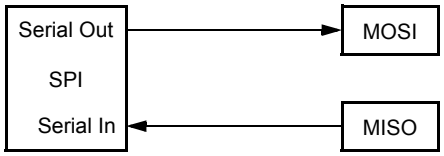
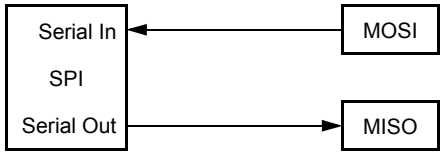
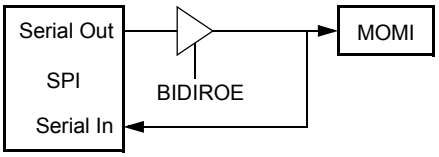
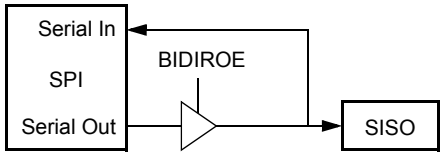
Figure 15-6. PMF Configure 3 Register (PMFCFG3)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set, except for bits PINVA, PINVB and PINVC

Table 15-9. PMFCFG3 Field Descriptions

Field	Description
7 PMFWAI	**PMF Stops While in WAIT Mode** — When set to zero, the PWM generators will continue to run while the chip is in WAIT mode. In this mode, the peripheral clock continues to run but the CPU clock does not. If the device enters WAIT mode and this bit is one, then the PWM outputs will be switched to their inactive state until WAIT mode is exited. At that point the PWM outputs will resume operation as programmed in the PWM registers. This bit cannot be modified after the WP bit is set. 0 PMF continues to run in WAIT mode 1 PMF is disabled in WAIT mode
6 PMFFRZ	**PMF Stops While in FREEZE Mode** — When set to zero, the PWM generators will continue to run while the chip is in FREEZE mode. If the device enters FREEZE mode and this bit is one, then the PWM outputs will be switched to their inactive state until FREEZE mode is exited. At that point the PWM outputs will resume operation as programmed in the PWM registers. This bit cannot be modified after the WP bit is set. 0 PMF continues to run in FREEZE mode 1 PMF is disabled in FREEZE mode

Table 17-11. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

The direction of each serial I/O pin depends on the BIDIROE bit. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

- The SCK is output for the master mode and input for the slave mode.
- The $\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.
- The bidirectional mode does not affect SCK and $\overline{SS}$ functions.

NOTE

In bidirectional master mode, with mode fault enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode. In this case MISO becomes occupied by the SPI and MOSI is not used. This must be considered, if the MISO pin is used for another purpose.

17.4.6 Error Conditions

The SPI has one error condition:

- Mode fault error

17.4.6.1 Mode Fault Error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation, the MODF bit in the SPI status register is set automatically, provided the MODFEN bit is set.

In the special case where the SPI is in master mode and MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. In case

21.4.2.2 CAN Physical Layer Control Register (CPCR)

Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CPE	SPE	WUPE1-0		0	SLR2-0		
W								
Reset	0	0	1	0	0	0	0	0

Figure 21-3. CAN Physical Layer Control Register (CPCR)

1. Read: Anytime
   Write: Anytime except CPE which is set once

Table 21-5. CPCR Register Field Descriptions

Field	Description
7 CPE	CAN Physical Layer Enable Set once. If set to 1, the CAN Physical Layer exits shutdown mode and enters normal mode. 0 CAN Physical Layer is disabled (shutdown mode) 1 CAN Physical Layer is enabled
6 SPE	Split Enable If set to 1, the CAN Physical Layer SPLIT pin drives a 2.5 V bias in normal and listen-only mode. 0 SPLIT pin is high-impedance 1 SPLIT pin drives a 2.5 V bias
5-4 WUPE1-0	Wake-Up Receiver Enable and Filter Select If WUPE[1:0]≠0, the CAN Physical Layer wake-up receiver is enabled when not in shutdown mode. To save additional power, these bits should be set to 00, if the CAN bus is not used to wake up the device. For robustness against false wake-up an optional pulse filter can be enabled. 00 Wake-up receiver is disabled 10 Wake-up receiver is enabled, no filtering 01 Wake-up receiver is enabled, first wake-up event is masked 11 Wake-up receiver is enabled, first two wake-up events are masked
2-0 SLR2-0	Slew Rate The slew rate controls recessive to dominant and dominant to recessive transitions. This affects the delay time from CPTXD to the bus and from the bus to CPRXD. The loop time is thus affected by the slew rate selection. Six slew rates are available: 000 CAN Physical Layer slew rate 0 001 CAN Physical Layer slew rate 1 010 CAN Physical Layer slew rate 2 011 Reserved 100 CAN Physical Layer slew rate 4 101 CAN Physical Layer slew rate 5 110 CAN Physical Layer slew rate 6 111 Reserved

Chapter 22
Pulse-Width Modulator (S12PWM8B8CV2)

Table 22-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
v02.00	Feb. 20, 2009	All	Initial revision of scalable PWM. Started from pwm_8b8c (v01.08).

22.1 Introduction

The Version 2 of S12 PWM module is a channel scalable and optimized implementation of S12 PWM8B8C Version 1. The channel is scalable in pairs from PWM0 to PWM7 and the available channel number is 2, 4, 6 and 8. The shutdown feature has been removed and the flexibility to select one of four clock sources per channel has improved. If the corresponding channels exist and shutdown feature is not used, the Version 2 is fully software compatible to Version 1.

22.1.1 Features

The scalable PWM block includes these distinctive features:

- Up to eight independent PWM channels, scalable in pairs (PWM0 to PWM7)
- Available channel number could be 2, 4, 6, 8 (refer to device specification for exact number)
- Programmable period and duty cycle for each channel
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- Up to eight 8-bit channel or four 16-bit channel PWM resolution
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
- Programmable clock select logic

22.1.2 Modes of Operation

There is a software programmable option for low power consumption in wait mode that disables the input clock to the prescaler.

Table 22-7. PWMPRCLK Field Descriptions

Field	Description
6–4 PCKB[2:0]	**Prescaler Select for Clock B** — Clock B is one of two clock sources which can be used for all channels. These three bits determine the rate of clock B, as shown in Table 22-8.
2–0 PCKA[2:0]	**Prescaler Select for Clock A** — Clock A is one of two clock sources which can be used for all channels. These three bits determine the rate of clock A, as shown in Table 22-8.

Table 22-8. Clock A or Clock B Prescaler Selects

PCKA/B2	PCKA/B1	PCKA/B0	Value of Clock A/B
0	0	0	bus clock
0	0	1	bus clock / 2
0	1	0	bus clock / 4
0	1	1	bus clock / 8
1	0	0	bus clock / 16
1	0	1	bus clock / 32
1	1	0	bus clock / 64
1	1	1	bus clock / 128

22.3.2.5 PWM Center Align Enable Register (PWMCAE)

The PWMCAE register contains eight control bits for the selection of center aligned outputs or left aligned outputs for each PWM channel. If the CAEx bit is set to a one, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. See Section 22.4.2.5, “Left Aligned Outputs” and Section 22.4.2.6, “Center Aligned Outputs” for a more detailed description of the PWM output modes.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
Reset	0	0	0	0	0	0	0	0

Figure 22-7. PWM Center Align Enable Register (PWMCAE)

Read: Anytime

Write: Anytime

NOTE

Write these bits only when the corresponding channel is disabled.

22.3.2.10 PWM Channel Counter Registers (PWMCNTx)

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source. The counter can be read at any time without affecting the count or the operation of the PWM channel. In left aligned output mode, the counter counts from 0 to the value in the period register - 1. In center aligned output mode, the counter counts from 0 up to the value in the period register and then back down to 0.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. The counter is also cleared at the end of the effective period (see Section 22.4.2.5, “Left Aligned Outputs” and Section 22.4.2.6, “Center Aligned Outputs” for more details). When the channel is disabled (PWMEx = 0), the PWMCNTx register does not count. When a channel becomes enabled (PWMEx = 1), the associated PWM counter starts at the count in the PWMCNTx register. For more detailed information on the operation of the counters, see Section 22.4.2.4, “PWM Timer Counters”.

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low or high order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

Module Base + 0x000C = PWMCNT0, 0x000D = PWMCNT1, 0x000E = PWMCNT2, 0x000F = PWMCNT3
Module Base + 0x0010 = PWMCNT4, 0x0011 = PWMCNT5, 0x0012 = PWMCNT6, 0x0013 = PWMCNT7

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 22-12. PWM Channel Counter Registers (PWMCNTx)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Read: Anytime

Write: Anytime (any value written causes PWM counter to be reset to $00).

22.3.2.11 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends

- The channel is disabled

In this way, the output of the PWM will always be either the old duty waveform or the new duty waveform, not some variation in between. If the channel is not enabled, then writes to the duty register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active duty due to the double buffering scheme.

See Section 22.4.2.3, “PWM Period and Duty” for more information.

NOTE

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time. If the polarity bit is one, the output starts high and then goes low when the duty count is reached, so the duty registers contain a count of the high time. If the polarity bit is zero, the output starts low and then goes high when the duty count is reached, so the duty registers contain a count of the low time.

To calculate the output duty cycle (high time as a% of period) for a particular channel:

- Polarity = 0 (PPOL x =0)

  Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
- Polarity = 1 (PPOLx = 1)

  Duty Cycle = [PWMDTYx / PWMPERx] * 100%

For boundary case programming values, please refer to Section 22.4.2.8, “PWM Boundary Cases”.

Module Base + 0x001C = PWMDTY0, 0x001D = PWMDTY1, 0x001E = PWMDTY2, 0x001F = PWMDTY3
Module Base + 0x0020 = PWMDTY4, 0x0021 = PWMDTY5, 0x0022 = PWMDTY6, 0x0023 = PWMDTY7

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 22-14. PWM Channel Duty Registers (PWMDTYx)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Read: Anytime

Write: Anytime

Table E-1. GDU Electrical Characteristics (Junction Temperature From –40°C To +175°C)

4.85V<=VDDX,VDDA<=5.15V						
33	Current Sense Amplifier output voltage range	V_{CSAout}	0	—	VDDA	V
34	Current Sense Amplifier open loop gain	AV_{CSA}	—	100000	—	—
35	Current Sense Amplifier common mode rejection ratio	$CMRR_{CSA}$	—	400	—	—
36	Current Sense Amplifier input offset	V_{CSAoff}	-15	—	15	mV
37	Max effective Current Sense Amplifier output resistance [0.1V .. VDDA - 0.2V]	R_{CSAout}	—	—	2	Ω
38	Min Current Sense Amplifier output current [0.1V .. VDDA - 0.2V](15)	I_{CSAout}	-750	—	750	μA
39	Current Sense Amplifier large signal settling time	t_{cslsst}	—	2.9	—	μs
40	Current Sense Amplifier unity gain bandwidth	GBW	—	1.9	—	MHz
41	Current Sense Amplifier input resistance	(16)	—	—	—	—
42	Over Current Comparator filter time constant(17)	τ_{OCC}	3	5	10	μs
43	Over Current Comparator threshold tolerance	V_{OCCtt}	-75	—	75	mV
44	HD input current when GDU is enabled	I_{HD}	—	130μ + V_{HD}/63K	—	A
45	VLS regulator minimum RDSon (VSUP >= 6V)	R_{VLSmin}	—	—	40	Ω
46	VCP to VBSx switch resistance	R_{VCPVBS}	—	600	1000	Ω
47	VBSx current whilst high side inactive	I_{VBS}	—	—	310	μA
48a	Desaturation comparator filter time constant fast (GDU V6 GDSFHS/GDSFLS=0) (GDU V4 high side) (GDU V4 low side on all mask sets except 3N95G)	τ_{desatf}	90	—	250	ns
48b	Desaturation comparator filter time constant slow (GDU V6 GDSFHS/GDSFLS=1) (GDU V4 mask set 3N95G low side)	τ_{desats}	240	—	670	ns
49a	LS desaturation comparator level, GDUV6, GDSLLS = 000 (18)	$V_{desatls}$	0.23	0.35	0.46	V
49b	LS desaturation comparator level, GDUV6, GDSLLS = 001(18)	$V_{desatls}$	0.355	0.5	0.645	V
49c	LS desaturation comparator level, GDUV6, GDSLLS = 010(18)	$V_{desatls}$	0.46	0.65	0.84	V
49d	LS desaturation comparator level, GDUV6, GDSLLS = 011(18)	$V_{desatls}$	0.575	0.8	1.035	V
49e	LS desaturation comparator level, GDUV6, GDSLLS = 100(18)	$V_{desatls}$	0.69	0.95	1.23	V
49f	LS desaturation comparator level, GDUV6, GDSLLS = 101(18)	$V_{desatls}$	0.81	1.1	1.41	V
49g	LS desaturation comparator level, GDUV6, GDSLLS = 110(18)	$V_{desatls}$	0.925	1.25	1.605	V
49h	LS desaturation comparator level, GDUV6, GDSLLS = 111(18)	$V_{desatls}$	1.03	1.4	1.81	V
50a	HS desaturation comparator level, GDUV6, GDSLHS = 000	$V_{desaths}$	V_{HD}-0.23	V_{HD}-0.35	V_{HD}-0.46	V
50b	HS desaturation comparator level, GDUV6, GDSLHS = 001	$V_{desaths}$	V_{HD}-0.355	V_{HD}-0.5	V_{HD}-0.645	V
50c	HS desaturation comparator level, GDUV6, GDSLHS = 010	$V_{desaths}$	V_{HD}-0.46	V_{HD}-0.65	V_{HD}-0.84	V
50d	HS desaturation comparator level, GDUV6, GDSLHS = 011	$V_{desaths}$	V_{HD}-0.575	V_{HD}-0.8	V_{HD}-1.035	V
50e	HS desaturation comparator level, GDUV6, GDSLHS = 100	$V_{desaths}$	V_{HD}-0.69	V_{HD}-0.95	V_{HD}-1.23	V
50f	HS desaturation comparator level, GDUV6, GDSLHS = 101	$V_{desaths}$	V_{HD}-0.81	V_{HD}-1.1	V_{HD}-1.41	V
50g	HS desaturation comparator level, GDUV6, GDSLHS = 110	$V_{desaths}$	V_{HD}-0.925	V_{HD}-1.25	V_{HD}-1.605	V
50h	HS desaturation comparator level, GDUV6, GDSLHS = 111	$V_{desaths}$	V_{HD}-1.03	V_{HD}-1.4	V_{HD}-1.81	V

1. Without using the boost option. The minimum level can be relaxed when the boost option is used. The lower limit is sensed on VLS, the upper limit is sensed on HD.
2. Without using the boost option. The minimum level can be relaxed when the boost option is used. The lower limit is sensed on VLS, the upper limit is sensed on HD. Operation beyond 20V is limited to 1 hour over lifetime of the device