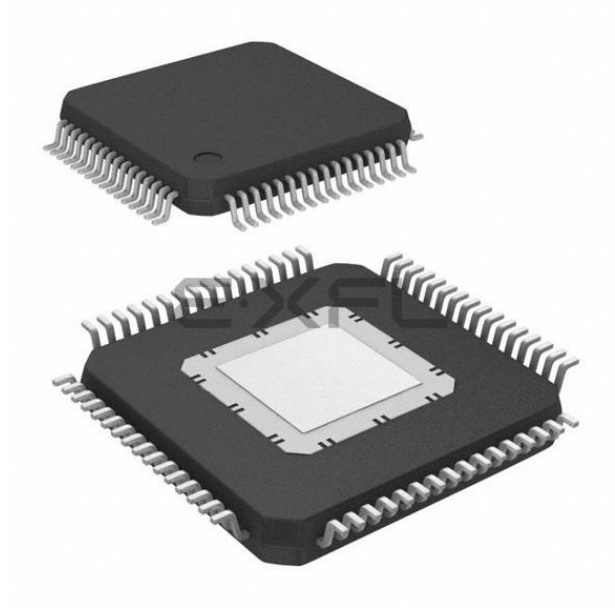

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Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
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Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f2mkh

1.7.2.16 Timer IOC0_[3:0] Signals

The signals IOC0_[3:0] are associated with the input capture or output compare functionality of the timer (TIM0) module.

1.7.2.17 Timer IOC1_[1:0] Signals (ZVMC256 only)

The signals IOC1_[1:0] are associated with the input capture or output compare functionality of the timer (TIM1) module.

1.7.2.18 PWM1_[5:0] Signals

The signals PWM1_[5:0] are associated with the PMF module digital channel outputs.

1.7.2.19 PWM0_[7,5,3,1] Signals (ZVMC256 only)

The PWM0 signals are associated with the PWM0 module digital channel outputs.

1.7.2.20 PTU Signals

1.7.2.20.1 PTUT[1:0] Signals

These signals are the PTU trigger output signals. These signals are routed to pins for debugging purposes.

1.7.2.20.2 PTURE Signal

This signal is the PTU reload enable output signal. This signal is routed to a pin for debugging purposes.

1.7.2.21 Interrupt Signals — $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$

$\overline{\text{IRQ}}$ is a maskable level or falling edge sensitive input. $\overline{\text{XIRQ}}$ is a non-maskable level-sensitive interrupt.

1.7.2.22 Oscillator and Clock Signals

1.7.2.22.1 Oscillator Pins — EXTAL and XTAL

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the internal PLLCLK, independent of EXTAL and XTAL. XTAL is the oscillator output.

1.7.2.22.2 ECLK

This signal is associated with the output of the bus clock (ECLK).

NOTE

This feature is only intended for debug purposes at room temperature.
It must not be used for clocking external devices in an application.

Table 5-5. BDCCSRH Field Descriptions

Field	Description
7 ENBDC	**Enable BDC** — This bit controls whether the BDC is enabled or disabled. When enabled, active BDM can be entered and non-intrusive commands can be carried out. When disabled, active BDM is not possible and the valid command set is restricted. Further information is provided in Table 5-7. 0 BDC disabled 1 BDC enabled **Note:** ENBDC is set out of reset in special single chip mode.
6 BDMACT	**BDM Active Status** — This bit becomes set upon entering active BDM. BDMACT is cleared as part of the active BDM exit sequence. 0 BDM not active 1 BDM active **Note:** BDMACT is set out of reset in special single chip mode.
5 BDCCIS	**BDC Continue In Stop** — If ENBDC is set then BDCCIS selects the type of BDC operation in stop mode (as shown in Table 5-3). If ENBDC is clear, then the BDC has no effect on stop mode and no BDC communication is possible.If ACK pulse handshaking is enabled, then the first ACK pulse following stop mode entry is a long ACK. This bit cannot be written when the device is in stop mode. 0 Only the BDCCLK clock continues in stop mode 1 All clocks continue in stop mode
3 STEAL	**Steal enabled with ACK**— This bit forces immediate internal accesses with the ACK handshaking protocol enabled. If ACK handshaking is disabled then BDC accesses steal the next bus cycle. 0 If ACK is enabled then BDC accesses await a free cycle, with a timeout of 512 cycles 1 If ACK is enabled then BDC accesses are carried out in the next bus cycle
2 CLKSW	**Clock Switch** — The CLKSW bit controls the BDCSI clock source. This bit is initialized to “0” by each reset and can be written to “1”. Once it has been set, it can only be cleared by a reset. When setting CLKSW a minimum delay of 150 cycles at the initial clock speed must elapse before the next command can be sent. This guarantees that the start of the next BDC command uses the new clock for timing subsequent BDC communications. 0 BDCCLK used as BDCSI clock source 1 Device fast clock used as BDCSI clock source **Note:** Refer to the device specification to determine which clock connects to the BDCCLK and fast clock inputs.
1 UNSEC	**Unsecure** — If the device is unsecure, the UNSEC bit is set automatically. 0 Device is secure. 1 Device is unsecure. **Note:** When UNSEC is set, the device is unsecure and the state of the secure bits in the on-chip Flash EEPROM can be changed.
0 ERASE	**Erase Flash** — This bit can only be set by the dedicated ERASE_FLASH command. ERASE is unaffected by write accesses to BDCCSR. ERASE is cleared either when the mass erase sequence is completed, independent of the actual status of the flash array or by a soft reset. Reading this bit indicates the status of the requested mass erase sequence. 0 No flash mass erase sequence pending completion 1 Flash mass erase sequence pending completion.

5.4.5.2.1 FILL_MEM and DUMP_MEM Increments and Alignment

FILL_MEM and DUMP_MEM increment the previously accessed address by the previous access size to calculate the address of the current access. On misaligned longword accesses, the address bits [1:0] are forced to zero, therefore the following FILL_MEM or DUMP_MEM increment to the first address in the next 4-byte field. This is shown in Table 5-11, the address of the first DUMP_MEM.32 following READ_MEM.32 being calculated from 0x004000+4.

When misaligned word accesses are realigned, then the original address (not the realigned address) is incremented for the following FILL_MEM, DUMP_MEM command.

Misaligned word accesses can cause the same locations to be read twice as shown in rows 6 and 7. The hardware ensures alignment at an attempted misaligned word access across a 4-byte boundary, as shown in row 7. The following word access in row 8 continues from the realigned address of row 7.

Table 5-11. Consecutive Accesses With Variable Size

Row	Command	Address	Address[1:0]	00	01	10	11
1	READ_MEM.32	0x004003	11	Accessed	Accessed	Accessed	Accessed
2	DUMP_MEM.32	0x004004	00	Accessed	Accessed	Accessed	Accessed
3	DUMP_MEM.16	0x004008	00	Accessed	Accessed		
4	DUMP_MEM.16	0x00400A	10			Accessed	Accessed
5	DUMP_MEM.08	0x00400C	00	Accessed			
6	DUMP_MEM.16	0x00400D	01		Accessed	Accessed	
7	DUMP_MEM.16	0x00400E	10			Accessed	Accessed
8	DUMP_MEM.16	0x004010	01	Accessed	Accessed		

5.4.5.2.2 READ_SAME Effects Of Variable Access Size

READ_SAME uses the unadjusted address given in the previous READ_MEM command as a base address for subsequent READ_SAME commands. When the READ_MEM and READ_SAME size parameters differ then READ_SAME uses the original base address buts aligns 32-bit and 16-bit accesses, where those accesses would otherwise cross the aligned 4-byte boundary. Table 5-12 shows some examples of this.

Table 5-12. Consecutive READ_SAME Accesses With Variable Size

Row	Command	Base Address	00	01	10	11
1	READ_MEM.32	0x004003	Accessed	Accessed	Accessed	Accessed
2	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
3	READ_SAME.16	—			Accessed	Accessed
4	READ_SAME.08	—				Accessed
5	READ_MEM.08	0x004000	Accessed			
6	READ_SAME.08	—	Accessed			
7	READ_SAME.16	—	Accessed	Accessed		
8	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
9	READ_MEM.08	0x004002			Accessed	

6.4.5 Trace Buffer Operation

The trace buffer is a 64 lines deep by 64-bits wide RAM array. If the TSOURCE bit is set the DBG module can store trace information in the RAM array in a circular buffer format. Data is stored in mode dependent formats, as described in the following sections. After each trace buffer entry, the counter register DBGCNT is incremented. Trace buffer rollover is possible when configured for End- or Mid-Aligned tracing, such that older entries are replaced by newer entries. Tracing of CPU activity is disabled when the BDC is active.

The RAM array can be accessed through the register DBGTB using 16-bit wide word accesses. After each read, the internal RAM pointer is incremented so that the next read will receive fresh information. Reading the trace buffer whilst the DBG is armed returns invalid data and the trace buffer pointer is not incremented.

In Detail mode the address range for CPU access tracing can be limited to a range specified by the TRANGE bits in DBGTCRH. This function uses comparators C and D to define an address range inside which accesses should be traced. Thus traced accesses can be restricted, for example, to particular register or RAM range accesses.

The external event pin can be configured to force trace buffer entries in Normal or Loop1 trace modes. All tracing modes support trace buffer gating. In Pure PC and Detail modes external events do not force trace buffer entries.

If the external event pin is configured to gate trace buffer entries then any trace mode is valid.

6.4.5.1 Trace Trigger Alignment

Using the TALIGN bits (see Section 6.3.2.3”) it is possible to align the trigger with the end, the middle, or the beginning of a tracing session.

If End or Mid-Alignment is selected, tracing begins when the ARM bit in DBGC1 is set and State1 is entered. The transition to Final State if End-Alignment is selected, ends the tracing session. The transition to Final State if Mid-Alignment is selected signals that another 32 lines are traced before ending the tracing session. Tracing with Begin-Alignment starts at the trigger and ends when the trace buffer is full.

Table 6-47. Tracing Alignment

TALIGN	Tracing Begin	Tracing End
00	On arming	At trigger
01	At trigger	When trace buffer is full
10	On arming	When 32 trace buffer lines have been filled after trigger
11	Reserved	

6.4.5.1.1 Storing with Begin-Alignment

Storing with Begin-Alignment, data is not stored in the trace buffer until the Final State is entered. Once the trigger condition is met the DBG module remains armed until 64 lines are stored in the trace buffer.

7.2.2.5 ECC Debug Data (ECCDDH, ECCDDL)

Module Base + 0x000C — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	DDATA[15:8]							
Reset	0	0	0	0	0	0	0	0

Module Base + 0x000D — Access: User read/write

	7	6	5	4	3	2	1	0
R W	DDATA[7:0]							
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-6. ECC Debug Data (ECCDDH, ECCDDL)

1. Read: Anytime
   Write: Anytime

Table 7-6. ECCDD Register Field Descriptions

Field	Description
DDATA [23:0]	ECC Debug Raw Data — This register contains the raw data which will be written into the system memory during a debug write command or the read data from the debug read command.

7.2.2.6 ECC Debug ECC (ECCDE)

Module Base + 0x000E — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	DECC[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime

Figure 7-7. ECC Debug ECC (ECCDE)

Table 7-7. ECCDE Field Description

Field	Description
5:0 DECC[5:0]	ECC Debug ECC — This register contains the raw ECC value which will be written into the system memory during a debug write command or the ECC read value from the debug read command.

Several examples of PLL divider settings are shown in Table 8-34. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 8-34. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz
off	$00	1MHz	00	$18	50MHz	01	$00	50MHz	25MHz
4MHz	$00	4MHz	01	$05	48MHz	00	$00	48MHz	24MHz

The phase detector inside the PLL compares the feedback clock (FBCLK = VCOCLK/(SYNDIV+1)) with the reference clock (REFCLK = (IRC1M or OSCCLK)/(REFDIV+1)). Correction pulses are generated based on the phase difference between the two signals. The loop filter alters the DC voltage on the internal filter capacitor, based on the width and direction of the correction pulse which leads to a higher or lower VCO frequency.

The user must select the range of the REFCLK frequency (REFFRQ[1:0] bits) and the range of the VCOCLK frequency (VCOFRQ[1:0] bits) to ensure that the correct PLL loop bandwidth is set.

The lock detector compares the frequencies of the FBCLK and the REFCLK. Therefore the speed of the lock detector is directly proportional to the reference clock frequency. The circuit determines the lock condition based on this comparison. So e.g. a failure in the reference clock will cause the PLL not to lock.

If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and for instance check the LOCK bit. If interrupt requests are disabled, software can poll the LOCK bit continuously (during PLL start-up) or at periodic intervals. In either case, only when the LOCK bit is set, the VCOCLK will have stabilized to the programmed frequency.

- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within the tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of the tolerance, Δ_{unl}.

Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.In case of loss of reference clock (e.g. IRCCLK) the PLL will not lock or if already locked, then it will unlock. The frequency of the VCOCLK will be very low and will depend on the value of the VCOFRQ[1:0] bits.

9.5 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B_LBA.

9.5.1 Module Memory Map

Figure 9-3 gives an overview of all ADC12B_LBA registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ADCCTL_0	R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
		W								
0x0001	ADCCTL_1	R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
		W								
0x0002	ADCSTS	R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
		W								
0x0003	ADCTIM	R	0	PRS[6:0]						
		W								
0x0004	ADCFMT	R	DJM	0	0	0	0	SRES[2:0]		
		W								
0x0005	ADCFLWCTL	R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
		W								
0x0006	ADCEIE	R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
		W								
0x0007	ADCIE	R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
		W								
0x0008	ADCEiF	R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
		W								
0x0009	ADCIF	R	SEQAD_IF	CONIF_OIF	Reserved	0	0	0	0	0
		W								
0x000A	ADCCONIE_0	R	CON_IE[15:8]							
		W								
0x000B	ADCCONIE_1	R	CON_IE[7:1]							EOL_IE
		W								
0x000C	ADCCONIF_0	R	CON_IF[15:8]							
		W								
0x000D	ADCCONIF_1	R	CON_IF[7:1]							EOL_IF
		W								
0x000E	ADCIMDRI_0	R	CSL_IMD	RVL_IMD	0	0	0	0	0	0
		W								
0x000F	ADCIMDRI_1	R	0	0	RIDX_IMD[5:0]					
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 1 of 3)

9.5.2.24 ADC Command and Result Offset Register 1 (ADCCROFF1)

It is important to note that these bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).

Module Base + 0x0025

	7	6	5	4	3	2	1	0
R	0	CMDRES_OFF1[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-27. ADC Command and Result Offset Register 1 (ADCCROFF1)

Read: Anytime

Write: These bits are writable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-32. ADCCROFF1 Field Descriptions

Field	Description
6-0 CMDRES_OFF1[6:0]	**ADC Result Address Offset Value** — These bits represent the conversion command and result offset value relative to the conversion command base pointer address and result base pointer address in the memory map to refer to CSL_1 and RVL_1. It is used to calculate the address inside the system RAM to which the result at the end of the current conversion is stored to and the area (RAM or NVM) from which the conversion commands are loaded from. These bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).,These bits can only be modified if bit ADC_EN is clear. See also Section 9.6.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) and Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs) for more details.

13.3.3.1.2 IDR0–IDR3 for Standard Identifier Mapping

Module Base + 0x00X0

	7	6	5	4	3	2	1	0
R W	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
Reset:	x	x	x	x	x	x	x	x

Figure 13-30. Identifier Register 0 — Standard Mapping

Table 13-30. IDR0 Register Field Descriptions — Standard

Field	Description
7-0 ID[10:3]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 13-31.

Module Base + 0x00X1

	7	6	5	4	3	2	1	0
R W	ID2	ID1	ID0	RTR	IDE (=0)			
Reset:	x	x	x	x	x	x	x	x

= Unused; always read ‘x’

Figure 13-31. Identifier Register 1 — Standard Mapping

Table 13-31. IDR1 Register Field Descriptions

Field	Description
7-5 ID[2:0]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 13-30.
4 RTR	**Remote Transmission Request** — This flag reflects the status of the Remote Transmission Request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)

16.3.2.7 SCI Status Register 1 (SCISR1)

The SCISR1 and SCISR2 registers provides inputs to the MCU for generation of SCI interrupts. Also, these registers can be polled by the MCU to check the status of these bits. The flag-clearing procedures require that the status register be read followed by a read or write to the SCI data register.It is permissible to execute other instructions between the two steps as long as it does not compromise the handling of I/O, but the order of operations is important for flag clearing.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
W								
Reset	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-10. SCI Status Register 1 (SCISR1)

Read: Anytime

Write: Has no meaning or effect

Table 16-11. SCISR1 Field Descriptions

Field	Description
7 TDRE	**Transmit Data Register Empty Flag** — TDRE is set when the transmit shift register receives a byte from the SCI data register. When TDRE is 1, the transmit data register (SCIDRH/L) is empty and can receive a new value to transmit.Clear TDRE by reading SCI status register 1 (SCISR1), with TDRE set and then writing to SCI data register low (SCIDRL). 0 No byte transferred to transmit shift register 1 Byte transferred to transmit shift register; transmit data register empty
6 TC	**Transmit Complete Flag** — TC is set low when there is a transmission in progress or when a preamble or break character is loaded. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted.When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL). TC is cleared automatically when data, preamble, or break is queued and ready to be sent. TC is cleared in the event of a simultaneous set and clear of the TC flag (transmission not complete). 0 Transmission in progress 1 No transmission in progress
5 RDRF	**Receive Data Register Full Flag** — RDRF is set when the data in the receive shift register transfers to the SCI data register. Clear RDRF by reading SCI status register 1 (SCISR1) with RDRF set and then reading SCI data register low (SCIDRL). 0 Data not available in SCI data register 1 Received data available in SCI data register
4 IDLE	**Idle Line Flag** — IDLE is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M =1) appear on the receiver input. Once the IDLE flag is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag.Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL). 0 Receiver input is either active now or has never become active since the IDLE flag was last cleared 1 Receiver input has become idle **Note:** When the receiver wakeup bit (RWU) is set, an idle line condition does not set the IDLE flag.

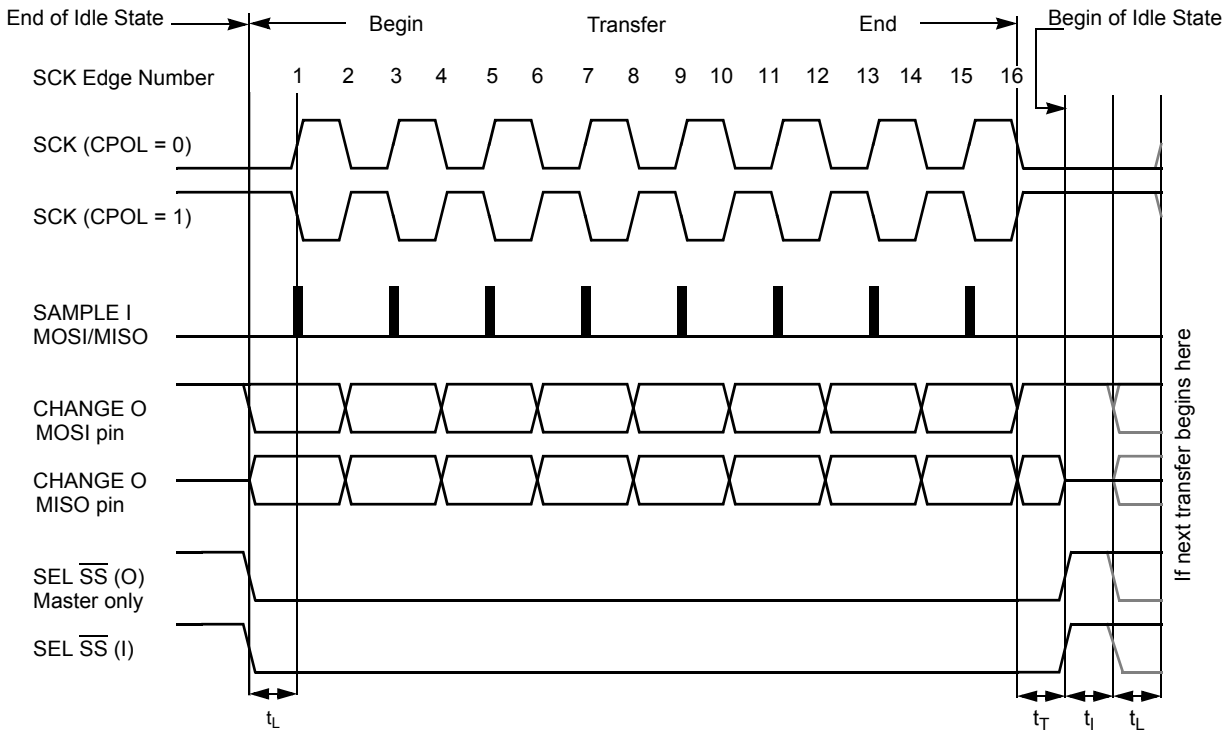
Table 17-4. SPICR2 Field Descriptions

Field	Description
6 XFRW	**Transfer Width —** This bit is used for selecting the data transfer width. If 8-bit transfer width is selected, SPIDRL becomes the dedicated data register and SPIDRH is unused. If 16-bit transfer width is selected, SPIDRH and SPIDRL form a 16-bit data register. Please refer to Section 17.3.2.4, “SPI Status Register (SPISR) for information about transmit/receive data handling and the interrupt flag clearing mechanism. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 8-bit Transfer Width (n = 8)(1) 1 16-bit Transfer Width (n = 16)[1]
4 MODFEN	**Mode Fault Enable Bit** — This bit allows the MODF failure to be detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration, refer to Table 17-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 $\overline{SS}$ port pin is not used by the SPI. 1 $\overline{SS}$ port pin with MODF feature.
3 BIDIROE	**Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode, this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state. 0 Output buffer disabled. 1 Output buffer enabled.
1 SPISWAI	**SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 SPI clock operates normally in wait mode. 1 Stop SPI clock generation when in wait mode.
0 SPC0	**Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 17-5. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

1. n is used later in this document as a placeholder for the selected transfer width.

Table 17-5. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	



t_L = Minimum leading time before the first SCK edge

t_T = Minimum trailing time after the last SCK edge

t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time)

t_L, t_T, and t_I are guaranteed for the master mode and required for the slave mode.

Figure 17-12. SPI Clock Format 0 (CPHA = 0), with 8-bit Transfer Width selected (XFRW = 0)

Table 18-24. Fault Protection Features Summary

Priority	Condition	GSUF	GHHDF	GOCIF0	GOCIF1	GLVLSF	GDHSIF [2:0]	GDLSIF [2:0]		HS2	HS1	HS0	LS2	LS1	LS0
low	normal operation,no error condition, FET pre-driver driven by PMF module	0	0	0	0	0	000	000		PWM [4]	PWM [2]	PWM [0]	PWM [5]	PWM [3]	PWM [1]
	startup condition after reset deassert, no error condition	1	0	0	0	0	000	000		off	off	off	on/off (1)	on/off	on/off
	overvoltage on HD pin GOCA1=0	x	1	0	0	0	000	000		off	off	off	on	on	on
	overcurrent condition comparator 0 GOCA0=0	x	x	1	x	0	000	000		off	off	off	on	on	on
	overcurrent condition comparator 1 GOCA1=0	x	x	x	1	0	000	000		off	off	off	on	on	on
	undervoltage condition on VLS_OUT pin	x	x	x	x	1	000	000		off	off	off	off	off	off
	overcurrent condition comparator 0 GOCA0=1	x	x	1	x	x	000	000		off	off	off	off	off	off
	overcurrent condition comparator 1 GOCA1=1	x	x	x	1	x	000	000		off	off	off	off	off	off
	desaturation error condition on high-side FET pre-drivers	x	x	x	x	x	001	000		PWM [4]	PWM [2]	off	PWM [5]	PWM [3]	PWM [1]
		x	x	x	x	x	010	000		PWM [4]	off	PWM [0]	PWM [5]	PWM [3]	PWM [1]
		x	x	x	x	x	100	000		off	PWM [2]	PWM [0]	PWM [5]	PWM [3]	PWM [1]
	desaturation error condition on low-side FET pre-drivers	x	x	x	x	x	000	001		PWM [4]	PWM [2]	PWM [0]	PWM [5]	PWM [3]	off
		x	x	x	x	x	000	010		PWM [4]	PWM [2]	PWM [0]	PWM [5]	off	PWM [1]
		x	x	x	x	x	000	100		PWM [4]	PWM [2]	PWM [0]	off	PWM [3]	PWM [1]
high	overvoltage on HD pin GOCA1=1	x	1	x	x	x	xxx	xxx		off	off	off	off	off	off

1. Startup condition of the low-side drivers LS[2:0] on GDUV6 depends on the flash option bit. On GDUV4 and V5 the low-side drivers are on out of reset.

Table 20-9. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 20-10.
5–2 RNV[5:2]	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 20-11. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 20-10. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED(1)
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

Table 20-11. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED(1)
10	UNSECURED
11	SECURED

1. Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 20.5.

20.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to indicate the amount of parameters loaded into the FCCOB registers for Flash memory operations.

Offset Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CCOBIX[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

20.4.7.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 20-48. Erase Flash Block Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x09	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 20-49. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 20-50. Erase P-Flash Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0A	Global address [23:16] to identify P-Flash block to be erased
FCCOB1	Global address [15:0] anywhere within the sector to be erased. Refer to Section 20.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 22-4. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7-0 PCLK[7:0]	Pulse Width Channel 7-0 Clock Select 0 Clock A or B is the clock source for PWM channel 7-0, as shown in Table 22-5 and Table 22-6. 1 Clock SA or SB is the clock source for PWM channel 7-0, as shown in Table 22-5 and Table 22-6.

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK and PCLKABx bits in PWMCLKAB (see Section 22.3.2.7, “PWM Clock A/B Select Register (PWMCLKAB)). For Channel 0, 1, 4, 5, the selection is shown in Table 22-5; For Channel 2, 3, 6, 7, the selection is shown in Table 22-6.

Table 22-5. PWM Channel 0, 1, 4, 5 Clock Source Selection

PCLKAB[0,1,4,5]	PCLK[0,1,4,5]	Clock Source Selection
0	0	Clock A
0	1	Clock SA
1	0	Clock B
1	1	Clock SB

Table 22-6. PWM Channel 2, 3, 6, 7 Clock Source Selection

PCLKAB[2,3,6,7]	PCLK[2,3,6,7]	Clock Source Selection
0	0	Clock B
0	1	Clock SB
1	0	Clock A
1	1	Clock SA

22.3.2.4 PWM Prescale Clock Select Register (PWMPRCLK)

This register selects the prescale clock source for clocks A and B independently.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 22-6. PWM Prescale Clock Select Register (PWMPRCLK)

Read: Anytime

Write: Anytime

NOTE

PCKB2–0 and PCKA2–0 register bits can be written anytime. If the clock pre-scale is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table C-3. ADC Conversion Performance 5 V range (Junction Temperature From –40°C To +150°C)

Supply voltage 4.5 V < V_{DDA} < 5.5 V, 4.5V < V_{REF} < 5.5 V. (V_{REF}= V_{RH} - V_{RL}). f_{ADCCLK} = 8.0 MHz
The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
1		Resolution (V_{REF} = 5.12V)	12-Bit	LSB	—	1.25	—	mV
2		Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3		Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4		Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5		Resolution (V_{REF} = 5.12V)	10-Bit	LSB	—	5	—	mV
6		Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7		Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8		Absolute Error	10-Bit	AE	-3	±2	3	counts
9		Resolution (V_{REF} = 5.12V)	8-Bit	LSB	—	20	—	mV
10		Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11		Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12		Absolute Error	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.
2. These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table C-4. ADC Conversion Performance 5 V range (Junction Temperature From 150°C To +175°C)

Supply voltage 4.5 V < V_{DDA} < 5.5 V, 4.5V < V_{REF} < 5.5 V. (V_{REF}= V_{RH} - V_{RL}). f_{ADCCLK} = 8.0 MHz
The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
1		Resolution (V_{REF} = 5.12V)	12-Bit	LSB	—	1.25	—	mV
2		Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3		Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4		Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5		Resolution (V_{REF} = 5.12V)	10-Bit	LSB	—	5	—	mV
6		Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7		Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8		Absolute Error	10-Bit	AE	-3	±2	3	counts
9		Resolution (V_{REF} = 5.12V)	8-Bit	LSB	—	20	—	mV
10		Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11		Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12		Absolute Error	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2. These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table F-1. FTMRZ128K512 NVM Timing Characteristics (Junction Temperature From –40°C To +150°C)

Derivatives ZVML128, ZVMC128, ZVML64, ZVMC64, ZVML32									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	50	50	50	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	33760	t_{RD1ALL}	0.68	0.68	1.35	67.52	ms
4	Erase Verify Block (Pflash)	0	33320	t_{RD1BLK_P}	0.67	0.67	1.33	66.64	ms
5	Erase Verify Block (EEPROM)	0	823	t_{RD1BLK_D}	0.02	0.02	0.03	1.65	ms
6	Erase Verify P-Flash Section	0	505	t_{RD1SEC}	0.01	0.01	0.04	2.02	ms
7	Read Once	0	481	t_{RDONCE}	9.62	9.62	9.62	481.00	us
8	Program P-Flash (4 Word)	164	3077	t_{PGM_4}	0.22	0.23	0.41	12.51	ms
9	Program Once	164	3054	$t_{PGMONCE}$	0.22	0.23	0.23	3.26	ms
10	Erase All Blocks	100066	34223	t_{ERSALL}	95.99	100.75	101.43	193.53	ms
11	Erase Flash Block (Pflash)	100060	33681	t_{ERSBLK_P}	95.97	100.73	101.41	192.44	ms
12	Erase Flash Block (EEPROM)	100060	1154	t_{ERSBLK_D}	95.32	100.08	100.11	127.38	ms
13	Erase P-Flash Sector	20015	914	t_{ERSPG}	19.08	20.03	20.05	26.85	ms
14	Unsecure Flash	100066	34288	t_{UNSECU}	95.99	100.75	101.44	193.66	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	9.86	9.86	9.86	493.00	us
16	Set User Margin Level	0	427	t_{MLOADU}	8.54	8.54	8.54	427.00	us
17	Set Factory Margin Level	0	436	t_{MLOADF}	8.72	8.72	8.72	436.00	us
18	Erase Verify EEPROM Sector	0	583	$t_{DRD1SEC}$	0.01	0.01	0.05	2.33	ms
19	Program EEPROM (1 Word)	68	1657	t_{DPGM_1}	0.10	0.10	0.20	6.71	ms
20	Program EEPROM (2 Word)	136	2660	t_{DPGM_2}	0.18	0.19	0.35	10.81	ms
21	Program EEPROM (3 Word)	204	3663	t_{DPGM_3}	0.27	0.28	0.50	14.91	ms
22	Program EEPROM (4 Word)	272	4666	t_{DPGM_4}	0.35	0.37	0.65	19.00	ms
23	Erase EEPROM Sector	5015	810	t_{DERSPG}	4.79	5.03	20.34	38.85	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	9.50	9.50	9.50	475.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

M.14 0x0640-0x067F ADC1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0640	ADC1CTL_0	R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
		W								
0x0641	ADC1CTL_1	R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
		W								
0x0642	ADC1STS	R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
		W								
0x0643	ADC1TIM	R	0	PRS[6:0]						
		W								
0x0644	ADC1FMT	R	DJM	0	0	0	0	SRES[2:0]		
		W								
0x0645	ADC1FLWCTL	R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
		W								
0x0646	ADC1EIE	R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
		W								
0x0647	ADC1IE	R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
		W								
0x0648	ADC1EiF	R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
		W								
0x0649	ADC1IF	R	SEQAD_IF	CONIF_OIF	Reserved	0	0	0	0	0
		W								
0x064A	ADC1CONIE_0	R	CON_IE[15:8]							
		W								
0x064B	ADC1CONIE_1	R	CON_IE[7:1]							EOL_IE
		W								
0x064C	ADC1CONIF_0	R	CON_IF[15:8]							
		W								
0x064D	ADC1CONIF_1	R	CON_IF[7:1]							EOL_IF
		W								
0x064E	ADC1IMDRI_0	R	CSL_IMD	RVL_IMD	0	0	0	0	0	0
0x064F	ADC1IMDRI_1	R	0	0	RIDX_IMD					
		W								
0x0650	ADC1EOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0651	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0652	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0653	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0654	ADC1CMD_0	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0655	ADC1CMD_1 (not ZVMC256)	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0655	ADC1CMD_1 (ZVMC256)	R	VRH_SEL[1:0]		CH_SEL[5:0]					
		W								

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