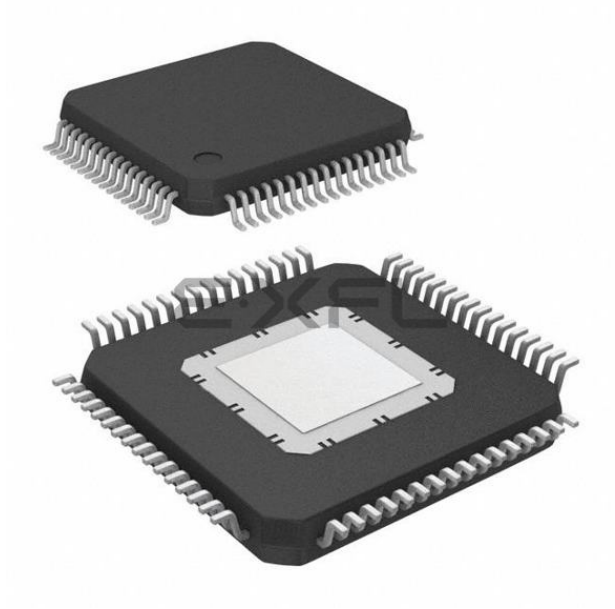


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f2wkh

Chapter 10
Supply Voltage Sensor - (BATSV3)

1.8.3 Device Level PMF Connectivity

Table 1-12. Mapping of PMF signals

PMF Connection	Usage
Channel0	High-Side Gate and Source Pins HG[0], HS[0]
Channel1	Low-Side Gate and Source Pins LG[0], LS[0]
Channel2	High-Side Gate and Source Pins HG[1], HS[1]
Channel3	Low-Side Gate and Source Pins LG[1], LS[1]
Channel4	High-Side Gate and Source Pins HG[2], HS[2]
Channel5	Low-Side Gate and Source Pins LG[2], LS[2]
FAULT5	External FAULT5 pin
FAULT4	HD Over voltage or GDU over current
FAULT3	VLS under voltage
FAULT2	GDU Desaturation[2] or GDU over current
FAULT1	GDU Desaturation[1] or GDU over current
FAULT0	GDU Desaturation[0] or GDU over current
IS2	GDU Phase Status[2]
IS1	GDU Phase Status[1]
IS0	GDU Phase Status[0]
async_event_edge_sel[1:0]	Tied to b11 (both edges active)

1.8.4 BDC Clock Source Connectivity

The BDC clock, BDCCLK, is mapped to the IRCCLK generated in the CPMU module.

The BDC clock, BDCFCLK is mapped to the device bus clock, generated in the CPMU module.

1.8.5 LINPHY Connectivity

The VLINSUP supply is device dependent.

On ZVML128, ZVMC128, ZVML64, ZVMC64 and ZVML32 devices with the maskset number 2N95G it is connected to VSUP

On all other devices it is connected to the device HD pin.

The LINPHY0 signals are mapped internally to SCI0. The receiver can be routed to TIM0 input capture channel3. These routing options are described in detail in the PIM section.

1.8.6 HVPHY Connectivity

The HVPHY signals (S12ZVM32 and S12ZVM16 derivatives only) are mapped internally to SCI0. The receiver can be routed to TIM0 input capture channel3.

reset sequence. The GSUF bit in the GDUF register is also loaded during the reset sequence. See Table 1-17, Table 1-18 and Table 1-19.

Table 1-17. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in CPMUCOP Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-18. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in CPMUCOP Register
1	0
0	1

Table 1-19. GDU Configuration

Mask Set	GSUF (GDUF[7]) Initialization	EPRES (GDUE[5]) Inclusion	GDUCTR1 Available bits	HD nominal over-voltage time constant
0N95G, 1N95G	1	Not usable	None	300ns
2N95G	0	Not usable	None	2.7us
3N95G	FOPT:NV[6]	Not included	GDUCTR1[0]	2.7us
0N14N	1	Not included	None	2.7us
1N14N	$\overline{\text{FOPT:NV[7]}}$ (1)	Not included	None	2.7us
0N00R,1N00R	$\overline{\text{FOPT:NV[7]}}$ (1)	Not included	GDUCTR1[7,6,0]	2.7us

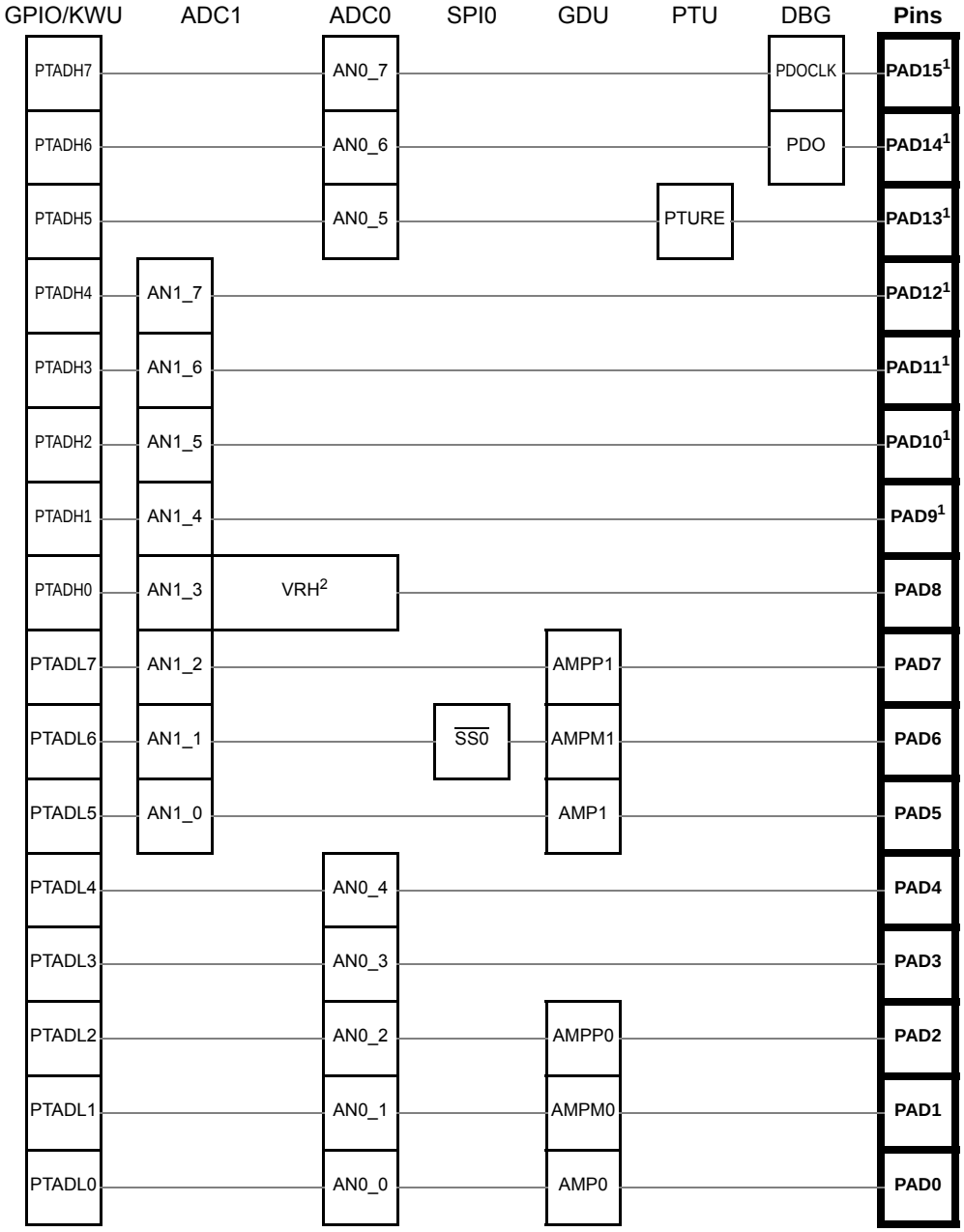
1. Note bit inversion

The EPRES bit was only included in early mask sets but was not usable. The implementation of GDUCTR1 register bits is also mask set dependent as shown in Table 1-19.

1.12.2 CPMU High Temperature Trimming

The value loaded from the flash into the CPMUHTTR register is a default value for the device family. There is no device specific trimming carried out during production. The specified V_{HT} value is a typical value that is part dependent and should thus be calibrated.

- Port AD



1. Only available for ZVMC256
2. Not available for ZVMC256

Most I/O pins can be configured by register bits to select data direction and to enable and select pullup or pulldown devices.

NOTE

This document shows the superset of all available features offered by the S12ZVM device family. Refer to the package and pinout section in the device overview for functions not available for a particular device or package option.

2.1.2 Features

The PIM includes these distinctive registers:

- Data registers and data direction registers for ports E, T, S, P and AD when used as general-purpose I/O
- Control registers to enable pull devices and select pullups/pulldowns on ports E, T, S, P and AD
- Control register to enable open-drain (wired-or) mode on port S
- Control register to enable digital input buffers on port AD and L[1]
- Interrupt enable register for pin interrupts and key-wakeup (KWU) on port S, P, AD, and L[1]
- Interrupt flag register for pin interrupts andkey-wakeup (KWU) on port S, P, AD, and L[1]
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Control register to enable ECLK output
- Routing registers to support signal relocation on external pins and control internal routings:
  - SPI0 to alternative pins
  - Various SCI0-LINPHY0 routing options supporting standalone use and conformance testing[2]
  - Various MSCAN0-CANPHY0 routing options for standalone use and conformance testing[1]
  - Internal RXD0 and RXD1 link to TIM0 input capture channel (IC0_3) for baud rate detection
  - Internal ACLK link to TIM0 input capture channel
  - 3 pin input mux to one TIM0 IC channel
  - 2 TIM0 channels to alternative pins[3]
  - PMF channels to GDU and/or pins

A standard port pin has the following minimum features:

- Input/output selection
- 5V output drive
- 5V digital and analog input
- Input with selectable pullup or pulldown device

Optional features supported on dedicated pins:

- Open drain for wired-or connections
- Interrupt input with glitch filtering
- High current drive strength from VDDX with over-current protection

1. Only available for ZVMC256
2. Only available for ZVML128, ZVML64, ZVML32, and ZVML31
3. Only available for S12ZVMC256, S12ZVML31, S12ZVM32, and S12ZVM16

Both interrupts are capable to wake-up the device from stop mode. Means for glitch filtering are not provided on these pins.

2.4.4 Pin interrupts and Key-Wakeup (KWU)

Ports AD, S, P and L offer pin interrupt and key-wakeup capability. The related interrupt enable (PIE) as well as the sensitivity to rising or falling edges (PPS) can be individually configured on per-pin basis. All bits/pins in a port share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag (PIF) and its corresponding port interrupt enable (PIE) are both set. The pin interrupt feature is also capable to wake up the CPU when it is in stop or wait mode (key-wakeup).

A digital filter on each pin prevents short pulses from generating an interrupt. A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level. Else the sampling logic is restarted.

In run and wait mode the filters are continuously clocked by the bus clock. Pulses with a duration of $t_{PULSE} < n_{P\_MASK}/f_{bus}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > n_{P\_PASS}/f_{bus}$ guarantee a pin interrupt.

In stop mode the filter clock is generated by an RC-oscillator. The minimum pulse length varies over process conditions, temperature and voltage (Figure 2-36). Pulses with a duration of $t_{PULSE} < t_{P\_MASK}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > t_{P\_PASS}$ guarantee a wakeup event.

Please refer to the appendix table “Pin Timing Characteristics” for pulse length limits.

To maximize current saving the RC oscillator is active only if the following condition is true on any individual pin:

individual pin:

Sample count <= 4 (at active or passive level) and interrupt enabled (PIE[x]=1) and interrupt flag not set (PIF[x]=0).

3.1.4 Modes of Operation

3.1.4.1 Chip configuration modes

The S12ZMMC determines the chip configuration mode of the device. It captures the state of the MODC pin at reset and provides the ability to switch from special-single chip mode to normal single chip-mode.

3.1.4.2 Power modes

The S12ZMMC module is only active in run and wait mode.There is no bus activity in stop mode.

3.1.5 Block Diagram

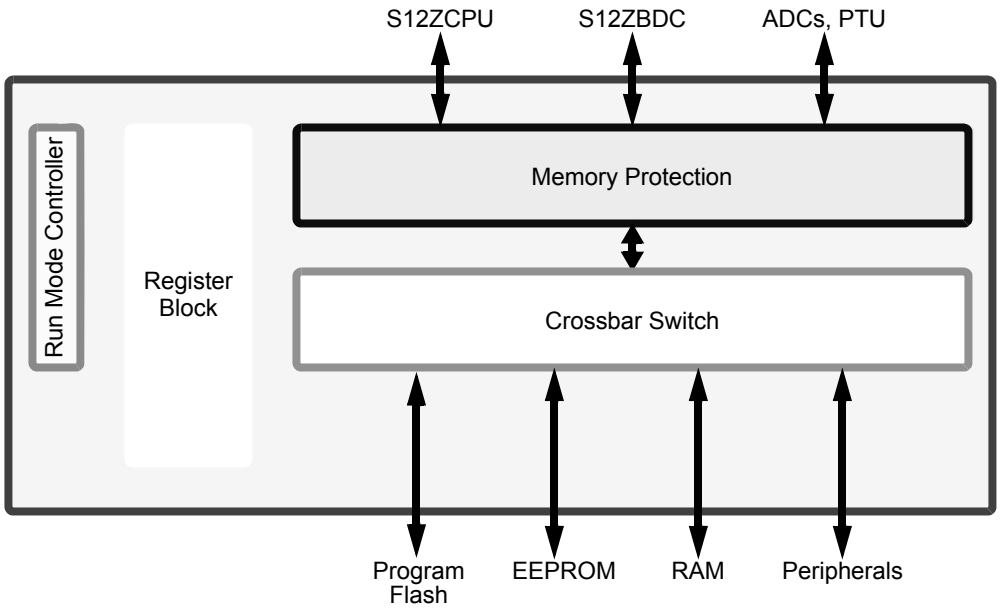


Figure 3-1. S12ZMMC Block Diagram

3.2 External Signal Description

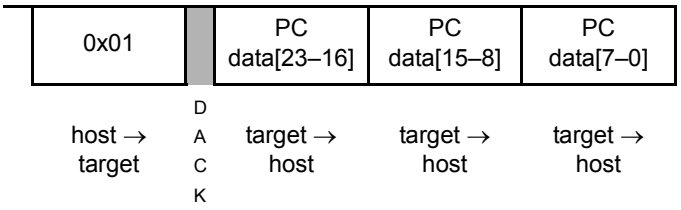
The S12ZMMC uses two external pins to determine the devices operating mode: RESET and MODC (Table 3-3)
See device overview for the mapping of these signals to device pins.

Table 3-3. External System Pins Associated With S12ZMMC

Pin Name	Description
$\overline{\text{RESET}}$	External reset signal. The $\overline{\text{RESET}}$ signal is active low.
MODC	This input is captured in bit MODC of the MODE register when the external $\overline{\text{RESET}}$ pin deasserts.

5.4.4.15 SYNC_PC

Sample current PC **Non-intrusive**



This command returns the 24-bit CPU PC value to the host. Unsuccessful SYNC_PC accesses return 0xEE for each byte. If enabled, an ACK pulse is driven before the data bytes are transmitted. The value of 0xEE is returned if a timeout occurs, whereby NORESP is set. This can occur if the CPU is executing the WAI instruction, or the STOP instruction with BDCCIS clear, or if a CPU access is delayed by EWAIT. If the CPU is executing the STOP instruction and BDCCIS is set, then SYNC_PC returns the PC address of the instruction following STOP in the code listing.

This command can be used to dynamically access the PC for performance monitoring as the execution of this command is considerably less intrusive to the real-time operation of an application than a BACKGROUND/read-PC/GO command sequence. Whilst the BDC is not in active BDM, SYNC_PC returns the PC address of the instruction currently being executed by the CPU. In active BDM, SYNC_PC returns the address of the next instruction to be executed on returning from active BDM. Thus following a write to the PC in active BDM, a SYNC_PC returns that written value.

5.4.4.16 WRITE_MEM.sz, WRITE_MEM.sz_WS

WRITE_MEM.sz

Write memory at the specified address **Non-intrusive**

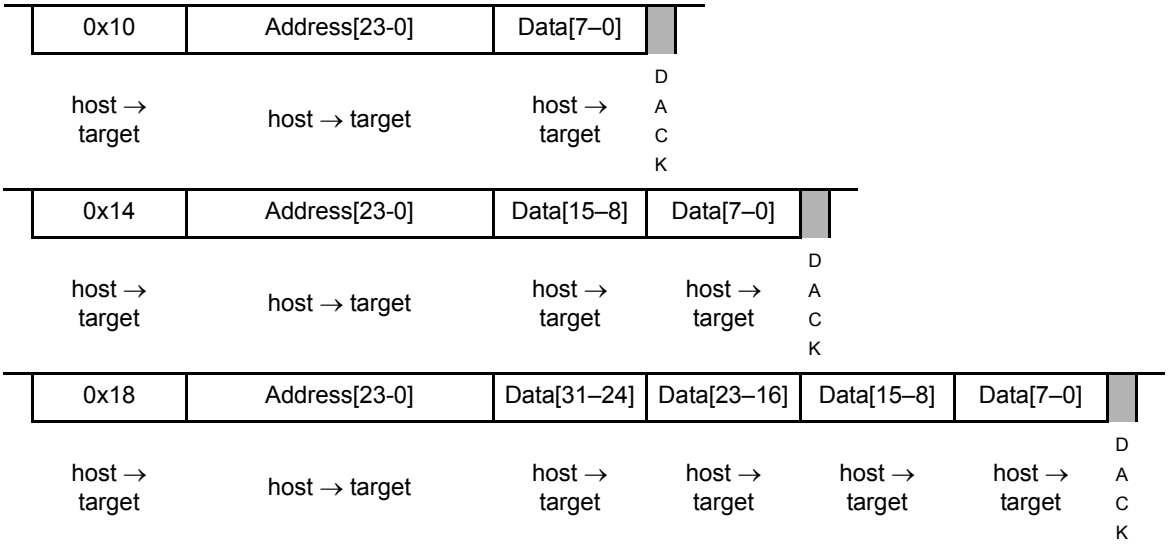


Table 6-32 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, as matches based on instructions reaching the execution stage are data independent.

Table 6-32. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

6.3.2.17 Debug Comparator B Address Register (DBGBAH, DBGBAM, DBGBAL)

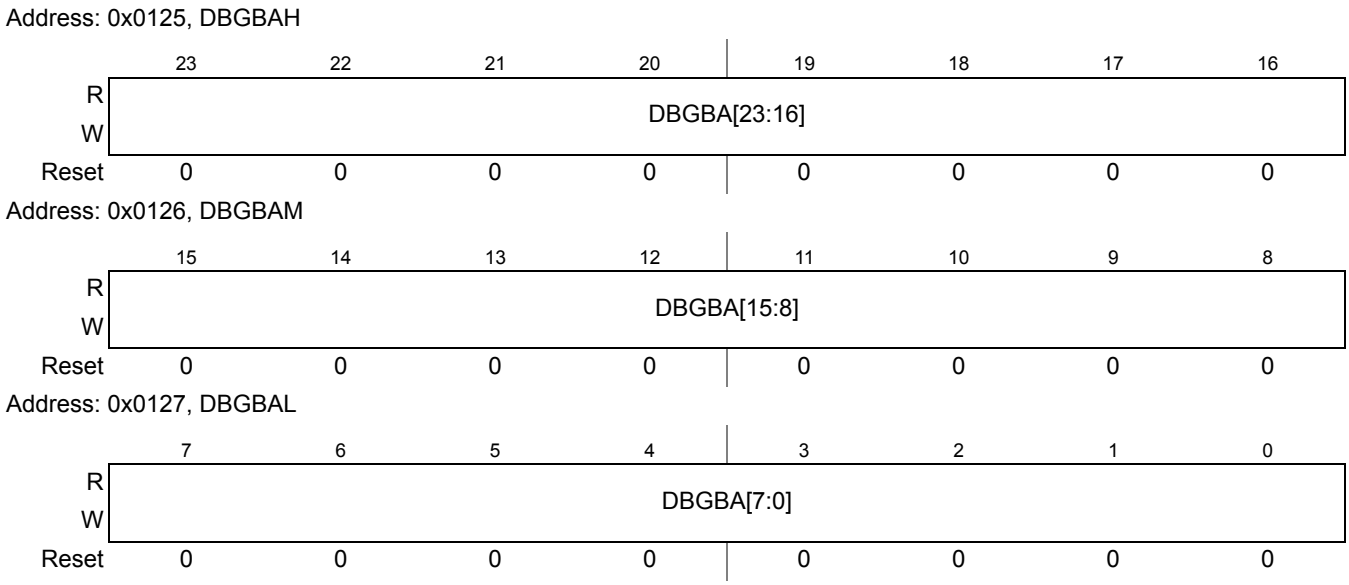


Figure 6-19. Debug Comparator B Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-33. DBGBAH, DBGBAM, DBGBAL Field Descriptions

Field	Description
23–16 DBGBA [23:16]	**Comparator Address Bits [23:16]**— These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one
15–0 DBGBA [15:0]	**Comparator Address Bits**[15:0]— These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

Write: If DBG not armed and PTACT is clear.

This register can be accessed with a byte resolution, whereby DBGCDM0, DBGCDM1, DBGCDM2, DBGCDM3 map to DBGCDM[31:0] respectively.

XGATE data accesses have a maximum width of 16-bits and are mapped to DBGCDM[15:0].

Table 6-38. DBGCDM Field Descriptions

Field	Description
31–16 Bits[31:16] (DBGCDM0, DBGCDM1)	**Comparator Data Mask Bits** — These bits control whether the comparator compares the data bus bits to the corresponding comparator data compare bits. 0 Do not compare corresponding data bit 1 Compare corresponding data bit
15–0 Bits[15:0] (DBGCDM2, DBGCDM3)	**Comparator Data Mask Bits** — These bits control whether the comparator compares the data bus bits to the corresponding comparator data compare bits. 0 Do not compare corresponding data bit 1 Compare corresponding data bit

6.3.2.22 Debug Comparator D Control Register (DBGDCTL)

Address: 0x0140

	7	6	5	4	3	2	1	0
R	0	0	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-24. Debug Comparator D Control Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-39. DBGDCTL Field Descriptions

Field[1]	Description
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored if INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

8.3.2.18 Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

The CPMUAPICTL register allows the configuration of the autonomous periodical interrupt features.

Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-24. Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

Read: Anytime

Write: Anytime

Table 8-19. CPMUAPICTL Field Descriptions

Field	Description
7 APICLK	**Autonomous Periodical Interrupt Clock Select Bit** — Selects the clock source for the API. Writable only if APIFE = 0. APICLK cannot be changed if APIFE is set by the same write operation. 0 Autonomous Clock (ACLK) used as source. 1 Bus Clock used as source.
4 APIES	**Autonomous Periodical Interrupt External Select Bit** — Selects the waveform at the external pin API_EXTCLK as shown in Figure 8-25. See device level specification for connectivity of API_EXTCLK pin. 0 If APIEA and APIFE are set, at the external pin API_EXTCLK periodic high pulses are visible at the end of every selected period with the size of half of the minimum period (APIR=0x0000 in Table 8-23). 1 If APIEA and APIFE are set, at the external pin API_EXTCLK a clock is visible with 2 times the selected API Period.
3 APIEA	**Autonomous Periodical Interrupt External Access Enable Bit** — If set, the waveform selected by bit APIES can be accessed externally. See device level specification for connectivity. 0 Waveform selected by APIES can not be accessed externally. 1 Waveform selected by APIES can be accessed externally, if APIFE is set.
2 APIFE	**Autonomous Periodical Interrupt Feature Enable Bit** — Enables the API feature and starts the API timer when set. 0 Autonomous periodical interrupt is disabled. 1 Autonomous periodical interrupt is enabled and timer starts running.
1 APIE	Autonomous Periodical Interrupt Enable Bit 0 API interrupt request is disabled. 1 API interrupt will be requested whenever APIF is set.
0 APIF	**Autonomous Periodical Interrupt Flag** — APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1.Writing a 0 has no effect. If enabled (APIE = 1), APIF causes an interrupt request. 0 API time-out has not yet occurred. 1 API time-out has occurred.

Table 9-14. ADCEIF Field Descriptions (continued)

Field	Description
3 TRIG_EIF	**Trigger Error Interrupt Flag** — This flag indicates that a trigger error occurred. This flag is set in “Restart” Mode when a conversion sequence got aborted and no Restart Event occurred before the Trigger Event or if the Trigger Event occurred before the Restart Event was finished (conversion command has been loaded). This flag is set in “Trigger” Mode when a Trigger Event occurs before the Restart Event is issued to start conversion of the initial Command Sequence List. In “Trigger” Mode only a Restart Event is required to start conversion of the initial Command Sequence List. This flag is set when a Trigger Event occurs before a conversion sequence got finished. This flag is also set if a Trigger occurs while a Trigger Event is just processed - first conversion command of a sequence is beginning to sample (see also Section 9.6.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios). This flag is also set if the Trigger Event occurs automatically generated by hardware in “Trigger Mode” due to a Restart Event and simultaneously a Trigger Event is generated via data bus or internal interface. The ADC ceases operation if this error flag is set (issue of type severe). 0 No trigger error occurred. 1 A trigger error occurred.
2 RSTAR_EIF	**Restart Request Error Interrupt Flag** — This flag indicates a flow control issue. It is set when a Restart Request occurs after a Trigger Event and before one of the following conditions was reached: - The “End Of List” command type has been executed - Depending on bit STR_SEQA if the “End Of List” command type is about to be executed - The current CSL has been aborted or is about to be aborted due to a Sequence Abort Request. The ADC continues operation if this error flag is set. This flag is not set for Restart Request overrun scenarios (see also Section 9.6.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios). 0 No Restart request error situation occurred. 1 Restart request error situation occurred.
1 LDOK_EIF	**Load OK Error Interrupt Flag** — This flag can only be set in “Restart Mode”. It indicates that a Restart Request occurred without LDOK. This flag is not set if a Sequence Abort Event is already in process (bit SEQA set) when the Restart Request occurs or a Sequence Abort Request occurs simultaneously with the Restart Request. The LDOK_EIF error flag is also not set in “Restart Mode” if the first Restart Event occurs after: - ADC got enabled - Exit from Stop Mode - ADC Soft-Reset - ADC used in CSL single buffer mode The ADC continues operation if this error flag is set. 0 No Load OK error situation occurred. 1 Load OK error situation occurred.

11.3.2.11 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-17. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 .

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 11-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

18.4 Functional Description

18.4.1 General

The PMF module provides the values to be driven onto the outputs of the low-side and high-side FET pre-drivers. If the FET pre-drivers are enabled, the PMF channels drive their corresponding high-side or low-side FET pre-drivers according Table 18-22.

Table 18-22. PMF Channel Assignment

PMF Channel	PMF Channel Assignment
0	High-Side Gate and Source Pins HG[0], HS[0]
1	Low-Side Gate and Source Pins LG[0], LS[0]
2	High-Side Gate and Source Pins HG[1], HS[1]
3	Low-Side Gate and Source Pins LG[1], LS[1]
4	High-Side Gate and Source Pins HG[2], HS[2]
5	Low-Side Gate and Source Pins LG[2], LS[2]

18.4.2 Low-Side FET Pre-Drivers

The three low-side FET pre-drivers turn on and off the external low-side power FETs. The energy required to charge the gate capacitance of the power FET C_G is drawn from the output of the voltage regulator VLS. See Figure 18-20. The register bits GSRCLS[2:0] in the GDUSRC Register (see Figure 18-8) control the slew rate of the low-side FET pre-drivers in order to control fast voltage changes dv/dt (see also Section 18.5.1, “FET Pre-Driver Details).

18.4.3 High-Side FET Pre-Driver

The three high-side FET pre-drivers turn on and off the external high-side power FETs. The required charge for the gate capacitance of the external power FET is delivered by the bootstrap capacitor. After the supply voltage is applied to the microcontroller or after exit from stop mode, the low-side FET pre-drivers should be activated for a short time in order to charge the bootstrap capacitor C_{BS}. Care must be taken after a long period of inactivity of the low-side FET pre-drivers to verify that the bootstrap capacitor C_{BS} is not discharged.

The register bits GSRCHS[2:0] in the GDUSRC Register (see Figure 18-8) control the slew rate of the high-side FET pre-driver in order to control fast voltage changes dv/dt (see also Section 18.5.1, “FET Pre-Driver Details).

NOTE

The minimum PWM pulse on & off time must be $t_{minpulse}$.

18.4.11 Interrupts

This section describes the interrupts generated in the GDU module. The interrupts are only available in CPU run mode. Entering and exiting stop mode has no effect on the interrupt flags. The GDU module has two interrupt vectors which are listed in Table 18-25. The low-side and high-side desaturation error flags are combined into one interrupt line and the over and under voltage detection are combined into another interrupt line. (see device specific section interrupt vector table)

Table 18-25. GDU Module Interrupt Sources

#	GDU Module Interrupt Source	Module Internal Interrupt Source	Local Enable
0	GDU desaturation error interrupt	GDU low-side and high-side desaturation error flags GDHSF[2:0] and GDLSF[2:0]	GDSEIE = 1
1	GDU over/under voltage detection and overcurrent detection interrupt	GDU low voltage condition on pin VLS (GLVLSIF)	GLVLSIE = 1
		GDU high voltage condition on pin HD (GHHDIF)	GHHDIE = 1
		GDU Overcurrent Condition (GOCIF[1:0])	GOCIE[1:0]=11

19.1.1 Features

The LIN Physical Layer module includes the following distinctive features:

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4 kbit/s, 20 kbit/s and Fast Mode (up to 250 kbit/s).
- Switchable 34 kΩ/330 kΩ pullup resistors (in shutdown mode, 330 kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.
- Automatic transmitter shutdown in case of an overcurrent or TxD-dominant timeout.
- Fulfills the OEM “Hardware Requirements for LIN (CAN and FlexRay) Interfaces in Automotive Applications” v1.3.

The HV Physical Layer module includes the following distinctive features:

- Compliant with the ISO9141 (K-line) standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for: 5.2 kHz, 10 kHz and Fast Mode (up to 125 kHz).
- Switchable 34 kΩ/330 kΩ pullup resistors (in shutdown mode, 330 kΩ only).
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.

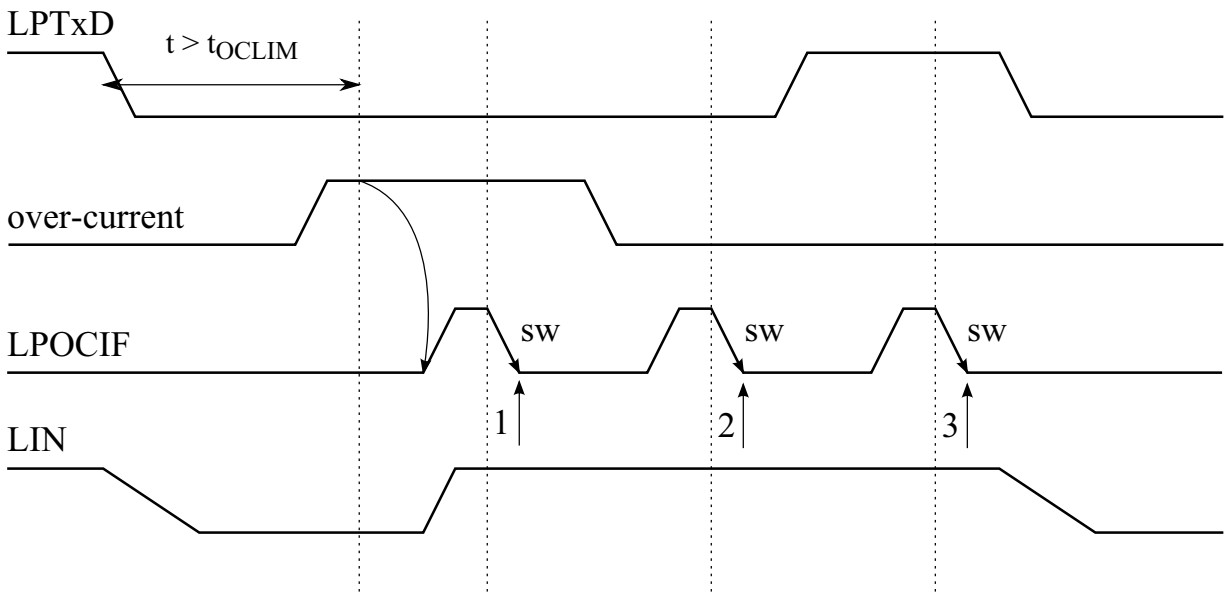
The LIN/HV transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pullup resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

19.1.2 Modes of Operation

The LIN/HV Physical Layer can operate in the following four modes:

1. Shutdown Mode

   The LIN/HV Physical Layer is fully disabled. No wake-up functionality is available. The internal pullup resistor is replaced by a high ohmic one (330 kΩ) to maintain the LIN Bus pin in the recessive state. All registers are accessible.



1: Flag cleared, transmitter re-enable not successful because over-current is still present
2: Flag cleared, transmitter re-enable not successful because LPTxD is dominant
3: Flag cleared, transmitter re-enable successful

Figure 19-12. Overcurrent interrupt handling

19.4.4.2 TxD-dominant timeout Interrupt

NOTE

In order to perform PWM communication, the TxD-dominant timeout feature must be disabled.

To protect the LIN bus from a network lock-up, the LIN Physical Layer implements a TxD-dominant timeout mechanism. When the LPTxD signal has been dominant for more than t_{DTLIM} the transmitter is disabled and the LPDT status flag and the LPDTIF interrupt flag are set.

In order to re-enable the transmitter again, the following prerequisites must be met:

1) TxD-dominant condition is over (LPDT=0)

2) LPTxD is recessive or the LIN Physical Layer is in shutdown or receive only mode for a minimum of a transmit bit time

21.2.1 CANH — CAN Bus High Pin

The CANH signal either connects directly to CAN bus high line or through an optional external common mode choke.

21.2.2 CANL — CAN Bus Low Pin

The CANL signal either connects directly to CAN bus low line or through an optional external common mode choke.

21.2.3 SPLIT — CAN Bus Termination Pin

The SPLIT pin can drive a 2.5 V bias for bus termination purpose (CAN bus middle point). Usage of this pin is optional and depends on bus termination strategy for a given bus network.

21.2.4 VDDC — Supply Pin for CAN Physical Layer

The VDDC pin is used to supply the CAN Physical Layer with 5 V from an external source.

21.2.5 VSSC — Ground Pin for CAN Physical Layer

The VSSC pin is the return path for the 5 V supply (VDDC).

21.3 Internal Signal Description

21.3.1 CPTXD — TXD Input to CAN Physical Layer

CPTXD is the input signal to the CAN Physical Layer. A logic 1 on this input is considered CAN recessive and a logic 0 as dominant level.

Per default, CPTXD is connected device-internally to the TXCAN transmitter output of the MSCAN module. For optional routing options consult the device level documentation.

21.3.2 CPRXD — RXD Output of CAN Physical Layer

CPRXD is the output signal of the CAN Physical Layer. A logic 1 on this output represents CAN recessive and a logic 0 a dominant level.

In stand-by mode the wake-up receiver is routed to this output. A dominant pulse filter can optionally be enabled to increase robustness against false wake-up pulses. In any other mode this signal defaults to the precision receiver without a pulse filter.

Per default, CPRXD is connected device-internally to the RXCAN receiver input of the MSCAN module. For optional routing options consult the device level documentation.

Table 21-7. CPIE Register Field Descriptions

Field	Description
4 CPVFIE	CAN Physical Layer Voltage-Failure Interrupt Enable If enabled, the CAN Physical Layer generates an interrupt if any of the CAN Physical Layer voltage failure interrupt flags assert. 0 Voltage failure interrupt is disabled 1 Voltage failure interrupt is enabled
3 CPDTIE	CPTXD-Dominant Timeout Interrupt Enable If enabled, the CAN Physical Layer generates an interrupt if the CPTXD-dominant timeout interrupt flag asserts. 0 CPTXD-dominant timeout interrupt is disabled 1 CPTXD-dominant timeout interrupt is enabled
0 CPOCIE	CAN Physical Layer Over-current Interrupt Enable If enabled, the CAN Physical Layer generates an interrupt if any of the CAN Physical Layer over-current interrupt flags assert. 0 Over-current interrupt is disabled 1 Over-current interrupt is enabled

21.4.2.8 CAN Physical Layer Interrupt Flag Register (CPIF)

Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CHVHIF	CHVLIF	CLVHIF	CLVLIF	CPDTIF	0	CHOCIF	CLOCIF
W								
Reset	0	0	0	0	0	0	0	0

Figure 21-9. CAN Physical Layer Interrupt Flag Register (CPIF)

1. Read: Anytime
   Write: Anytime, write 1 to clear

If any of the flags is asserted an error interrupt is pending if enabled. A flag can be cleared by writing a logic level 1 to the corresponding bit location. Writing a 0 has no effect.

Table 21-8. CPIF Register Field Descriptions

Field	Description
7 CHVHIF	CANH Voltage Failure High Interrupt Flag This flag is set to 1 when the CPCHVH bit in the CAN Physical Layer Status Register (CPSR) changes. 0 No change in CPCHVH 1 CPCHVH has changed
6 CHVLIF	CANH Voltage Failure Low Interrupt Flag This flag is set to 1 when the CPCHVL bit in the CAN Physical Layer Status Register (CPSR) changes. 0 No change in CPCHVL 1 CPCHVL has changed

- For channels 0, 1, 4, and 5 the clock choices are clock A.
- For channels 2, 3, 6, and 7 the clock choices are clock B.

22.6 Interrupts

The PWM module has no interrupt.