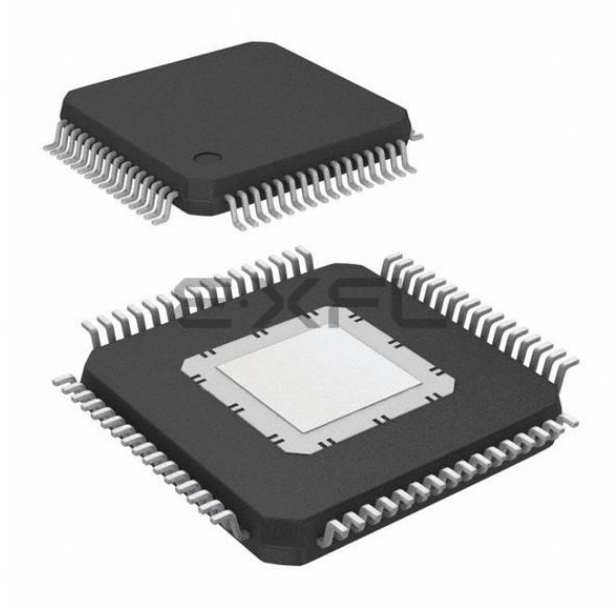

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f3mkh

Table 1-5. Module Register Address Ranges

Address	Module	Size (Bytes)
0x06E0–0x06EF	Reserved	16
0x06F0–0x06F7	BATS	8
0x06F8–0x06FF	Reserved	8
0x0700–0x0707	SCI0	8
0x0708–0x070F	Reserved	8
0x0710–0x0717	SCI1	8
0x0718–0x077F	Reserved	104
0x0780–0x0787	SPI0	8
0x0788–0x07FF	Reserved	120
0x0800–0x083F	CAN0	64
0x0840–0x097F	Reserved	320
0x0980–0x0987	LINPHY (S12ZVML derivatives)	8
0x0980–0x0987	HV Physical Interface (S12ZVM32, S12ZVM16 derivatives)	8
0x0988–0x098F	Reserved	8
0x0990–0x0997	CANPHY (ZVMC256 only)	8
0x0998–0x0FFF	Reserved	1640

1. Reading from the first 16 locations in this reserved range returns undefined data

2. Address range = 0x0690-0x069F on Maskset N06E

NOTE

Reserved register space shown above is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns zero.

1.6.1 Flash Module

This device family instantiates different flash modules, depending on derivative. The flash documentation for the all devices is featured in the FTMRZ section.

4.5.3 Wake Up from Stop or Wait Mode

4.5.3.1 CPU Wake Up from Stop or Wait Mode

Every I-bit maskable interrupt request which is configured to be handled by the CPU is capable of waking the MCU from stop or wait mode. Additionally machine exceptions can wake-up the MCU from stop or wait mode.

To determine whether an I-bit maskable interrupts is qualified to wake up the CPU or not, the same settings as in normal run mode are applied during stop or wait mode:

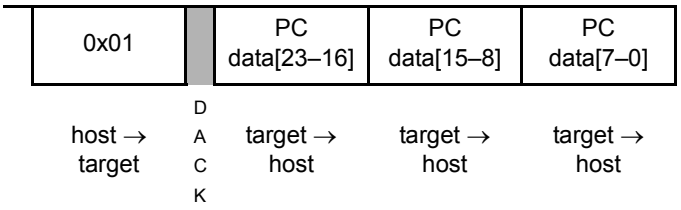
- If the I-bit in the CCW is set, all I-bit maskable interrupts are masked from waking up the MCU.
- An I-bit maskable interrupt is ignored if it is configured to a priority level below or equal to the current IPL in CCW.

The X-bit maskable interrupt request can wake up the MCU from stop or wait mode at anytime, even if the X-bit in CCW is set[1]. If the X-bit maskable interrupt request is used to wake-up the MCU with the X-bit in the CCW set, the associated ISR is not called. The CPU then resumes program execution with the instruction following the WAI or STOP instruction. This feature works following the same rules like any interrupt request, i.e. care must be taken that the X-bit maskable interrupt request used for wake-up remains active at least until the system begins execution of the instruction following the WAI or STOP instruction; otherwise, wake-up may not occur.

1. The capability of the $\overline{\text{XIRQ}}$ pin to wake-up the MCU with the X bit set may not be available if, for example, the $\overline{\text{XIRQ}}$ pin is shared with other peripheral modules on the device. Please refer to the Port Integration Module (PIM) section of the MCU reference manual for details.

5.4.4.15 SYNC_PC

Sample current PC **Non-intrusive**



This command returns the 24-bit CPU PC value to the host. Unsuccessful SYNC_PC accesses return 0xEE for each byte. If enabled, an ACK pulse is driven before the data bytes are transmitted. The value of 0xEE is returned if a timeout occurs, whereby NORESP is set. This can occur if the CPU is executing the WAI instruction, or the STOP instruction with BDCCIS clear, or if a CPU access is delayed by EWAIT. If the CPU is executing the STOP instruction and BDCCIS is set, then SYNC_PC returns the PC address of the instruction following STOP in the code listing.

This command can be used to dynamically access the PC for performance monitoring as the execution of this command is considerably less intrusive to the real-time operation of an application than a BACKGROUND/read-PC/GO command sequence. Whilst the BDC is not in active BDM, SYNC_PC returns the PC address of the instruction currently being executed by the CPU. In active BDM, SYNC_PC returns the address of the next instruction to be executed on returning from active BDM. Thus following a write to the PC in active BDM, a SYNC_PC returns that written value.

5.4.4.16 WRITE_MEM.sz, WRITE_MEM.sz_WS

WRITE_MEM.sz

Write memory at the specified address **Non-intrusive**

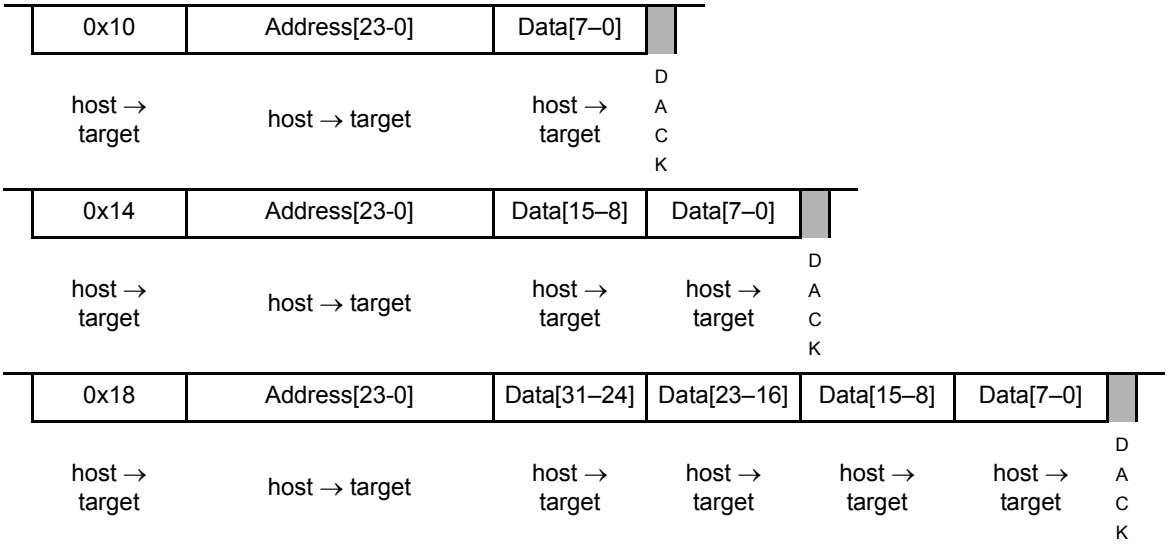


Table 8-31. CPMUVREGCTL Field Descriptions (continued)

Field	Description
4 EXTS1ON	**External voltage regulator Enable Bit for VDDS1 domain** — Should be enabled after system startup if VDDS1 is used. 0 VDDS1 domain disabled 1 VDDS1 domain enabled. BCTLS1 pin is active.
2 EXTCON	**External voltage regulator Enable Bit for VDDC domain** — Should be disabled after system startup if VDDC domain is not used. Must be kept set, if an internal or external CANPHY is present in the application. 0 VDDC domain disabled 1 VDDC domain enabled. BCTLC pin is active.
1 EXTXON	**External voltage regulator Enable Bit for VDDX domain** — Should be set to 1 if external BJT is present on the PCB, cleared otherwise. 0 VDDX control loop does not use external BJT 1 VDDX control loop uses external BJT
0 INTXON	**Internal voltage regulator Enable Bit for VDDX domain**— Should be set to 1 if no external BJT is present on the PCB, cleared otherwise. 0 VDDX control loop does not use internal power transistor 1 VDDX control loop uses internal power transistor

8.3.2.28 S12CPMU_UHV_V10_V6 Oscillator Register 2 (CPMUOSC2)

This registers configures the external oscillator (XOSCLCP).

Module Base + 0x001E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	OMRE	OSCMOD
W								
Reset	0	0	0	0	0	0	0	0

Figure 8-39. S12CPMU_UHV_V10_V6 Oscillator Register 2 (CPMUOSC2)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

Several examples of PLL divider settings are shown in Table 8-34. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 8-34. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz
off	$00	1MHz	00	$18	50MHz	01	$00	50MHz	25MHz
4MHz	$00	4MHz	01	$05	48MHz	00	$00	48MHz	24MHz

The phase detector inside the PLL compares the feedback clock (FBCLK = VCOCLK/(SYNDIV+1)) with the reference clock (REFCLK = (IRC1M or OSCCLK)/(REFDIV+1)). Correction pulses are generated based on the phase difference between the two signals. The loop filter alters the DC voltage on the internal filter capacitor, based on the width and direction of the correction pulse which leads to a higher or lower VCO frequency.

The user must select the range of the REFCLK frequency (REFFRQ[1:0] bits) and the range of the VCOCLK frequency (VCOFRQ[1:0] bits) to ensure that the correct PLL loop bandwidth is set.

The lock detector compares the frequencies of the FBCLK and the REFCLK. Therefore the speed of the lock detector is directly proportional to the reference clock frequency. The circuit determines the lock condition based on this comparison. So e.g. a failure in the reference clock will cause the PLL not to lock.

If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and for instance check the LOCK bit. If interrupt requests are disabled, software can poll the LOCK bit continuously (during PLL start-up) or at periodic intervals. In either case, only when the LOCK bit is set, the VCOCLK will have stabilized to the programmed frequency.

- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within the tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of the tolerance, Δ_{unl}.

Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.In case of loss of reference clock (e.g. IRCCLK) the PLL will not lock or if already locked, then it will unlock. The frequency of the VCOCLK will be very low and will depend on the value of the VCOFRQ[1:0] bits.

13.2 External Signal Description

The MSCAN uses two external pins.

NOTE

On MCUs with an integrated CAN physical interface (transceiver) the MSCAN interface is connected internally to the transceiver interface. In these cases the external availability of signals TXCAN and RXCAN is optional.

13.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

13.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

0 = Dominant state
1 = Recessive state

13.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 13-2. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

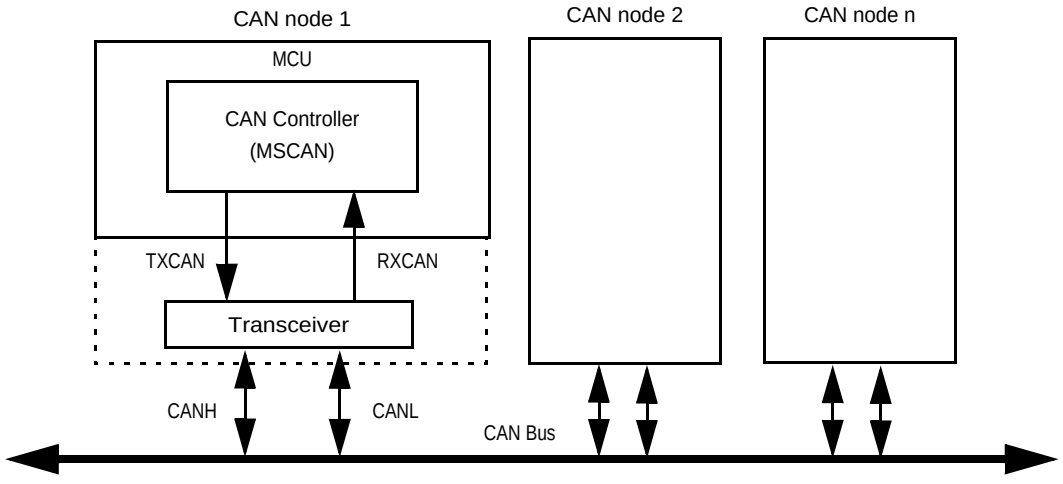


Figure 13-2. CAN System

Table 13-7. CANBTR1 Register Field Descriptions (continued)

Field	Description
6-4 TSEG2[2:0]	**Time Segment 2** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 13-44). Time segment 2 (TSEG2) values are programmable as shown in Table 13-8.
3-0 TSEG1[3:0]	**Time Segment 1** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 13-44). Time segment 1 (TSEG1) values are programmable as shown in Table 13-9.

1. In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

Table 13-8. Time Segment 2 Values

TSEG22	TSEG21	TSEG20	Time Segment 2
0	0	0	1 Tq clock cycle(1)
0	0	1	2 Tq clock cycles
:	:	:	:
1	1	0	7 Tq clock cycles
1	1	1	8 Tq clock cycles

1. This setting is not valid. Please refer to Table 13-36 for valid settings.

Table 13-9. Time Segment 1 Values

TSEG13	TSEG12	TSEG11	TSEG10	Time segment 1
0	0	0	0	1 Tq clock cycle(1)
0	0	0	1	2 Tq clock cycles1
0	0	1	0	3 Tq clock cycles1
0	0	1	1	4 Tq clock cycles
:	:	:	:	:
1	1	1	0	15 Tq clock cycles
1	1	1	1	16 Tq clock cycles

1. This setting is not valid. Please refer to Table 13-36 for valid settings.

The bit time is determined by the oscillator frequency, the baud rate prescaler, and the number of time quanta (Tq) clock cycles per bit (as shown in Table 13-8 and Table 13-9).

Eqn. 13-1

$$\text{Bit Time} = \frac{(\text{Prescaler value})}{f_{CANCLK}} \bullet (1 + \text{TimeSegment1} + \text{TimeSegment2})$$

For microcontrollers without a clock and reset generator (CRG), CANCLK is driven from the crystal oscillator (oscillator clock).

A programmable prescaler generates the time quanta (Tq) clock from CANCLK. A time quantum is the atomic unit of time handled by the MSCAN.

Eqn. 13-2

$$\Gamma q = \frac{f_{CANCLK}}{(\text{Prescaler value}}$$

A bit time is subdivided into three segments as described in the Bosch CAN 2.0A/B specification. (see Figure 13-44):

- SYNC_SEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time Segment 1: This segment includes the PROP_SEG and the PHASE_SEG1 of the CAN standard. It can be programmed by setting the parameter TSEG1 to consist of 4 to 16 time quanta.
- Time Segment 2: This segment represents the PHASE_SEG2 of the CAN standard. It can be programmed by setting the TSEG2 parameter to be 2 to 8 time quanta long.

Eqn. 13-3

$$\text{Bit Rate} = \frac{f_{Tq}}{(\text{number of Time Quanta})}$$

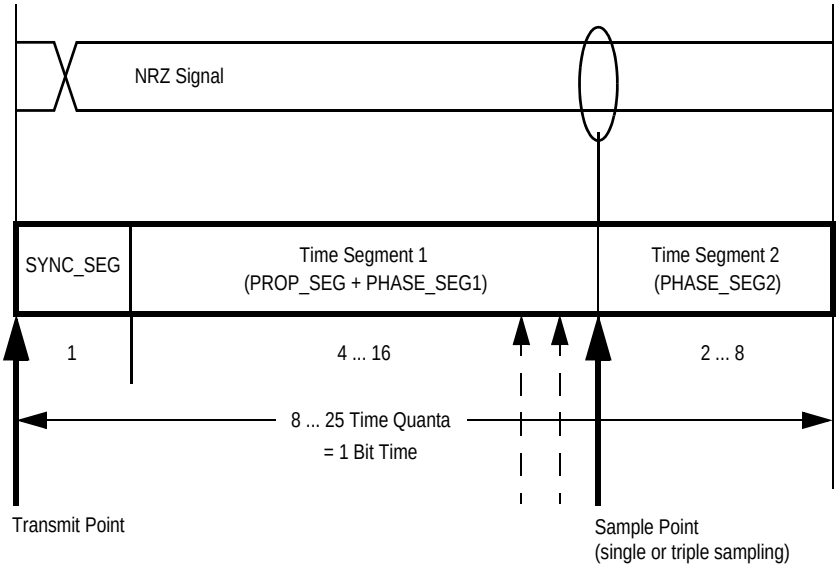


Figure 13-44. Segments within the Bit Time

Table 13-35. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the CAN bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node in receive mode samples the CAN bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

The synchronization jump width (see the Bosch CAN 2.0A/B specification for details) can be programmed in a range of 1 to 4 time quanta by setting the SJW parameter.

The SYNC_SEG, TSEG1, TSEG2, and SJW parameters are set by programming the MSCAN bus timing registers (CANBTR0, CANBTR1) (see Section 13.3.2.3, “MSCAN Bus Timing Register 0 (CANBTR0)” and Section 13.3.2.4, “MSCAN Bus Timing Register 1 (CANBTR1)”).

Table 13-36 gives an overview of the Bosch CAN 2.0A/B specification compliant segment settings and the related parameter values.

NOTE

It is the user’s responsibility to ensure the bit time settings are in compliance with the CAN standard.

Table 13-36. Bosch CAN 2.0A/B Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronization Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

13.4.4 Modes of Operation

13.4.4.1 Normal System Operating Modes

The MSCAN module behaves as described within this specification in all normal system operating modes. Write restrictions exist for some registers.

Table 13-37. CPU vs. MSCAN Operating Modes

CPU Mode	MSCAN Mode			
	Normal	Reduced Power Consumption		
		Sleep	Power Down	Disabled (CANE=0)
RUN	CSWAI = X[1] SLPRQ = 0 SLPAK = 0	CSWAI = X SLPRQ = 1 SLPAK = 1		CSWAI = X SLPRQ = X SLPAK = X
WAIT	CSWAI = 0 SLPRQ = 0 SLPAK = 0	CSWAI = 0 SLPRQ = 1 SLPAK = 1	CSWAI = 1 SLPRQ = X SLPAK = X	CSWAI = X SLPRQ = X SLPAK = X
STOP			CSWAI = X SLPRQ = X SLPAK = X	CSWAI = X SLPRQ = X SLPAK = X

1. ‘X’ means don’t care.

13.4.5.1 Operation in Run Mode

As shown in Table 13-37, only MSCAN sleep mode is available as low power option when the CPU is in run mode.

13.4.5.2 Operation in Wait Mode

The WAI instruction puts the MCU in a low power consumption stand-by mode. If the CSWAI bit is set, additional power can be saved in power down mode because the CPU clocks are stopped. After leaving this power down mode, the MSCAN restarts and enters normal mode again.

While the CPU is in wait mode, the MSCAN can be operated in normal mode and generate interrupts (registers can be accessed via background debug mode).

13.4.5.3 Operation in Stop Mode

The STOP instruction puts the MCU in a low power consumption stand-by mode. In stop mode, the MSCAN is set in power down mode regardless of the value of the SLPRQ/SLPAK and CSWAI bits (Table 13-37).

13.4.5.4 MSCAN Normal Mode

This is a non-power-saving mode. Enabling the MSCAN puts the module from disabled mode into normal mode. In this mode the module can either be in initialization mode or out of initialization mode. See Section 13.4.4.5, “MSCAN Initialization Mode”.

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0009 TG0TVL	R	TG0TV[7:0]							
	W								
0x000A TG1LIST	R	0	0	0	0	0	0	0	TG1LIST
	W								
0x000B TG1TNUM	R	0	0	0	TG1TNUM[4:0]				
	W								
0x000C TG1TVH	R	TG1TV[15:8]							
	W								
0x000D TG1TVL	R	TG1TV[7:0]							
	W								
0x000E PTUCNTH	R	PTUCNT[15:8]							
	W								
0x000F PTUCNTL	R	PTUCNT[7:0]							
	W								
0x0010 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0011 PTUPTRH	R	PTUPTR[23:16]							
	W								
0x0012 PTUPTRM	R	PTUPTR[15:8]							
	W								
0x0013 PTUPTRL	R	PTUPTR[7:1]							0
	W								
0x0014 TG0L0IDX	R	0	TG0L10DX[6:0]						
	W								
0x0015 TG0L1IDX	R	0	TG0L1IDX[6:0]						
	W								
0x0016 TG1L0IDX	R	0	TG1L0IDX[6:0]						
	W								
0x0017 TG1L1IDX	R	0	TG1L1IDX[6:0]						
	W								

= Unimplemented

Figure 14-2. PTU Register Summary

The transmitting device can address messages to selected receivers by including addressing information in the initial frame or frames of each message.

The WAKE bit in SCI control register 1 (SCICR1) determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

16.4.6.6.1 Idle Input line Wakeup (WAKE = 0)

In this wakeup method, an idle condition on the RXD pin clears the RWU bit and wakes up the SCI. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle character appears on the RXD pin.

Idle line wakeup requires that messages be separated by at least one idle character and that no message contains idle characters.

The idle character that wakes a receiver does not set the receiver idle bit, IDLE, or the receive data register full flag, RDRF.

The idle line type bit, ILT, determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit. ILT is in SCI control register 1 (SCICR1).

16.4.6.6.2 Address Mark Wakeup (WAKE = 1)

In this wakeup method, a logic 1 in the most significant bit (MSB) position of a frame clears the RWU bit and wakes up the SCI. The logic 1 in the MSB position marks a frame as an address frame that contains addressing information. All receivers evaluate the addressing information, and the receivers for which the message is addressed process the frames that follow.Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD pin.

The logic 1 MSB of an address frame clears the receiver’s RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wakeup allows messages to contain idle characters but requires that the MSB be reserved for use in address frames.

NOTE

With the WAKE bit clear, setting the RWU bit after the RXD pin has been idle can cause the receiver to wake up immediately.

16.4.7 Single-Wire Operation

Normally, the SCI uses two pins for transmitting and receiving. In single-wire operation, the RXD pin is disconnected from the SCI. The SCI uses the TXD pin for both receiving and transmitting.

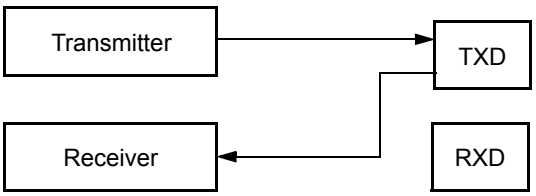


Figure 16-30. Single-Wire Operation (LOOPS = 1, RSRC = 1)

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

16.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

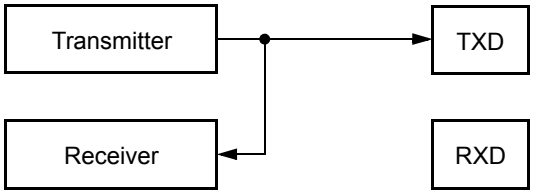


Figure 16-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

16.5 Initialization/Application Information

16.5.1 Reset Initialization

See Section 16.3.2, “Register Descriptions”.

17.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 17-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 17-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 17-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 17-10).

20.4.7.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 20-48. Erase Flash Block Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x09	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 20-49. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 20-50. Erase P-Flash Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0A	Global address [23:16] to identify P-Flash block to be erased
FCCOB1	Global address [15:0] anywhere within the sector to be erased. Refer to Section 20.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

20.4.8.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the SFDIF flag in combination with the SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 20.3.2.5, “Flash Configuration Register (FCNFG)”, Section 20.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 20.3.2.7, “Flash Status Register (FSTAT)”, and Section 20.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 20-31.

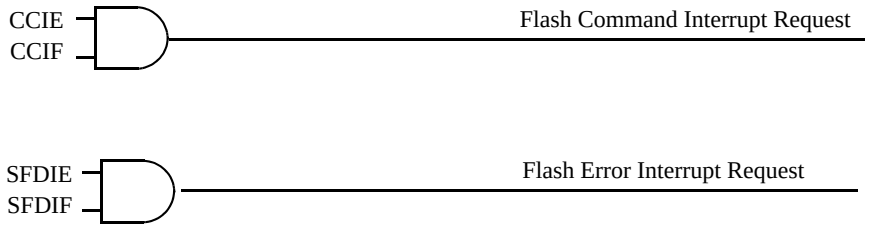


Figure 20-31. Flash Module Interrupts Implementation

20.4.9 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 20.4.8, “Interrupts”).

20.4.10 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

20.5 Security

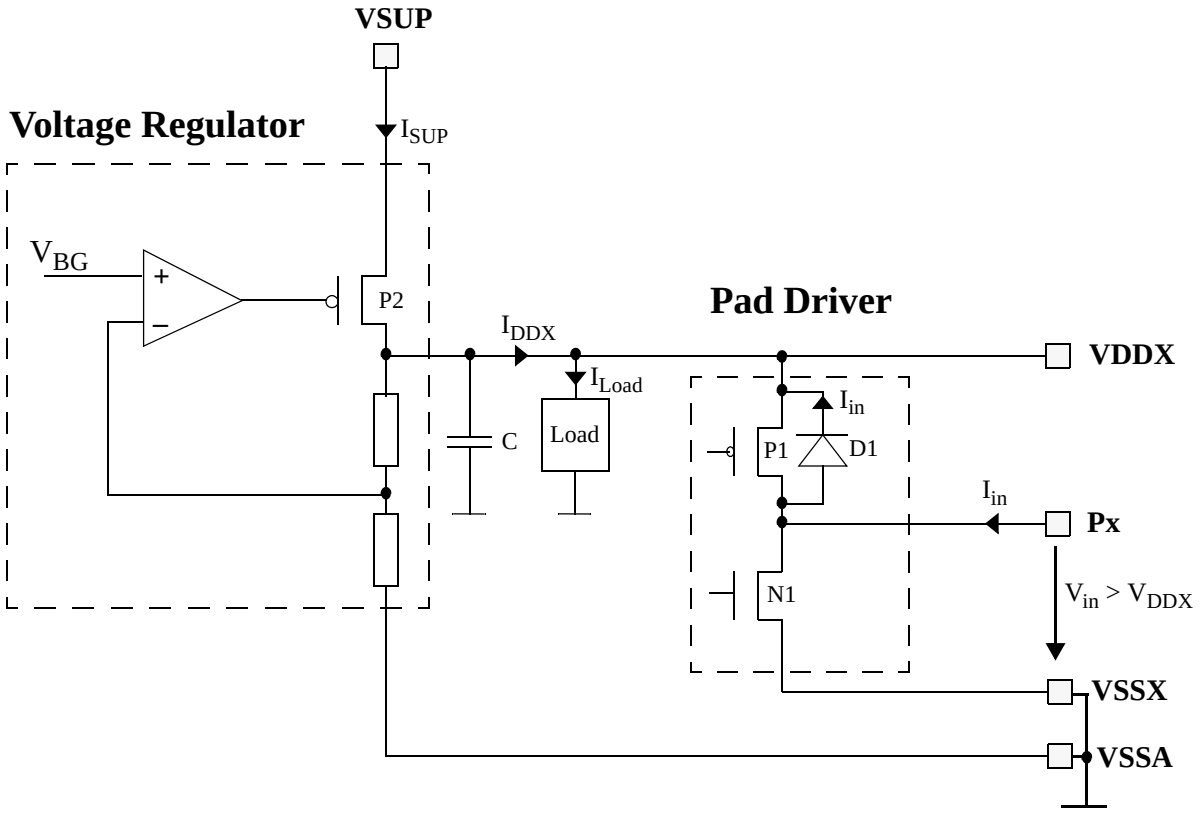
The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 20-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0xFF_FE0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

power; e.g., if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Figure A-1. Current Injection on GPIO Port if $V_{in} > V_{DDX}$



A.1.4 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation outside these ranges is not guaranteed. Stress beyond these limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level.

The CANPHY maximum ratings are specified in Appendix H.1

Table A-2. Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
1	Voltage regulator and LINPHY supply voltage	V_{SUP}	-0.3	42	V
2	DC voltage on LIN	V_{LIN}	-32	42	V
3	DC voltage on HVI pin PL0	V_{HVI}	-27	42	V
4	Core logic supply voltage	V_{DD}	-0.3	2.16	V

Appendix E
GDU Electrical Specifications

NOTE

It is necessary to consider the power dissipation of the FET channel versus the power dissipation in the FET-Predriver.

FET-Predriver dissipation is Power VSUP x f(PWM) x C(FET-GATE)
FET channel power dissipation is a function of channel current and voltage.

Reducing the RDSON of the external FET to reduce the FET power dissipation increases the FET gate capacitance.

At a certain FET level, further reduction of FET RDSON actually increases overall power consumption because the increased charging and discharging power dissipation due to increased gate capacitance outweighs the FET power reduction due to RDSON reduction.

E.1 GDU specifications for devices featuring GDU V4 or V6

Table E-1. GDU Electrical Characteristics (Junction Temperature From –40°C To +175°C)

4.85V<=VDDX,VDDA<=5.15V						
Num	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	VSUP Supply range	V_{VSUP}	-0.3	—	40	V
2a	VSUP, HD Supply range FETs can be turned on(1) (normal range)	V_{VSUP}/V_{HD}	7	14	20	V
2b	VSUP, HD Supply range FETs can be turned on(2) (extended range)	V_{VSUP}/V_{HD}	7	14	26.6	V
3	External FET Vgs drive with boost(3) (7V < V_{RBATP} < 20V)	V_{VGS}	9	9.6	12	V
4	External FET Vgs drive without boost(4)	V_{VGS}	5	9.6	12	V
5	External FET total gate charge @ 10V(5)	QG	—	75	—	nC
6	Pull resistance between HGx and HSx	R_{HSpul}	60	80	120	KΩ
7	Pull resistance between LGx and LSx	R_{LSpul}	60	80	120	KΩ
8a	VLS output voltage for Vsup >=12.5V, Iout=30mA -40°C < T_j < 150°C	V_{VLS_OUT}	10.5	11	11.5	V
8b	VLS output voltage for Vsup >=12.5V, Iout=30mA 150°C < T_j < 175°C	V_{VLS_OUT}	10.0	10.6	11.5	V
9	VLS current limit threshold	I_{LIMVLS}	60	77	112	mA
10a	VLS low voltage monitor trippoint assert (GDUV6 with GVLSLVL=1 or GDUV4)	V_{LVLSHA}	6.2	6.5	7	V
10b	VLS low voltage monitor trippoint deassert (GDUV6 with GVLSLVL=1 or GDUV4)	V_{LVLSHD}	6.2	6.58	7	V
10c	VLS low voltage monitor trippoint assert (GDUV6 with GVLSLVL=0)	V_{LVLSLA}	5.2	5.5	6	V
10d	VLS low voltage monitor trippoint deassert (GDUV6 with GVLSLVL=0)	V_{LVLSLD}	5.2	5.55	6	V
11a	HD high voltage monitor assert trippoint low	V_{HVHDLA}	20	21	22	V

Table F-5. FTMRZ256K1KNVM Timing Characteristics (Junction Temperature From –40°C To +150°C)

Derivative ZVMC256									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	50	50	50	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	66973	t_{RD1ALL}	1.34	1.34	2.68	133.95	ms
4	Erase Verify Block (Pflash)	0	66284	t_{RD1BLK_P}	1.33	1.33	2.65	132.57	ms
5	Erase Verify Block (EEPROM)	0	1101	t_{RD1BLK_D}	0.02	0.02	0.04	2.20	ms
6	Erase Verify P-Flash Section	0	640	t_{RD1SEC}	0.01	0.01	0.03	1.28	ms
7	Read Once	0	512	t_{RDONCE}	10.24	10.24	10.24	512.00	us
8	Program P-Flash (4 Word)	164	3221	t_{PGM_4}	0.22	0.23	0.42	13.09	ms
9	Program Once	164	3138	$t_{PGMONCE}$	0.22	0.23	0.23	3.34	ms
10	Erase All Blocks	200126	67786	t_{ERSALL}	191.95	201.48	202.84	385.73	ms
11	Erase Flash Block (Pflash)	200120	66855	t_{ERSBLK_P}	191.93	201.46	202.79	383.86	ms
12	Erase Flash Block (EEPROM)	100060	1401	t_{ERSBLK_D}	95.32	100.09	100.12	127.88	ms
13	Erase P-Flash Sector	20015	1022	t_{ERSPG}	19.08	20.04	20.06	27.06	ms
14	Unsecure Flash	200126	67864	t_{UNSECU}	191.95	201.48	202.84	385.89	ms
15	Verify Backdoor Access Key	0	524	t_{VFYKEY}	10.48	10.48	10.48	524.00	us
16	Set User Margin Level	0	477	t_{MLOADU}	9.54	9.54	9.54	477.00	us
17	Set Factory Margin Level	0	486	t_{MLOADF}	9.72	9.72	9.72	486.00	us
18	Erase Verify EEPROM Sector	0	613	$t_{DRD1SEC}$	0.01	0.01	0.02	1.23	ms
19	Program EEPROM (1 Word)	68	1694	t_{DPGM_1}	0.10	0.10	0.20	6.86	ms
20	Program EEPROM (2 Word)	136	2718	t_{DPGM_2}	0.18	0.19	0.35	11.04	ms
21	Program EEPROM (3 Word)	204	3742	t_{DPGM_3}	0.27	0.28	0.50	15.22	ms
22	Program EEPROM (4 Word)	272	4766	t_{DPGM_4}	0.35	0.37	0.65	19.40	ms
23	Erase EEPROM Sector	5015	839	t_{DERSPG}	4.79	5.03	20.35	39.34	ms
24	Protection Override	0	506	$t_{PRTOVRD}$	10.12	10.12	10.12	506.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.

9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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TITLE: LQFP, 7 X 7 X 1.4 PKG, 0.5 PITCH, 48LD 4.4 X 4.4 EXPOSED PAD	DOCUMENT NO: 98ASA00945D	REV: X0
	STANDARD: NON–JEDEC	
	02 NOV 2015	