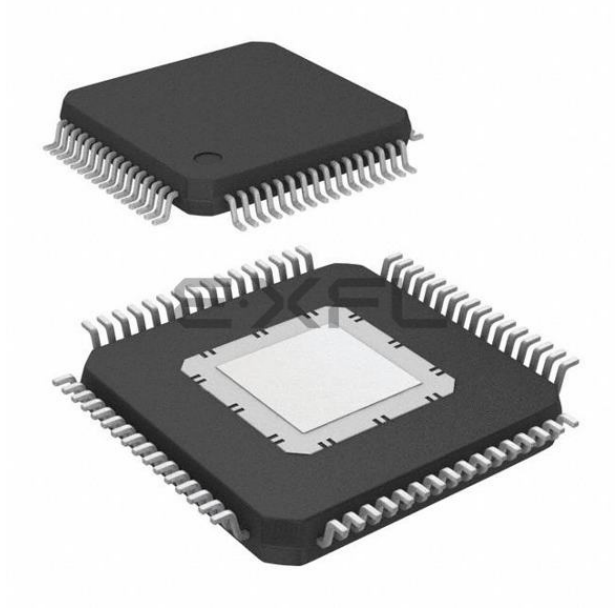

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f3mkhr

1.11 Resets and Interrupts

1.11.1 Reset

Table 1-15. lists all reset sources and the vector locations. Resets are explained in detail in the Chapter 8, “S12 Clock, Reset and Power Management Unit (V10 and V6)”.

Table 1-15. Reset Sources and Vector Locations

Vector Address	Reset Source	CCR Mask	Local Enable
0xFFFFFC	Power-On Reset (POR)	None	None
	Low Voltage Reset (LVR)	None	None
	External pin $\overline{\text{RESET}}$	None	None
	PLL clock monitor reset	None	None
	Oscillator Clock monitor reset	None	OSCE in CPMUOSC register OMRE in CPMUOSC2 register
	COP watchdog reset	None	CR[2:0] in CPMUCOP register

1.11.2 Interrupt Vectors

Table 1-16 lists all interrupt sources and vectors in the default order of priority. The interrupt module description provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 1-16. Interrupt Vector Locations

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + 0x1F8	Unimplemented page1 op-code trap (SPARE)	None	None	-	-
Vector base + 0x1F4	Unimplemented page2 op-code trap (TRAP)	None	None	-	-
Vector base + 0x1F0	Software interrupt instruction (SWI)	None	None	-	-
Vector base + 0x1EC	System call interrupt instruction (SYS)	None	None	-	-
Vector base + 0x1E8	Machine exception	None	None	-	-
Vector base + 0x1E4	Reserved				
Vector base + 0x1E0	Reserved				
Vector base + 0x1DC	Spurious interrupt	—	None	-	-
Vector base + 0x1D8	$\overline{\text{XIRQ}}$ interrupt request	X bit	None	Yes	Yes
Vector base + 0x1D4	$\overline{\text{IRQ}}$ interrupt request	I bit	IRQCR(IRQEN)	Yes	Yes
Vector base + 0x1D0	RTI time-out interrupt	I bit	CPMUINT (RTIE)	**See CPMU section**	Yes

2.3.4.4 Port L Input Register (PTIL)

Address 0x0331 Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTIL0[2]
W								
Reset	0	0	0	0	0	0	0	-

Figure 2-26. Port L Input Register (PTIL)

1. Read: Anytime
   Write: No Write
2. Only available for S12ZVMC256

Table 2-30. PTIL - Register Field Descriptions

Field	Description
0 PTIL0	**Port Input Data Register Port L —** A read returns the synchronized input state if the associated pin is used in digital mode, that is the related DIENL bit is set to 1 and the pin is not used in analog mode (PTAENL[PTAENL0]=0). See Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL)”. A one is read in any other case[1].

1. Refer to PTTEL bit description in Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL) for an override condition.

2.3.4.5 Port L Pull Select Register (PTPSL)

Address 0x0333 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTPSL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-27. Port L Pull Select Register (PTPSL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-31. PTPSL Register Field Descriptions

Field	Description
1-0 PTPSL0	**Port L Pull Select —** This bit selects a pull device on the HVI pin in analog mode for open input detection. By default a pulldown device is active as part of the input voltage divider. If this bit set to 1 and PTTEL=1 and not in stop mode a pullup to a level close to V_{DDX} takes effect and overrides the weak pulldown device. Refer to Section 2.5.2, “Open Input Detection on HVI”). 1 Pullup enabled 0 Pulldown enabled

3.1.1 Glossary

Table 3-2. Glossary Of Terms

Term	Definition
MCU	Microcontroller Unit
CPU	S12Z Central Processing Unit
BDC	S12Z Background Debug Controller
ADC	Analog-to-Digital Converter
PTU	Programmable Trigger Unit
unmapped address range	Address space that is not assigned to a memory
reserved address range	Address space that is reserved for future use cases
illegal access	Memory access, that is not supported or prohibited by the S12ZMMC, e.g. a data store to NVM
access violation	Either an illegal access or an uncorrectable ECC error
byte	8-bit data
word	16-bit data

3.1.2 Overview

The S12ZMMC provides access to on-chip memories and peripherals for the S12ZCPU, the S12ZBDC, the PTU, and the ADC. It arbitrates memory accesses and determines all of the MCU memory maps. Furthermore, the S12ZMMC is responsible for selecting the MCUs functional mode.

3.1.3 Features

- S12ZMMC mode operation control
- Memory mapping for S12ZCPU and S12ZBDC, PTU and ADCs
  - — Maps peripherals and memories into a 16 MByte address space for the S12ZCPU, the S12ZBDC, the PTU, and the ADCs
  - — Handles simultaneous accesses to different on-chip resources (NVM, RAM, and peripherals)
- Access violation detection and logging
  - — Triggers S12ZCPU machine exceptions upon detection of illegal memory accesses and uncorrectable ECC errors
  - — Logs the state of the S12ZCPU and the cause of the access error

Table 3-7. MMCPCH, MMCPCM, and MMCPCL Field Descriptions

Field	Description
7–0 (MMCPCH) 7–0 (MMCPCM) 7–0 (MMCPCL) CPUPC[23:0]	**S12ZCPU Program Counter Value**— The CPUPC[23:0] stores the CPU's program counter value at the time the access violation occurred. CPUPC[23:0] always points to the instruction which triggered the violation. These bits are undefined if the error code registers (MMCECn) are cleared.

3.4 Functional Description

This section provides a complete functional description of the S12ZMMC module.

3.4.1 Global Memory Map

The S12ZMMC maps all on-chip resources into an 16MB address space, the global memory map. The exact resource mapping is shown in Figure 3-8. The global address space is used by the S12ZCPU, ADCs, PTU, and the S12ZBDC module.

- All illegal accesses performed by an ADC or PTU module trigger error interrupts. See ADC and PTU section for details.

NOTE

Illegal accesses caused by S12ZCPU opcode prefetches will also trigger machine exceptions, even if those opcodes might not be executed in the program flow. To avoid these machine exceptions, S12ZCPU instructions must not be executed from the last (high addresses) 8 bytes of RAM, EEPROM, and Flash.

3.4.3 Uncorrectable ECC Faults

RAM and flash use error correction codes (ECC) to detect and correct memory corruption. Each uncorrectable memory corruption, which is detected during a S12ZCPU, ADC or PTU access triggers a machine exception. Uncorrectable memory corruptions which are detected during a S12ZBDC access, are captured in the RAMWF or the RDINV bit of the BDCCSRL register.

7.2.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field functions follow the register diagrams, in bit order.

7.2.2.1 ECC Status Register (ECCSTAT)

Module Base + 0x00000 — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RDY
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Never

Figure 7-2. ECC Status Register (ECCSTAT)

Table 7-2. ECCSTAT Field Description

Field	Description
0 RDY	ECC Ready— Shows the status of the ECC module. 0 Internal SRAM initialization is ongoing, access to the SRAM is disabled 1 Internal SRAM initialization is done, access to the SRAM is enabled

7.2.2.2 ECC Interrupt Enable Register (ECCIE)

Module Base + 0x00001 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIE
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime

Figure 7-3. ECC Interrupt Enable Register (ECCIE)

Table 7-3. ECCIE Field Description

Field	Description
0 SBEEIE	Single bit ECC Error Interrupt Enable — Enables Single ECC Error interrupt. 0 Interrupt request is disabled 1 Interrupt will be requested whenever SBEEIF is set

9.2 Introduction

The ADC12B_LBA is an n-channel multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ADC parameters and accuracy.

The List Based Architecture (LBA) provides flexible conversion sequence definition as well as flexible oversampling. The order of channels to be converted can be freely defined. Also, multiple instantiations of the module can be triggered simultaneously (matching sampling point across multiple module instantiations).

There are four register bits which control the conversion flow (please refer to the description of register ADCFLWCTL).
The four conversion flow control bits of register ADCFLWCTL can be modified in two different ways:

- Via data bus accesses
- Via internal interface Signals (Trigger, Restart, LoadOK, and Seq_Abort; see also Figure 9-2). Each Interface Signal is associated with one conversion flow control bit.

For information regarding internal interface connectivity related to the conversion flow control please refer to the device overview of the reference manual.

The ADCFLWCTL register can be controlled via internal interface only or via data bus only or by both depending on the register access configuration bits ACC_CFG[1:0].

The four bits of register ADCFLWCTL reflect the captured request and status of the four internal interface Signals (LoadOK, Trigger, Restart, and Seq_abort; see also Figure 9-2) if access configuration is set accordingly and indicate event progress (when an event is processed and when it is finished).

Conversion flow error situations are captured by corresponding interrupt flags in the ADCEIF register.

There are two conversion flow control modes (Restart Mode, Trigger Mode). Each mode causes a certain behavior of the conversion flow control bits which can be selected according to the application needs.

Please refer to Section 9.5.2.1, “ADC Control Register 0 (ADCCTL_0) and Section 9.6.3.2.4, “The two conversion flow control Mode Configurations for more information regarding conversion flow control.

Because internal components of the ADC are turned on/off with bit ADC_EN, the ADC requires a recovery time period (t_{REC}) after ADC is enabled until the first conversion can be launched via a trigger.

When bit ADC_EN gets cleared (transition from 1’b1 to 1’b0) any ongoing conversion sequence will be aborted and pending results, or the result of current conversion, gets discarded (not stored). The ADC cannot be re-enabled before any pending action or action in process is finished respectively aborted, which could take up to a maximum latency time of $t_{DISABLE}$ (see device level specification for more details).

12.3.2.7 Timer Control Register 3/Timer Control Register 4 (TCTL3 and TCTL4)

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 12-12. Timer Control Register 3 (TCTL3)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 12-13. Timer Control Register 4 (TCTL4)

Read: Anytime

Write: Anytime.

Table 12-8. TCTL3/TCTL4 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
1:0 EDGnB EDGnA	**Input Capture Edge Control** — These two pairs of control bits configure the input capture edge detector circuits.

Table 12-9. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

13.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

Module Base + 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
W								
Reset:	0	0	0	1	0	0	0	1

= Unimplemented

Figure 13-5. MSCAN Control Register 1 (CANCTL1)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-3. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 13.4.3.2, “Clock System,” and Section Figure 13-43., “MSCAN Clocking Scheme,”). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 13.4.4.4, “Listen-Only Mode”). In addition, the error counters are frozen. Listen only mode supports applications which require “hot plugging” or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
3 BORM	**Bus-Off Recovery Mode** — This bit configures the bus-off state recovery mode of the MSCAN. Refer to Section 13.5.2, “Bus-Off Recovery,” for details. 0 Automatic bus-off recovery (see Bosch CAN 2.0A/B protocol specification) 1 Bus-off recovery upon user request

Table 13-3. CANCTL1 Register Field Descriptions (continued)

Field	Description
2 WUPM	**Wake-Up Mode** — If WUPE in CANCTL0 is enabled, this bit defines whether the integrated low-pass filter is applied to protect the MSCAN from spurious wake-up (see Section 13.4.5.5, “MSCAN Sleep Mode”). 0 MSCAN wakes up on any dominant level on the CAN bus 1 MSCAN wakes up only in case of a dominant pulse on the CAN bus that has a length of T_{wup}
1 SLPAK	**Sleep Mode Acknowledge** — This flag indicates whether the MSCAN module has entered sleep mode (see Section 13.4.5.5, “MSCAN Sleep Mode”). It is used as a handshake flag for the SLPRQ sleep mode request. Sleep mode is active when SLPRQ = 1 and SLPAK = 1. Depending on the setting of WUPE, the MSCAN will clear the flag if it detects activity on the CAN bus while in sleep mode. 0 Running — The MSCAN operates normally 1 Sleep mode active — The MSCAN has entered sleep mode
0 INITAK	**Initialization Mode Acknowledge** — This flag indicates whether the MSCAN module is in initialization mode (see Section 13.4.4.5, “MSCAN Initialization Mode”). It is used as a handshake flag for the INITRQ initialization mode request. Initialization mode is active when INITRQ = 1 and INITAK = 1. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0–CANIDAR7, and CANIDMR0–CANIDMR7 can be written only by the CPU when the MSCAN is in initialization mode. 0 Running — The MSCAN operates normally 1 Initialization mode active — The MSCAN has entered initialization mode

13.3.2.3 MSCAN Bus Timing Register 0 (CANBTR0)

The CANBTR0 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
Reset:	0	0	0	0	0	0	0	0

Figure 13-6. MSCAN Bus Timing Register 0 (CANBTR0)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-4. CANBTR0 Register Field Descriptions

Field	Description
7-6 SJW[1:0]	**Synchronization Jump Width** — The synchronization jump width defines the maximum number of time quanta (Tq) clock cycles a bit can be shortened or lengthened to achieve resynchronization to data transitions on the CAN bus (see Table 13-5).
5-0 BRP[5:0]	**Baud Rate Prescaler** — These bits determine the time quanta (Tq) clock which is used to build up the bit timing (see Table 13-6).

Table 13-25. Message Buffer Organization

Offset Address	Register	Access
0x00X0	IDR0 — Identifier Register 0	R/W
0x00X1	IDR1 — Identifier Register 1	R/W
0x00X2	IDR2 — Identifier Register 2	R/W
0x00X3	IDR3 — Identifier Register 3	R/W
0x00X4	DSR0 — Data Segment Register 0	R/W
0x00X5	DSR1 — Data Segment Register 1	R/W
0x00X6	DSR2 — Data Segment Register 2	R/W
0x00X7	DSR3 — Data Segment Register 3	R/W
0x00X8	DSR4 — Data Segment Register 4	R/W
0x00X9	DSR5 — Data Segment Register 5	R/W
0x00XA	DSR6 — Data Segment Register 6	R/W
0x00XB	DSR7 — Data Segment Register 7	R/W
0x00XC	DLR — Data Length Register	R/W
0x00XD	TBPR — Transmit Buffer Priority Register(1)	R/W
0x00XE	TSRH — Time Stamp Register (High Byte)	R
0x00XF	TSRL — Time Stamp Register (Low Byte)	R

1. Not applicable for receive buffers

Figure 13-24 shows the common 13-byte data structure of receive and transmit buffers for extended identifiers. The mapping of standard identifiers into the IDR registers is shown in Figure 13-25.

All bits of the receive and transmit buffers are ‘x’ out of reset because of RAM-based implementation[1]. All reserved or unused bits of the receive and transmit buffers always read ‘x’.

1. Exception: The transmit buffer priority registers are 0 out of reset.

14.3.2.18 PTU Debug Register (PTUDEBUG)

Module Base + 0x001F — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	PTUREPE	PTUT1PE	PTUT0PE	0	0	0	0
W						PTUFRE	TG1FTE	TG0FTE
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-21. PTU Debug Register (PTUDEBUG)

1. Read: Anytime
   Write: only in special mode

Table 14-21. PTUDEBUG Register Field Descriptions

Field	Description
6 PTUREPE	**PTURE Pin Enable** — This bit enables the output port for pin PTURE. 0 PTURE output port are disabled 1 PTURE output port are enabled
5 PTUT1PE	**PTU PTUT1 Pin Enable** — This bit enables the output port for pin PTUT1. 0 PTUT1 output port are disabled 1 PTUT1 output port are enabled
4 PTUT0PE	**PTU PTUT0 Pin Enable** — This bit enables the output port for pin PTUT0. 0 PTUT0 output port are disabled 1 PTUT0 output port are enabled
2 PTUFRE	Force Reload event generation — If one of the TGs is enabled then writing 1 to this bit will generate a reload event. The reload event forced by PTUFRE does not set the PTUROIF interrupt flag. Also the ptu_reload signal asserts for one bus clock cyclet. Writing 0 to this bit has no effect. Always reads back as 0. This behavior is not available during stop or freeze mode.
1 TG1FTE	**Trigger Generator 1 Force Trigger Event** — If TG1 is enabled then writing 1 to this bit will generate a trigger event independent on the list based trigger generation. Writing 0 to this bit has no effect. Always reads back as 0.This behavior is not available during stop or freeze mode.
0 TG0FTE	**Trigger Generator 0 Force Trigger Event** — If TG0 is enabled then writing 1 to this bit will generate a trigger event independent on the list based trigger generation. Writing 0 to this bit has no effect. Always reads back as 0. This behavior is not available during stop or freeze mode.

14.4 Functional Description

14.4.1 General

The PTU module consists of two trigger generators (TG0 and TG1). For each TG a separate enable bit is available, so that both TGs can be enabled independently.

If both trigger generators are disabled then the PTU is disabled, the trigger generation stops and the memory accesses are disabled.

15.4.2 Prescaler

To permit lower PWM frequencies, the prescaler produces the PWM clock frequency by dividing the core clock frequency by one, two, four, and eight. Each PWM generator has its own prescaler divisor. Each prescaler is buffered and will not be used by its PWM generator until the corresponding Load OK bit is set and a new PWM reload cycle begins.

15.4.3 PWM Generator

Each PWM generator contains a 15-bit up/down PWM counter producing output signals with software-selectable

- Alignment — The logic state of each pair EDGE bit determines whether the PWM pair outputs are edge-aligned or center-aligned
- Period — The value written to each pair PWM counter modulo register is used to determine the PWM pair period. The period can also be varied by using the prescaler
- With edge-aligned output, the modulus is the period of the PWM output in clock cycles
- With center-aligned output, the modulus is one-half of the PWM output period in clock cycles
- Pulse width — The number written to the PWM value register determines the pulse width duty cycle of the PWM output in clock cycles
  - — With center-aligned output, the pulse width is twice the value written to the PWM value register
  - — With edge-aligned output, the pulse width is the value written to the PWM value register

15.4.3.1 Alignment and Compare Output Polarity

Each edge-align bit, EDGEx, selects either center-aligned or edge-aligned PWM generator outputs.

PWM compare output polarity is selected by the CINV*n* bit field in the source control (PMFCINV) register. Please see the output operations in Figure 15-42 and Figure 15-43.

The PWM compare output is driven to a high state when the value of PWM value (PMFVAL*n*) register is greater than the value of PWM counter, and PWM compare is counting downwards if the corresponding channel CINV*n*=0. Or, the PWM compare output is driven to low state if the corresponding channel CINV*n*=1.

The PWM compare output is driven to low state when the value of PWM value (PMFVAL*n*) register matches the value of PWM counter, and PWM counter is counting upwards if the corresponding channel CINV*n*=0. Or, the PWM compare output is driven to high state if the corresponding channel CINV*n*=1.

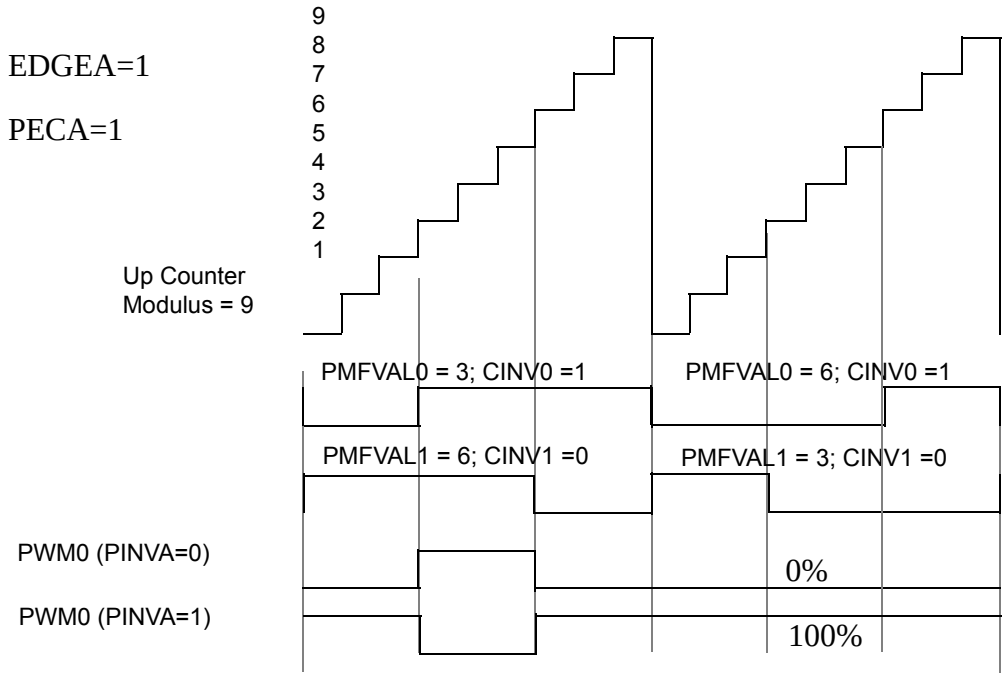
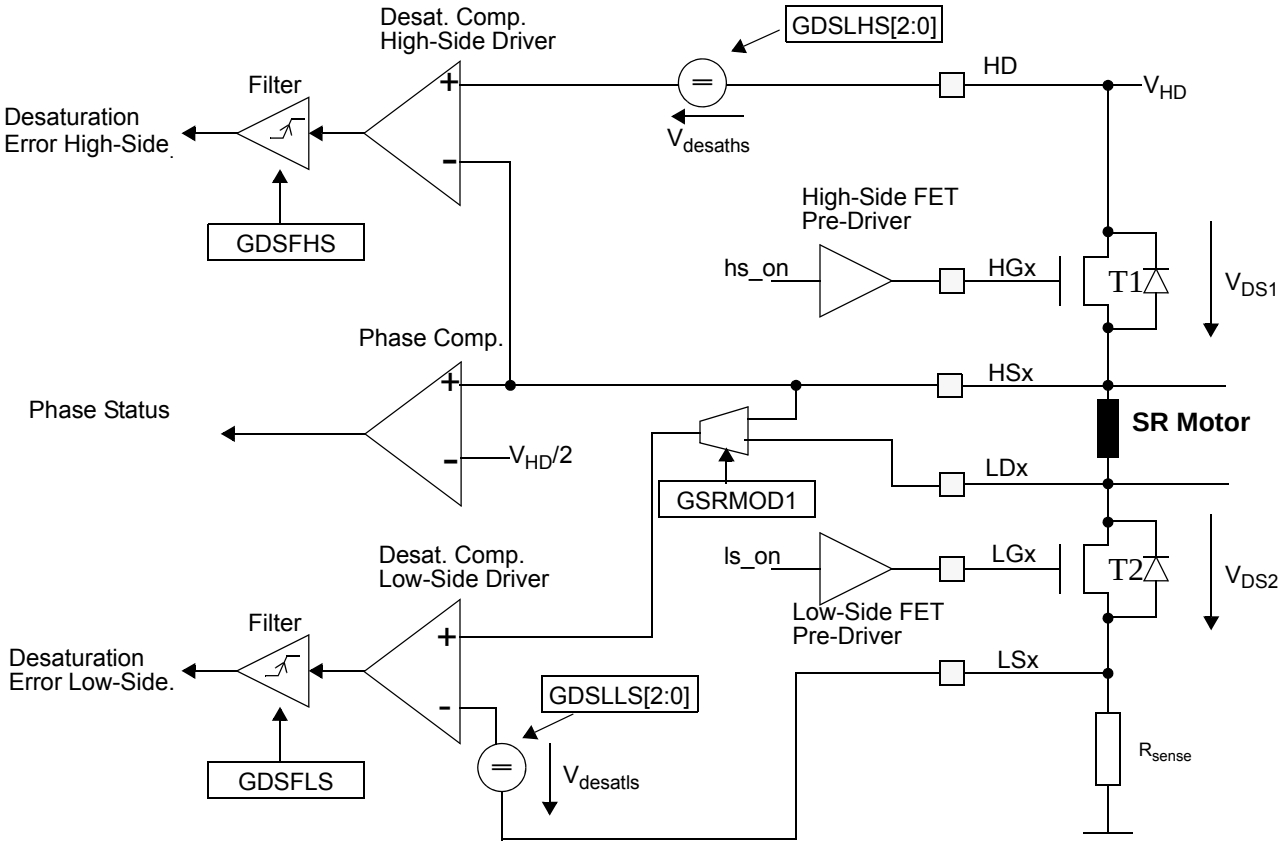


Figure 15-64. Variable Edge Placement Waveform - Phase Shift PWM Output (Edge-Aligned)

15.4.9 Double Switching PWM Output

By using the AND function in Figure 15-63 in complementary center-aligned mode, the PWM output can be configured for double switching operation (Figure 15-65, Figure 15-66). By setting the non-inverted value register greater or equal to the PWM modulus the output function can be switched to single pulse generation on PWM reload cycle basis.

Figure 18-24. Desaturation Comparators and Phase Comparators in SR mode (LDx connected)[1]



18.4.6 Phase Comparators

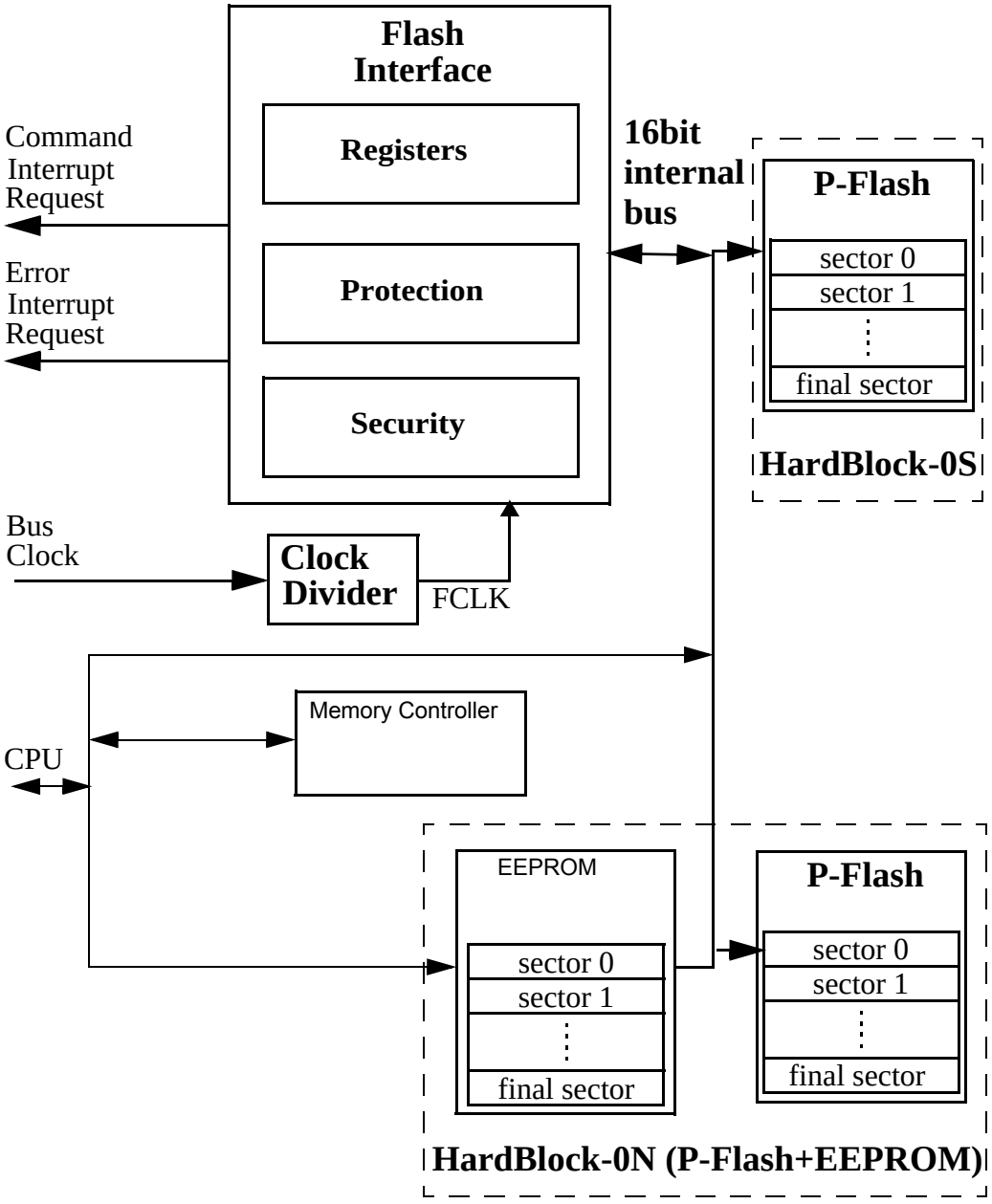
The GDU module includes three phase comparators. The phase comparators compares the voltage on the HS[2:0] pins with one half voltage on HD pin. If V_{HSx} is greater than 0.5 V_{HD} the associated phase status bit GPHS[2:0] is set. (see Figure 18-7) If the V_{HSx} is less than 0.5 V_{HD} the associated phase status bit GPHS[2:0] is cleared. If a desaturation error is detected the state of the phase status bit GPHS[2:0] are copied to the GDUPHL register. The phase flags get unlocked when the associated desaturation interrupt flag is cleared.

1. LDx pins and the routing option of HSx or LDx to the desaturation comparator of the low-side driver controlled by GSRMOD1 is only available on GDUV6.

NOTE

Since all MOSFET transistors are turned off, VBSX can reach phase voltage plus bootstrap voltage which may exceed allowable levels during high supply voltage conditions. If such operating condition exist the application must make sure that VBSX levels are clamped below maximum ratings for example by using clamping diodes.

Table 20-2. FTMRZ Block Diagram (Two P-Flash blocks plus EEPROM block)



20.2 External Signal Description

The Flash module contains no signals that connect off-chip.

Offset Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	CCIE	0	ERSAREQ	IGNSF	WSTAT[1:0]		FDFD	FSFD
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-9. Flash Configuration Register (FCNFG)

CCIE, IGNSF, WSTAT, FDFD, and FSFD bits are readable and writable, ERSAREQ bit is read only, and remaining bits read 0 and are not writable.

Table 20-14. FCNFG Field Descriptions

Field	Description
7 CCIE	**Command Complete Interrupt Enable** — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 20.3.2.7)
5 ERSAREQ	**Erase All Request** — Requests the Memory Controller to execute the Erase All Blocks command and release security. ERSAREQ is not directly writable but is under indirect user control. Refer to the Reference Manual for assertion of the *soc_erase_all_req* input to the FTMRZ module. 0 No request or request complete 1 Request to: a) run the Erase All Blocks command b) verify the erased state c) program the security byte in the Flash Configuration Field to the unsecure state d) release MCU security by setting the SEC field of the FSEC register to the unsecure state as defined in Table 20-9 of Section 20.3.2.2. The ERSAREQ bit sets to 1 when *soc_erase_all_req* is asserted, CCIF=1 and the Memory Controller starts executing the sequence. ERSAREQ will be reset to 0 by the Memory Controller when the operation is completed (see Section 20.4.7.7.1).
4 IGNSF	**Ignore Single Bit Fault** — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 20.3.2.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
3–2 WSTAT[1:0]	**Wait State control bits** — The WSTAT[1:0] bits define how many wait-states are inserted on each read access to the Flash as shown on Table 20-15.Right after reset the maximum amount of wait-states is set, to be later re-configured by the application if needed. Depending on the system operating frequency being used the number of wait-states can be reduced or disabled, please refer to the Data Sheet for details. For additional information regarding the procedure to change this configuration please see Section 20.4.3. The WSTAT[1:0] bits should not be updated while the Flash is executing a command (CCIF=0); if that happens the value of this field will not change and no action will take place.

4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 20-54. Verify Backdoor Access Key Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0C	Not required
FCCOB1	Key 0	
FCCOB2	Key 1	
FCCOB3	Key 2	
FCCOB4	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0xFF_FE00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 20-55. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 20.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

20.4.7.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 20-56. Set User Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0D	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x011C	DBGADM0	R W	Bit 31	30	29	28	27	26	25	Bit 24
0x011D	DBGADM1	R W	Bit 23	22	21	20	19	18	17	Bit 16
0x011E	DBGADM2	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x011F	DBGADM3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0120	DBGBCTL	R W	0	0	INST	0	RW	RWE	reserved	COMPE
0x0121- 0x0124	Reserved	R W	0	0	0	0	0	0	0	0
0x0125	DBGBAH	R W	DBGBA[23:16]							
0x0126	DBGBAM	R W	DBGBA[15:8]							
0x0127	DBGBAL	R W	DBGBA[7:0]							
0x0128- 0x012F	Reserved	R W	0	0	0	0	0	0	0	0
0x0130	DBGCCTL2	R W	0	NDB	INST	0	RW	RWE	reserved	COMPE
0x0131- 0x0134	Reserved	R W	0	0	0	0	0	0	0	0
0x0135	DBGCAH2	R W	DBGCA[23:16]							
0x0136	DBGCAM2	R W	DBGCA[15:8]							
0x0137	DBGCAL2	R W	DBGCA[7:0]							
0x0138	DBGCD02	R W	Bit 31	30	29	28	27	26	25	Bit 24
0x0139	DBGCD12	R W	Bit 23	22	21	20	19	18	17	Bit 16
0x013A	DBGCD22	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x013B	DBGCD32	R W	Bit 7	6	5	4	3	2	1	Bit 0