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Details

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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f3vkh

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Table 0-1. Revision History

Date	Revision	Description
19 APR 2016	2.8	Added PAD pin leakage specification at 125°C Table A-12 Updated t_{HGON} , t_{HGOFF} parameter values Table E-1 Specified VRH drop when using VDDS1 or VDDS2 as VRH on ZVMC256 Section C.1.1.5 Added min. and max. desaturation comparator filter times to electrical spec. Table E-1 Updated 64LQFP-EP thermal parameters Table A-9, Table A-10
06 JUN 2016	2.9	Fixed corrupted symbol fonts Table A-3, Table A-5 Corrected wrong IFR reference Section 20.3.2.10 Clarified PAD8 leakage better Table A-12 Added I _{SUPR} and I _{SUPW} maximum values at T _J = 175°C for ZVMC256 Table A-18 Added Pseudo STOP maximum current for ZVMC256 Table A-20 Removed bandgap temperature dependency footnote, Table B-1 Changed ZVMC256 SNPS monitor threshold min/max values Table B-2 Changed VLS current limit threshold to 112mA Table E-1, Table E-2 Removed desaturation comparator filter times from GDU chapter. Added desaturation comparator levels to Table E-1, Table E-2 Added low side desaturation comparator functional range as footnote Table E-1, Table E-2
29 JUN 2016	2.10	Updated GDU VBS filter Figure 18-20 Removed incorrect reference to temperature sensor influencing GDU outputs Section 1.13.3.4 Changed Stop IDD (ISUPS) specifications for ZVMC256 Table A-19
28 OCT 2016	2.11	Added IOC0 signal mapping to 48LQFP package Figure 1-6 Fixed corrupted symbol fonts in PIM chapter Added diode to VDDC pin Figure 1-18 Updated Stop mode current ISUPS maximum values Table A-19 Updated tdelon, tdeloff values Table E-1

1.4.12 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.4.13 Analog-to-Digital Converter Module (ADC)

- Dual ADC
 - 12-bit resolution
 - Up to 16 external channels & 8 internal channels
 - 2.5us for single 12-bit resolution conversion
 - Left or right aligned result data
 - Continuous conversion mode
- Programmers model with list based command and result storage architecture ADC directly writes results to RAM, preventing stall of further conversions
- Internal signals monitored with the ADC module
 - VRH, VRL, (VRL+VRH)/2, Vsup monitor, Vbg, TempSense, GDU phase, GDU DC-link
- External pins can also be used as digital I/O

1.4.14 Supply Voltage Sensor (BATS)

- Monitoring of supply (VSUP) voltage
- Internal ADC interface from an internal resistive divider
- Generation of low or high voltage interrupts

1.4.15 On-Chip Voltage Regulator system (VREG)

- Voltage regulator
 - Linear voltage regulator directly supplied by VSUP
 - Low-voltage detect on VSUP
 - Power-on reset (POR)
 - Low-voltage reset (LVR) for VDDX domain
 - External ballast device support to reduce internal power dissipation
 - Capable of supplying both the MCU internally plus external components
 - Over-temperature interrupt
- Internal voltage regulator
 - Linear voltage regulator with bandgap reference

Chapter 1 Device Overview MC9S12ZVM-Family



Figure 1-13. BDCM Complementary Mode Waveform

Assuming first quadrant operation, forward accelerating operation, the applied voltage at node A must exceed the applied voltage at node B (Figure 1-11). Thus the PWM0_0 duty cycle must exceed the PWM0_2 duty cycle.

The duty cycle of PWM0_0 defines the voltage at the first power stage branch.

The duty cycle of PWM0_2 defines the voltage at the second power stage branch.

Modulating the duty cycle every period using the function F_{PWM} then the duty cycle is expressed as:

 $PWM0_0 \text{ duty-cycle} = 0.5 + (0.5 * F_{PWM}); \text{ For -1} <= F_{PWM} <= 1;$

 $PWM0_2 \text{ duty-cycle} = 0.5 - (0.5 * F_{PWM})$

2.3.3.2 Port Input Register



1. Read: Anytime

Write:Never

This is a generic description of the standard port input registers. Refer to Table 2-39 to determine the

implemented bits in the respective register. Unimplemented bits read zero.

Table 2-18.	Port Input	Register Field	Descriptions
-------------	------------	-----------------------	--------------

Field	Description
7-0 PTIx7-0	Port Input — Data input
	A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.3.3 Data Direction Register



1. Read: Anytime Write: Anytime



This is a generic description of the standard data direction registers. Refer to Table 2-39 to determine the implemented bits in the respective register. Unimplemented bits read zero.

STOP Mode With BDC Enabled And BDCCIS Set

If the BDC is enabled and BDCCIS is set, then the BDC prevents core clocks being disabled in stop mode. This allows BDC communication, for access of internal memory mapped resources, but not CPU registers, to continue throughout stop mode.

A BACKGROUND command issued whilst in stop mode remains pending internally until the device leaves stop mode. This means that subsequent active BDM commands, issued whilst BACKGROUND is pending, set the ILLCMD flag because the device is not yet in active BDM.

If ACK handshaking is enabled, then the first ACK, following a stop mode entry is long to indicate a stop exception. The BDC indicates a stop mode occurrence by setting the BDCCSR bit STOP. If the host attempts further communication before the ACK pulse generation then the OVRUN bit is set.

5.1.3.3.2 Wait Mode

The device enters wait mode when the CPU starts to execute the WAI instruction. The second part of the WAI instruction (return from wait mode) can only be performed when an interrupt occurs. Thus on entering wait mode the CPU is in the middle of the WAI instruction and cannot permit access to CPU internal resources, nor allow entry to active BDM. Thus only commands classified as Non-Intrusive or Always-Available are possible in wait mode.

On entering wait mode, the WAIT flag in BDCCSR is set. If the ACK handshake protocol is enabled then the first ACK generated after WAIT has been set is a long-ACK pulse. Thus the host can recognize a wait mode occurrence. The WAIT flag remains set and cannot be cleared whilst the device remains in wait mode. After the device leaves wait mode the WAIT flag can be cleared by writing a "1" to it.

A BACKGROUND command issued whilst in wait mode sets the NORESP bit and the BDM active request remains pending internally until the CPU leaves wait mode due to an interrupt. The device then enters BDM with the PC pointing to the address of the first instruction of the ISR.

With ACK disabled, further Non-Intrusive or Always-Available commands are possible, in this pending state, but attempted Active-Background commands set NORESP and ILLCMD because the BDC is not in active BDM state.

With ACK enabled, if the host attempts further communication before the ACK pulse generation then the OVRUN bit is set.

Similarly the STEP1 command issued from a WAI instruction cannot be completed by the CPU until the CPU leaves wait mode due to an interrupt. The first STEP1 into wait mode sets the BDCCSR WAIT bit.

If the part is still in Wait mode and a further STEP1 is carried out then the NORESP and ILLCMD bits are set because the device is no longer in active BDM for the duration of WAI execution.

5.1.4 Block Diagram

A block diagram of the BDC is shown in Figure 5-1.



FILL_MEM.sz_WS

FILL_MEM{_WS} is used with the WRITE_MEM{_WS} command to access large blocks of memory. An initial WRITE_MEM{_WS} is executed to set up the starting address of the block and write the first datum. If an initial WRITE_MEM{_WS} is not executed before the first FILL_MEM{_WS}, an illegal command response is returned. The FILL_MEM{_WS} command stores subsequent operands. The initial address is incremented by the operand size (1, 2, or 4) and saved in a temporary register. Subsequent FILL_MEM{_WS} commands use this address, perform the memory write, increment it by the current operand size, and store the updated address in the temporary register. If the with-status option is specified, the BDCCSRL status byte is returned after the write data. This status byte reflects the state after the memory write was performed. If enabled an ACK pulse is generated after the internal write access has been completed or aborted. The effect of the access size and alignment on the next address to be accessed is explained in more detail in Section 5.4.5.2"

NOTE

FILL_MEM{_WS} is a valid command only when preceded by SYNC, NOP, WRITE_MEM{_WS}, or another FILL_MEM{_WS} command. Otherwise, an illegal command response is returned, setting the ILLCMD bit. NOP can be used for inter command padding without corrupting the address pointer.

The size field (sz) is examined each time a FILL_MEM{_WS} command is processed, allowing the operand size to be dynamically altered. The examples show the FILL_MEM.B{_WS}, FILL_MEM.W{_WS} and FILL_MEM.L{_WS} commands.

5.4.4.7 GO



Non-intrusive

- When a reset occurs the debugger pulls BKGD low until the reset ends, forcing SSC mode entry.
- Then the debugger reads the reset flags to determine the cause of reset.
- If required, the debugger can read the trace buffer to see what happened just before reset. Since the trace buffer and DBGCNT register are not affected by resets other than POR.
- The debugger configures and arms the DBG to start tracing on returning to application code.
- The debugger then sets the PC according to the reset flags.
- Then the debugger returns to user code with GO or STEP1.

6.5.3 Breakpoints from other S12Z sources

The DBG is neither affected by CPU BGND instructions, nor by BDC BACKGROUND commands.

6.5.4 Code Profiling

The code profiling data output pin PDO is mapped to a device pin that can also be used as GPIO in an application. If profiling is required and all pins are required in the application, it is recommended to use the device pin for a simple output function in the application, without feedback to the chip. In this way the application can still be profiled, since the pin has no effect on code flow.

The PDO provides a simple bit stream that must be strobed at both edges of the profiling clock when profiling. The external development tool activates profiling by setting the DBG ARM bit, with PROFILE and PDOE already set. Thereafter the first bit of the profiling bit stream is valid at the first rising edge of the profiling clock. No start bit is provided. The external development tool must detect this first rising edge after arming the DBG. To detect the end of profiling, the DBG ARM bit can be monitored using the BDC.

Field	Description				
7 WCOP	 Window COP Mode Bit — When set, a write to the CPMUARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period generates a COP reset. As long as all writes occur during this window, \$55 can be written as often as desired. Once \$AA is written after the \$55, the time-out logic restarts and the user must wait until the next window before writing to CPMUARMCOP. Table 8-15 shows the duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation 				
6 RSBCK	COP and RTI Stop in Active BDM Mode Bit 0 Allows the COP and RTI to keep running in Active BDM mode. 1 Stops the COP and RTI counters whenever the part is in Active BDM mode.				
5 WRTMASK	 Write Mask for WCOP and CR[2:0] Bit — This write-only bit serves as a mask for the WCOP and CR[2:0] bits while writing the CPMUCOP register. It is intended for BDM writing the RSBCK without changing the content of WCOP and CR[2:0]. Write of WCOP and CR[2:0] has an effect with this write of CPMUCOP Write of WCOP and CR[2:0] has no effect with this write of CPMUCOP. (Does not count for "write once".) 				
2–0 CR[2:0]	 COP Watchdog Timer Rate Select — These bits select the COP time-out rate (see Table 8-15 and Table 8-16). Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a System Reset. This can be avoided by periodically (before time-out) initializing the COP counter via the CPMUARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest time-out period (2²⁴ cycles) in normal COP mode (Window COP mode disabled): COP is enabled (CR[2:0] is not 000) BDM mode active RSBCK = 0 Operation in Special Mode 				

Table 8-14. CPMUCOP Field Descriptions

Table 8-15. COP Watchdog Rates if COPOSCSEL1=0. (default out of reset)

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is either IRCCLK or OSCCLK depending on the COPOSCSEL0 bit)	
0	0	0	COP disabled	
0	0	1	2 ¹⁴	
0	1	0	2 ¹⁶	
0	1	1	2 ¹⁸	
1	0	0	2 ²⁰	
1	0	1	2 ²²	
1	1	0	2 ²³	
1	1	1	2 ²⁴	

Chapter 8 S12 Clock, Reset and Power Management Unit (V10 and V6)

8.4.3 Stop Mode using PLLCLK as source of the Bus Clock

An example of what happens going into Stop Mode and exiting Stop Mode after an interrupt is shown in Figure 8-42. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop Mode.



Depending on the COP configuration there might be an additional significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

8.4.4 Full Stop Mode using Oscillator Clock as source of the Bus Clock

An example of what happens going into Full Stop Mode and exiting Full Stop Mode after an interrupt is shown in Figure 8-43.

Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop Mode.

Field	Description
5 TSFRZ	 Timer Stops While in Freeze Mode Allows the timer counter to continue running while in freeze mode. Disables the timer counter whenever the MCU is in freeze mode. This is useful for emulation. TSFRZ does not stop the pulse accumulator.
4 TFFCA	 Timer Fast Flag Clear All Allows the timer flag clearing to function normally. For TFLG1(0x000E), a read from an input capture or a write to the output compare channel (0x0010–0x001F) causes the corresponding channel flag, CnF, to be cleared. For TFLG2 (0x000F), any access to the TCNT register (0x0004, 0x0005) clears the TOF flag. This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses.
3 PRNT	 Precision Timer 0 Enables legacy timer. PR0, PR1, and PR2 bits of the TSCR2 register are used for timer counter prescaler selection. 1 Enables precision timer. All bits of the PTPSR register are used for Precision Timer Prescaler Selection, and all bits. This bit is writable only once out of reset.

12.3.2.5 Timer Toggle On Overflow Register 1 (TTOV)

Module Base + 0x0007



Figure 12-9. Timer Toggle On Overflow Register 1 (TTOV)

Read: Anytime

Write: Anytime

Table 12-5. TTOV Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
1:0 TOV[1:0]	 Toggle On Overflow Bits — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.

Field	Description
7-0 AM[7:0]	 Acceptance Mask Bits — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F

Access: User read/write⁽¹⁾

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 13-23. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

1. Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	 Acceptance Mask Bits — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

13.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 13.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

14.3.2.7 Trigger Generator 0 List Register (TG0LIST)



1. Read: Anytime

Write: Anytime, if TG0EN bit is cleared

Table 14-9. TG0LIST Register Field Descriptions

Field	Description
0 TG0LIST	 Trigger Generator 0 List — This bit shows the number of the current used list. 0 Trigger generator 0 is using list 0 1 Trigger generator 0 is using list 1

14.3.2.8 Trigger Generator 0 Trigger Number Register (TG0TNUM)



1. Read: Anytime

Write: Never

Table 14-10. TG0TNUM Register Field Descriptions

Field	Description
4:0 TG0TNUM[4:0]	Trigger Generator 0 Trigger Number — This register shows the number of generated triggers since the last reload event. After the generation of 32 triggers this register shows zero. The next reload event clears this register. See also Figure 14-22.

Figure 15-23. PMF Compare Invert Register (PMFCINV) Descriptions (continued)

Field	Description
1 CINV1	 PWM Compare Invert 1 — This bit controls the polarity of PWM compare output 1. Please see the output operations in Figure 15-42 and Figure 15-43. 0 PWM output 1 is high when PMFCNTA is less than PMFVAL1 1 PWM output 1 is high when PMFCNTA is greater than PMFVAL1.
0 CINV0	 PWM Compare Invert 0 — This bit controls the polarity of PWM compare output 0. Please see the output operations in Figure 15-42 and Figure 15-43. 0 PWM output 0 is high when PMFCNTA is less than PMFVAL0. 1 PWM output 0 is high when PMFCNTA is greater than PMFVAL0

NOTE

Changing CINVn can affect the present PWM cycle, if the related PMFVALn is zero.

15.3.2.19 PMF Enable Control A Register (PMFENCA)

Address: Module Base + 0x0020

Access: User read/write⁽¹⁾

_	7	6	5	4	3	2	1	0	
R			0 0 0		0	RSTRTA		PWMRIFA	
W		GLDONA				NOTIVIA	LDONA		
Reset	0	0	0	0	0	0	0	0	

Figure 15-24. PMF Enable Control A Register (PMFENCA)

1. Read: Anytime

Write: Anytime except GLDOKA and RSTRTA which cannot be modified after the WP bit is set.

Table 15-25. PMFENCA Field Descriptions

Field	Description
7 PWMENA	 PWM Generator A Enable — When MTG is clear, this bit when set enables the PWM generators A, B and C and PWM0–5 outputs. When PWMENA is clear, PWM generators A, B and C are disabled, and the PWM0–5 outputs are in their inactive states unless the corresponding OUTCTL bits are set. When MTG is set, this bit when set enables the PWM generator A and the PWM0 and PWM1 outputs. When PWMENA is clear, the PWM generator A is disabled and PWM0 and PWM1 outputs are in their inactive states unless the OUTCTL0 and OUTCTL1 bits are set. After setting this bit a reload event is generated at the beginning of the PWM cycle. PWM generator A and PWM0-1 (2–5 if MTG = 0) outputs disabled unless the respective OUTCTL bit is set 1 PWM generator A and PWM0-1 (2–5 if MTG = 0) outputs enabled
6 GLDOKA	 Global Load Okay A — When this bit is set, a PMF external global load OK defined on device level replaces the function of LDOKA. This bit cannot be modified after the WP bit is set. 0 LDOKA controls reload of double buffered registers 1 PMF external global load OK controls reload of double buffered registers
2 RSTRTA	 Restart Generator A — When this bit is set, PWM generator A will be restarted at the next commutation event. This bit cannot be modified after the WP bit is set. No PWM generator A restart at the next commutation event. PWM generator A restarts at the next commutation event.



Figure 15-85. Manual Fault Recovery (Faults 0 and 2) - QSMP = 01, 10, or 11



Figure 15-86. Manual Fault Recovery (Faults 1 and 3-5)

NOTE

PWM half-cycle boundaries occur at both the PWM cycle start and when the counter equals the modulus, so in edge-aligned operation full-cycles and half-cycles are equal.

NOTE

Fault protection also applies during software output control when the OUTCTL*n* bits are set. Fault recovery still occurs at half PWM cycle boundaries while the PWM generator is engaged, PWMEN equals one. But the OUT*n* bits can control the PWM outputs while the PWM generator is off, PWMEN equals zero. Thus, fault recovery occurs at IPbus cycles while the PWM generator is off and at the start of PWM cycles when the generator is engaged.

15.5 Resets

All PMF registers are reset to their default values upon any system reset.

15.6 Clocks

The gated system core clock is the clock source for all PWM generators. The system clock is used as a clock source for any other logic in this module. The system bus clock is used as clock for specific control registers and flags (LDOK*x*, PWMRF*x*, PMFOUTB).

NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
- 4 dimension to be determined at seating plane C.
- 5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
- A THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
- /7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- AND 0.25MM FROM THE LEAD TIP.
- /9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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TITLE: LQFP, 7 X 7 X 1	DOCUMENT NO: 98ASA00945D REV: X0				
0.5 PITCH, 48	STANDARD: NON-JEDEC				
4.4 X 4.4 EXPOS		02	NOV 2015		

Appendix L Ordering Information

Customers can choose either the mask-specific partnumber or the generic, mask-independent partnumber. Ordering a mask-specific partnumber enables the customer to specify which particular maskset they receive whereas ordering the generic partnumber means that the currently preferred maskset (which may change over time) is shipped. In either case, the marking on the device always shows the generic, mask-independent partnumber and the mask set number. The below figure illustrates the structure of a typical mask-specific ordering number.

NOTES



P or PC = prototype status (pre qualification)

Appendix M Detailed Register Address Map

M.2 0x0010-0x001F S12ZINT Address Name Bit 7 6 5 4 3 2 1 Bit 0 0x001F INT_CFDATA7 R 0 0 0 0 0 PRIOLVL[2:0]

Appendix M Detailed Register Address Map

M.3 0x0070-0x00FF S12ZMMC

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0				
0x0070	MODE	R	MODC	0	0	0	0	0	0	0				
		W												
0x0071-	Reserved	R	0	0	0	0	0	0	0	0				
0x007F		W												
0x0080	MMCECH	R W		ITR[3	3:0]			TGT	[3:0]					
0x0081	MMCECL	R W		ACC[3:0]			ERR	[3:0]					
0x0082	MMCCCRH	R	CPUU	0	0	0	0	0	0	0				
		w												
0x0083	MMCCCRL	R	0	CPUX	0	CPUI	0	0	0	0				
		W												
		_[
0x0084	Reserved	R	0	0	0	0	0	0	0	0				
		"L												
0x0085	MMCPCH	MMCPCH	5 MMCPCH	5 MMCPCH	MMCPCH	R				CPUPC[23:	16]			
		vv												
0x0086	MMCPCM	R				CPUPC[15	:8]							
		w												
0x0087	MMCPCL	R				CPUPC[7:	0]							
		W												
0x0088-	Reserved	R	0	0	0	0	0	0	0	0				
UXUUFF		W												

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0100	DBGC1	R W	ARM	0 TRIG	reserved	BDMBP	BRKCPU	reserved	EEVE1	EEVE0 ²
0v0101	DBGC2	R R		0	0	0				
0.00101		W					CDCIVI		ADUM	
		-								
0x0102	02 DBGTCRH F		reserved	TSOURCE	TRA	NGE	TRCMOD		TAL	IGN

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0	
0x0529	PMFFQCB	R W	LDFQB HALFB PRSCB					SCB	PWMRFB		
0x052A	PMFCNTB	R W	0	0 PMFCNTB							
0x052B	PMFCNTB	R W				PMFC	CNTB				
0x052C	PMFMODB	R W	0				PMFMODB				
0x052D	PMFMODB	R W				PMFN	IODB				
0x052E	PMFDTMB	R W	0	0	0	0		PMF	DTMB		
0x052F	PMFDTMB	R W		PMFDTMB							
0x0530	PMFENCC	R W	PWMENC	GLDOKC	0	0	0	RSTRTC	LDOKC	PWMRIEC	
0x0531	PMFFQCC	R W		LDF	QC		HALFC PRSCC PWMRFC			PWMRFC	
0x0532	PMFCNTC	R W	0				PMFCNTC				
0x0533	PMFCNTC	R W				PMFC	CNTC				
0x0534	PMFMODC	R W	0				PMFMODC				
0x0535	PMFMODC	R W				PMFN	NODC				
0x0536	PMFDTMC	R W	0	0	0	0		PMFD	DTMC		
0x0537	PMFDTMC	R W				PMFD	DTMC				
0x0538	PMFDMP0	R W	DM	P05	DM	P04	DMP03	DMP02	DMP01	DMP00	
0x0539	PMFDMP1	R W	DM	P15	DM	P14	DMP13	DMP12	DMP11	DMP10	

Appendix M Detailed Register Address Map

M.15 0x06A0-0x06BF GDU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0	
0x06A0	GDUE	R W	GWP	0	0	GCS1E	GBOE	GCS0E	GCPE	GFDE	
0x06A1	GDUCTR	R W	GHHDLVL	GVLSLVL		GBKTI	M2[3:0]		GBKTI	W1[1:0]	
0x06A2	GDUIE	R W	0	0	0	GOCI	E[1:0]	GDSEIE	GHHDIE	GLVLSIE	
0x06A3	GDUDSE	R W	0		GDHSIF[2:0]]	0		GDLSIF[2:0]		
0x06A4	GDUSTAT	R W		GPHS[2:0]		GOC	S[1:0]		GHHDS	GLVLSS	
0x06A5	GDUSRC	R W	0	(GSRCHS[2:0)]	0	(GSRCLS[2:0]		
0x06A6	GDUF	R W	GSUF	GHHDF	GLVLSF	GOCI	F[1:0]	0	GHHDIF	GLVLSIF	
0x06A7	GDUCLK1	R W	0	GBOCD[4:0]			GBODC[1:0]			PC[1:0]	
0x06A8	GDUBCL	R W	0	0	0	0	GBCL[3:0]				
0x06A9	GDUPHMUX	R W	0	0	0	0	0	0	0 GPHMX[1:0]		
0x06AA	GDUCSO	R W	0		GCSO1[2:0]		0		GCSO0[2:0]		
0x06AB	GDUDSLVL	R W	GDSFHS ¹	(GDSLHS[2:0]	GDSFLS ¹	(GDSLLS[2:0]	
0x06AC	GDUPHL	R W	0	0	0	0	0		GPHL[2:0]		
0x06AD	GDUCLK2	R W	0	0	0	0		GCPC	:D[3:0]		
0x06AE	GDUOC0	R W	GOCA0	GOCE0	0		GOCT0[4:0] ⁽²⁾				
0x06AF	GDUOC1	R W	GOCA1	GOCE1	0		GOCT1[4:0] ⁽³⁾				
0x06B0	GDUCTR1 ⁽⁴⁾	R W	GSRM	OD[1:0]	0	0	0	0	0	TDEL	