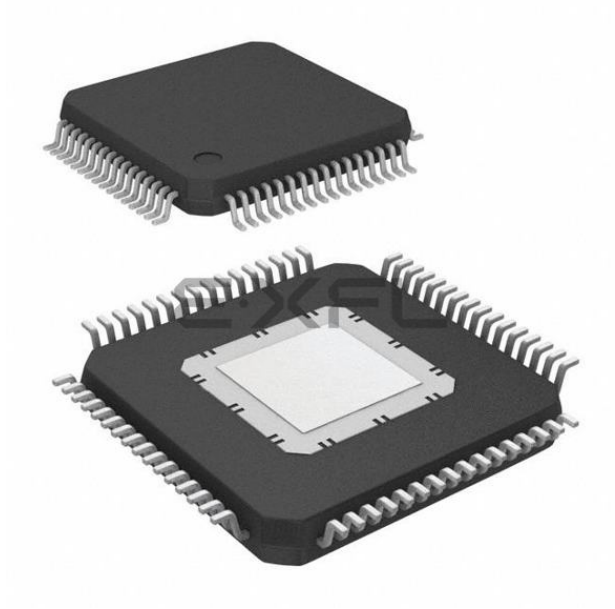

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f3wkh

Table 0-1. Revision History

Date	Revision	Description
19 APR 2016	2.8	Added PAD pin leakage specification at 125°C Table A-12 Updated t_{HGON}, t_{HGOFF} parameter values Table E-1 Specified VRH drop when using VDDS1 or VDDS2 as VRH on ZVMC256 Section C.1.1.5 Added min. and max. desaturation comparator filter times to electrical spec. Table E-1 Updated 64LQFP-EP thermal parameters Table A-9, Table A-10
06 JUN 2016	2.9	Fixed corrupted symbol fonts Table A-3, Table A-5 Corrected wrong IFR reference Section 20.3.2.10 Clarified PAD8 leakage better Table A-12 Added I_{SUPR} and I_{SUPW} maximum values at T_J = 175°C for ZVMC256 Table A-18 Added Pseudo STOP maximum current for ZVMC256 Table A-20 Removed bandgap temperature dependency footnote, Table B-1 Changed ZVMC256 SNPS monitor threshold min/max values Table B-2 Changed VLS current limit threshold to 112mA Table E-1, Table E-2 Removed desaturation comparator filter times from GDU chapter. Added desaturation comparator levels to Table E-1, Table E-2 Added low side desaturation comparator functional range as footnote Table E-1, Table E-2
29 JUN 2016	2.10	Updated GDU VBS filter Figure 18-20 Removed incorrect reference to temperature sensor influencing GDU outputs Section 1.13.3.4 Changed Stop IDD (ISUPS) specifications for ZVMC256 Table A-19
28 OCT 2016	2.11	Added IOC0 signal mapping to 48LQFP package Figure 1-6 Fixed corrupted symbol fonts in PIM chapter Added diode to VDDC pin Figure 1-18 Updated Stop mode current ISUPS maximum values Table A-19 Updated tdelon, tdeloff values Table E-1

Chapter 1
Device Overview MC9S12ZVM-Family

Table 1-1. Revision History

Version Number	Revision Date	Sections Affected	Description of Changes
1.8	04.Sep.2014	Section 1.2.1	• Added S12ZVML31 information to derivative table
2.0	10.Oct.2014	General	• Added ZVMC256 information
2.01	06.Feb.2015	General	• Added 2N95G maskset information. • Added TIM1 for ZVMC256
2.02	25.Aug.2016	Figure 1-6, Table 1-8 Section 1.13.3.6	• Clarified IOC0 device pin mapping dependencies • Clarified IOC0 device pin mapping dependencies • Removed Temperature Sensor from list of Dynamic motor control fault inputs

1.1 Introduction

The MC9S12ZVM-Family is an automotive 16-bit microcontroller family using the NVM + UHV technology that offers the capability to integrate 40 V analog components. This family reuses many features from the existing S12/S12X portfolio. The particular differentiating features of this family are the enhanced S12Z core, the combination of dual-ADC synchronized with PWM generation and the integration of “high-voltage” analog modules, including the voltage regulator (VREG), Gate Drive Unit (GDU), and either Local Interconnect Network (LIN) physical layer or CAN Physical layer. These features enable a fully integrated single chip solution to drive up to 6 external power MOSFETs for BLDC or PMSM motor drive applications.

The MC9S12ZVM-Family includes error correction code (ECC) on RAM and flash memory, EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12ZVM-Family allows the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12ZVM-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of existing S12(X) families. The MC9S12ZVM-Family is available in different pin-out options, using 80-pin, 64-pin and 48-pin LQFP-EP packages to accommodate LIN, CAN and external PWM based application interfaces. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12ZVM-Family is a general-purpose family of devices suitable for a range of applications, including:

- 3-phase sensorless BLDC motor control for
  - — Fuel pump

1.4.12 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.4.13 Analog-to-Digital Converter Module (ADC)

- Dual ADC
  - 12-bit resolution
  - Up to 16 external channels & 8 internal channels
  - 2.5us for single 12-bit resolution conversion
  - Left or right aligned result data
  - Continuous conversion mode
- Programmers model with list based command and result storage architecture
  ADC directly writes results to RAM, preventing stall of further conversions
- Internal signals monitored with the ADC module
  - VRH, VRL, (VRL+VRH)/2, Vsup monitor, Vbg, TempSense, GDU phase, GDU DC-link
- External pins can also be used as digital I/O

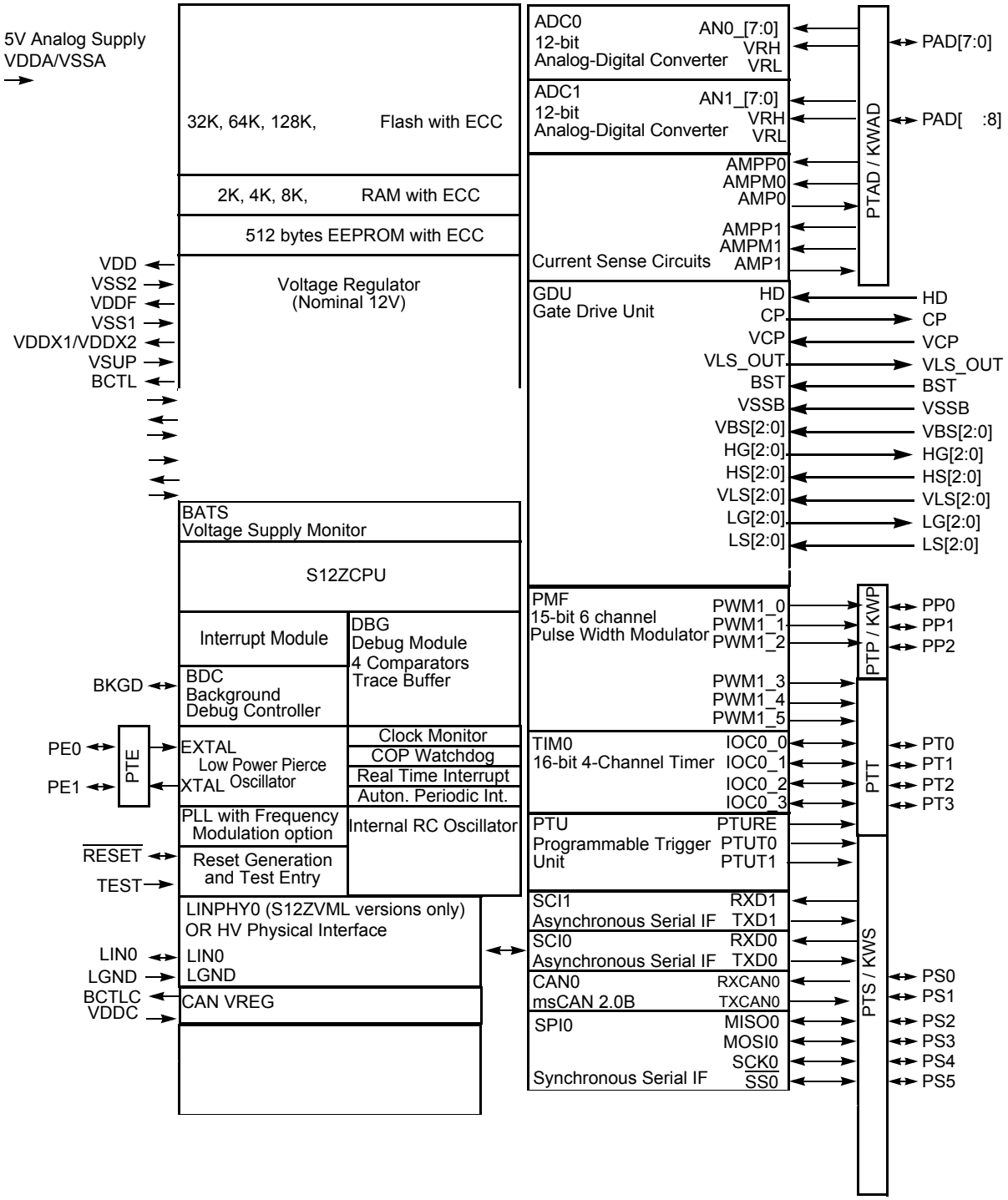
1.4.14 Supply Voltage Sensor (BATS)

- Monitoring of supply (VSUP) voltage
- Internal ADC interface from an internal resistive divider
- Generation of low or high voltage interrupts

1.4.15 On-Chip Voltage Regulator system (VREG)

- Voltage regulator
  - Linear voltage regulator directly supplied by VSUP
  - Low-voltage detect on VSUP
  - Power-on reset (POR)
  - Low-voltage reset (LVR) for VDDX domain
  - External ballast device support to reduce internal power dissipation
  - Capable of supplying both the MCU internally plus external components
  - Over-temperature interrupt
- Internal voltage regulator
  - Linear voltage regulator with bandgap reference

1.5 Block Diagram



Block Diagram shows the maximum configuration
Not all pins or all peripherals are available on all devices and packages.
Rerouting options are not shown.

Figure 1-1. MC9S12ZVM-Family Block Diagram

Table 1-5. Module Register Address Ranges

Address	Module	Size (Bytes)
0x06E0–0x06EF	Reserved	16
0x06F0–0x06F7	BATS	8
0x06F8–0x06FF	Reserved	8
0x0700–0x0707	SCI0	8
0x0708–0x070F	Reserved	8
0x0710–0x0717	SCI1	8
0x0718–0x077F	Reserved	104
0x0780–0x0787	SPI0	8
0x0788–0x07FF	Reserved	120
0x0800–0x083F	CAN0	64
0x0840–0x097F	Reserved	320
0x0980–0x0987	LINPHY (S12ZVML derivatives)	8
0x0980–0x0987	HV Physical Interface (S12ZVM32, S12ZVM16 derivatives)	8
0x0988–0x098F	Reserved	8
0x0990–0x0997	CANPHY (ZVMC256 only)	8
0x0998–0x0FFF	Reserved	1640

1. Reading from the first 16 locations in this reserved range returns undefined data

2. Address range = 0x0690-0x069F on Maskset N06E

NOTE

Reserved register space shown above is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns zero.

1.6.1 Flash Module

This device family instantiates different flash modules, depending on derivative. The flash documentation for the all devices is featured in the FTMRZ section.

1.7.2.16 Timer IOC0_[3:0] Signals

The signals IOC0_[3:0] are associated with the input capture or output compare functionality of the timer (TIM0) module.

1.7.2.17 Timer IOC1_[1:0] Signals (ZVMC256 only)

The signals IOC1_[1:0] are associated with the input capture or output compare functionality of the timer (TIM1) module.

1.7.2.18 PWM1_[5:0] Signals

The signals PWM1_[5:0] are associated with the PMF module digital channel outputs.

1.7.2.19 PWM0_[7,5,3,1] Signals (ZVMC256 only)

The PWM0 signals are associated with the PWM0 module digital channel outputs.

1.7.2.20 PTU Signals

1.7.2.20.1 PTUT[1:0] Signals

These signals are the PTU trigger output signals. These signals are routed to pins for debugging purposes.

1.7.2.20.2 PTURE Signal

This signal is the PTU reload enable output signal. This signal is routed to a pin for debugging purposes.

1.7.2.21 Interrupt Signals — $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$

$\overline{\text{IRQ}}$ is a maskable level or falling edge sensitive input. $\overline{\text{XIRQ}}$ is a non-maskable level-sensitive interrupt.

1.7.2.22 Oscillator and Clock Signals

1.7.2.22.1 Oscillator Pins — EXTAL and XTAL

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the internal PLLCLK, independent of EXTAL and XTAL. XTAL is the oscillator output.

1.7.2.22.2 ECLK

This signal is associated with the output of the bus clock (ECLK).

NOTE

This feature is only intended for debug purposes at room temperature.
It must not be used for clocking external devices in an application.

1.7.2.26.8 VDDC (Only Available On S12ZVMC Versions)

VDDC is the CANPHY supply. This is the output voltage of the external bipolar, whose base current is supplied by BCTLC. It is fed back to the MCU for regulation. On the ZVMC128 a diode is recommended between VDDA and VDDC, whereby the anode is connected to VDDC.

1.7.2.26.9 VSSC (Only Available On ZVMC256)

VSSC is the CANPHY ground.

1.7.2.27 Gate Drive Unit (GDU) Signals

These are associated with driving the external FETs.

1.7.2.27.1 HD — FET Predriver High side Drain Input

This is the drain connection of the external high-side FETs. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC via an analog multiplexer.

1.7.2.27.2 VBS[2:0] - Bootstrap Capacitor Connections

These signals are the bootstrap capacitor connections for phases HS[2:0]. The capacitor connected between HS[2:0] and these signals provides the gate voltage and current to drive the external FET.

1.7.2.27.3 HG[2:0] - High-Side Gate signals

The pins are the gate drives for the three high-side power FETs. The drivers provide a high current with low impedance to turn on and off the high-side power FETs.

1.7.2.27.4 HS[2:0] - High-Side Source signals

The pins are the source connection for the high-side power FETs and the drain connection for the low-side power FETs. The low voltage end of the bootstrap capacitor is also connected to this pin.

1.7.2.27.5 VLS[2:0] - Voltage Supply for Low -Side Drivers

The pins are the voltage supply pins for the three low-side FET pre-drivers. These pins should be connected to the voltage regulator output pin VLS_OUT.

1.7.2.27.6 LG[2:0] - Low-Side Gate signals

The pins are the gate drives for the low-side power FETs. The drivers provide a high current with low impedance to turn on and off the low-side power FETs.

1.7.2.27.7 LS[2:0] - Low-Side Source Signals

The pins are the low-side source connections for the low-side power FETs. The pins are the power ground pins used to return the gate currents from the low-side power FETs.

The exposed pad on the package bottom must be connected to a grounded contact pad on the PCB.

On MC9S12ZVM options the LIN0 pin is mapped to the HV physical interface function

IOC0_1 and IOC0_2 can be routed to Port S on the ZVMC256, ZVML31, ZVM32 and ZVM16 devices but not on other devices.

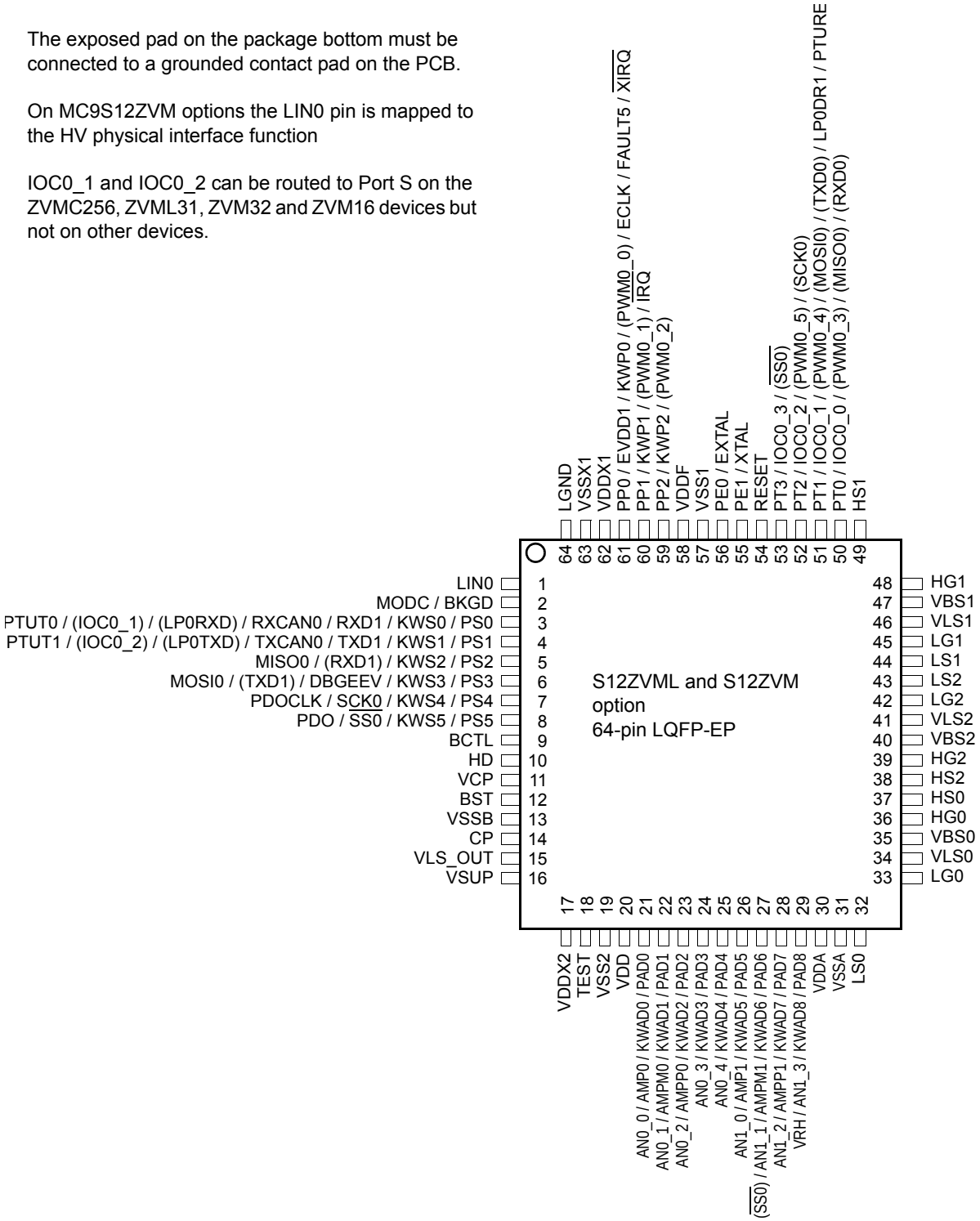


Figure 1-4. S12ZVM and S12ZVML option 64-pin LQFP pin out

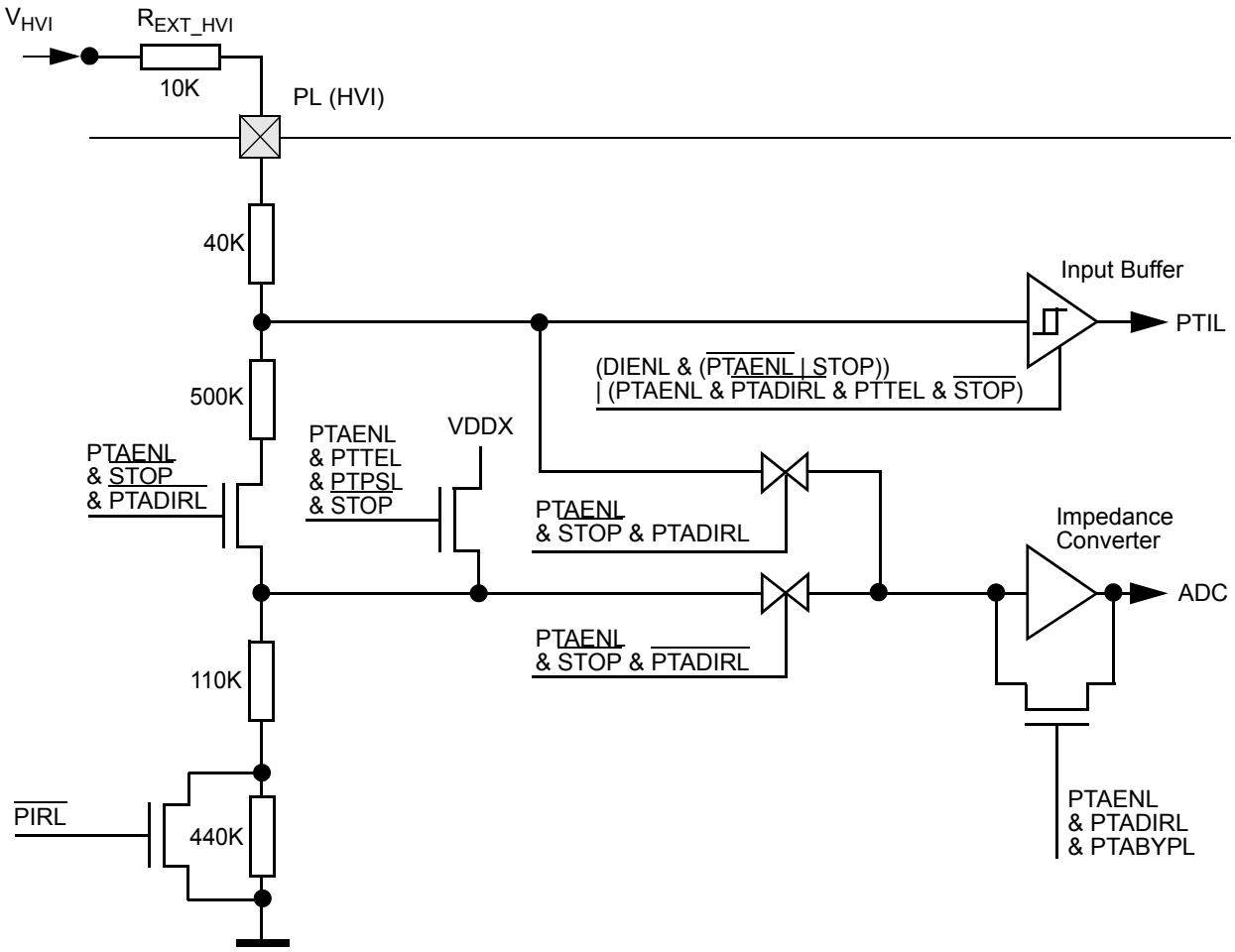


Figure 2-37. HVI Block Diagram

Voltages up to V_{HVI} can be applied to the HVI pin. Internal voltage dividers scale the input signals down to logic level. There are two modes, digital and analog, where these signals can be processed.

2.4.6.1 Digital Mode Operation

In digital mode (PTAENL=0) the input buffer is enabled if DIENL=1. The synchronized pin input state determined at threshold level V_{TH_HVI} can be read in register PTIL. Interrupt flag (PIFL) is set on input transitions if enabled (PIEL=1) and configured for the related edge polarity (PPSL). Wakeup from stop mode is supported.

2.4.6.2 Analog Mode Operation

In analog mode (PTAENL=1) the input buffer is forced off and the voltage applied to a selectable HVI pin can be measured on its related internal ADC channel(refer to device overview section for channel assignment). One of two input divider ratios ($Ratio_{H\_HVI}$, $Ratio_{L\_HVI}$) can be chosen (PIRL) on the analog

9.5.2.9 ADC Error Interrupt Flag Register (ADCEIF)

If one of the following error flags is set the ADC ceases operation:

- IA_EIF
- CMD_EIF
- EOL_EIF
- TRIG_EIF

In order to make the ADC operational again an ADC Soft-Reset must be issued which clears above listed error interrupt flags.

The error interrupt flags RSTAR_EIF and LDOK_EIF do not cause the ADC to cease operation. If set the ADC continues operation. Each of the two bits can be cleared by writing a value of 1’b1. Both bits are also cleared if an ADC Soft-Reset is issued.

All bits are cleared if bit ADC_EN is clear. Writing any flag with value 1’b0 does not clear a flag. Writing any flag with value 1’b1 does not set the flag.

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-12. ADC Error Interrupt Flag Register (ADCEIF)

Read: Anytime

Write:

- Bits RSTAR_EIF and LDOK_EIF are writable anytime
- Bits IA_EIF, CMD_EIF, EOL_EIF and TRIG_EIF are not writable

Table 9-14. ADCEIF Field Descriptions

Field	Description
7 IA_EIF	**Illegal Access Error Interrupt Flag** — This flag indicates that storing the conversion result caused an illegal access error or conversion command loading from outside system RAM or NVM area occurred. The ADC ceases operation if this error flag is set (issue of type severe). 0 No illegal access error occurred. 1 An illegal access error occurred.
6 CMD_EIF	**Command Value Error Interrupt Flag** — This flag indicates that an invalid command is loaded (Any command that contains reserved bit settings) or illegal format setting selected (reserved SRES[2:0] bit settings). The ADC ceases operation if this error flag is set (issue of type severe). 0 Valid conversion command loaded. 1 Invalid conversion command loaded.
5 EOL_EIF	**“End Of List” Error Interrupt Flag** — This flag indicates a missing “End Of List” command type in current executed CSL. The ADC ceases operation if this error flag is set (issue of type severe). 0 No “End Of List” error. 1 “End Of List” command type missing in current executed CSL.

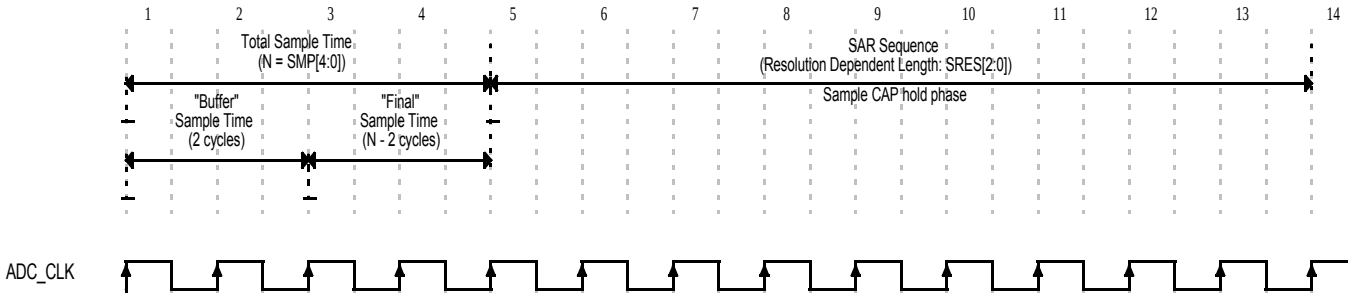


Figure 9-28. Sampling and Conversion Timing Example (8-bit Resolution, 4 Cycle Sampling)

Please note that there is always a pump phase of two ADC_CLK cycles before the sample phase begins, hence glitches during the pump phase could impact the conversion accuracy for short sample times.

9.6.3 Digital Sub-Block

The digital sub-block contains a list-based programmer's model and the control logic for the analog sub-block circuits.

9.6.3.1 Analog-to-Digital (A/D) Machine

The A/D machine performs the analog-to-digital conversion. The resolution is program selectable to be either 8- or 10- or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages.

By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

Only analog input signals within the potential range of VRL_0/1 to VRH_0/1/3 (availability of VRL_1 and VRH_2 see Table 9-2) (A/D reference potentials) will result in a non-railed digital output code.

9.6.3.2 Introduction of the Programmer's Model

The ADC_LBA provides a programmer's model that uses a system memory list-based architecture for definition of the conversion command sequence and conversion result handling.
The Command Sequence List (CSL) and Result Value List (RVL) are implemented in double buffered manner and the buffer mode is user selectable for each list (bits CSL_BMOD, RVL_BMOD). The 32-bit wide conversion command is double buffered and the currently active command is visible in the ADC register map at ADCCMD register space.

13.3.2.13 MSCAN Reserved Register

This register is reserved for factory testing of the MSCAN module and is not available in normal system operating modes.

Module Base + 0x000C — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-16. MSCAN Reserved Register

1. Read: Always reads zero in normal system operation modes
   Write: Unimplemented in normal system operation modes

NOTE

Writing to this register when in special system operating modes can alter the MSCAN functionality.

13.3.2.14 MSCAN Miscellaneous Register (CANMISC)

This register provides additional features.

Module Base + 0x000D — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	BOHOLD
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-17. MSCAN Miscellaneous Register (CANMISC)

1. Read: Anytime
   Write: Anytime; write of ‘1’ clears flag; write of ‘0’ ignored

Table 14-12. TG1LIST Register Field Descriptions

Field	Description
0 TG1LIST	Trigger Generator 1 List — This bit shows the number of the current used list. 0 Trigger generator 1 is using list 0 1 Trigger generator 1 is using list 1

Table 15-12. PMFFIE Field Descriptions

Field	Description
6,4-0 FIE[5:0]	**Fault *m* Pin Interrupt Enable** — This bit enables CPU interrupt requests to be generated by the FAULT*m* input. The fault protection circuit is independent of the FIEm bit and is active when FEN*m* is set. If a fault is detected, the PWM outputs are disabled or switched to output control according to the PMF Disable Mapping registers. 0 FAULT*m* CPU interrupt requests disabled 1 FAULT*m* CPU interrupt requests enabled *m* is 0, 1, 2, 3, 4 and 5.

15.3.2.8 PMF Fault Interrupt Flag Register (PMFFIF)

Address: Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	FIF5	0	FIF4	FIF3	FIF2	FIF1	FIF0
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-10. PMF Fault Interrupt Flag Register (PMFFIF)

1. Read: Anytime
   Write: Anytime. Write 1 to clear.

Table 15-13. PMFFIF Field Descriptions

Field	Description
6,4-0 FIF[5:0]	**Fault *m* Interrupt Flag** — This flag is set after the required number of samples have been detected after an edge to the active level(1) on the FAULT*m* input. Writing a logic one to FIF*m* clears it. Writing a logic zero has no effect. If a set flag is attempted to be cleared and a flag setting event occurs in the same cycle, then the flag remains set. The fault protection is enabled when FEN*m* is set even when the PWMs are not enabled; therefore, a fault will be latched in, requiring to be cleared in order to prevent an interrupt. 0 No fault on the FAULT*m* input 1 Fault on the FAULT*m* input **Note:** Clearing FIF*m* satisfies pending FIF*m* CPU interrupt requests. *m* is 0, 1, 2, 3, 4 and 5.

1. The active input level may be defined or programmable at SoC level. The default for internally connected resources is active-high. For availability and configurability of fault inputs on pins refer to the device overview section.

15.3.2.9 PMF Fault Qualifying Samples Register 0-1 (PMFQSMP0-1)

Address: Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	QSMP5		QSMP4	
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-11. PMF Fault Qualifying Samples Register (PMFQSMP0)

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 16-18 summarizes the results of the data bit samples.

Table 16-18. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 16-19 summarizes the results of the stop bit samples.

Table 16-19. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

Table 17-2. SPICR1 Field Descriptions (continued)

Field	Description
3 CPOL	**SPI Clock Polarity Bit** — This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Active-high clocks selected. In idle state SCK is low. 1 Active-low clocks selected. In idle state SCK is high.
2 CPHA	**SPI Clock Phase Bit** — This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...) of the SCK clock. 1 Sampling of data occurs at even edges (2,4,6,...) of the SCK clock.
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 17-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in the highest bit position. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 17-3. $\overline{SS}$ Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
0	1	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
1	0	$\overline{SS}$ input with MODF feature	$\overline{SS}$ input
1	1	$\overline{SS}$ is slave select output	$\overline{SS}$ input

17.3.2.2 SPI Control Register 2 (SPICR2)

Module Base +0x0001

	7	6	5	4	3	2	1	0
R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

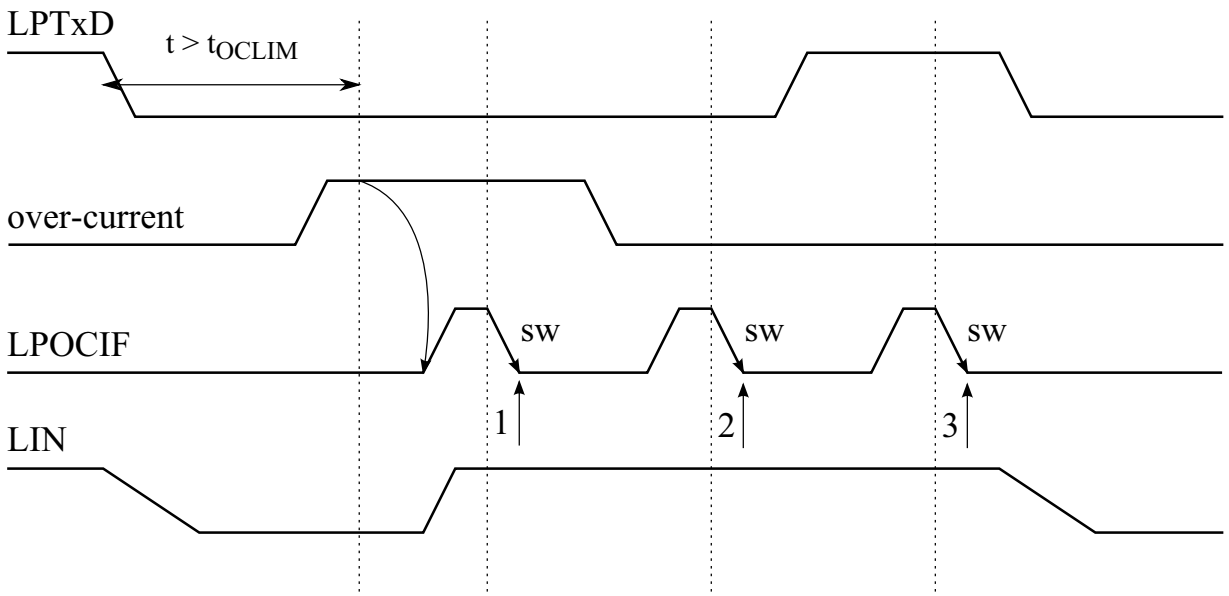
Figure 17-4. SPI Control Register 2 (SPICR2)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

NOTE

Since all MOSFET transistors are turned off, VBSX can reach phase voltage plus bootstrap voltage which may exceed allowable levels during high supply voltage conditions. If such operating condition exist the application must make sure that VBSX levels are clamped below maximum ratings for example by using clamping diodes.



1: Flag cleared, transmitter re-enable not successful because over-current is still present
2: Flag cleared, transmitter re-enable not successful because LPTxD is dominant
3: Flag cleared, transmitter re-enable successful

Figure 19-12. Overcurrent interrupt handling

19.4.4.2 TxD-dominant timeout Interrupt

NOTE

In order to perform PWM communication, the TxD-dominant timeout feature must be disabled.

To protect the LIN bus from a network lock-up, the LIN Physical Layer implements a TxD-dominant timeout mechanism. When the LPTxD signal has been dominant for more than t_{DTLIM} the transmitter is disabled and the LPDT status flag and the LPDTIF interrupt flag are set.

In order to re-enable the transmitter again, the following prerequisites must be met:

1) TxD-dominant condition is over (LPDT=0)

2) LPTxD is recessive or the LIN Physical Layer is in shutdown or receive only mode for a minimum of a transmit bit time

21.4 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the CAN Physical Layer.

21.4.1 Module Memory Map

A summary of the registers associated with the CAN Physical Layer sub-block is shown in Table 21-3. Detailed descriptions of the registers and bits are given in the following sections.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	CPDR	R	CPDR7	0	0	0	0	0	CPDR1	CPDR0
		W								
0x0001	CPCR	R	CPE	SPE	WUPE1-0		0	SLR2-0		
		W								
0x0002	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0003	CPSR	R	CPCHVH	CPCHVL	CPCLVH	CPCLVL	CPDT	0	0	0
		W								
0x0004	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0005	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0006	CPIE	R	0	0	0	CPVFIE	CPDTIE	0	0	CPOCIE
		W								
0x0007	CPIF	R	CHVHIF	CHVLIF	CLVHIF	CLVLIF	CPDTIF	0	CHOCIF	CLOCIF
		W								

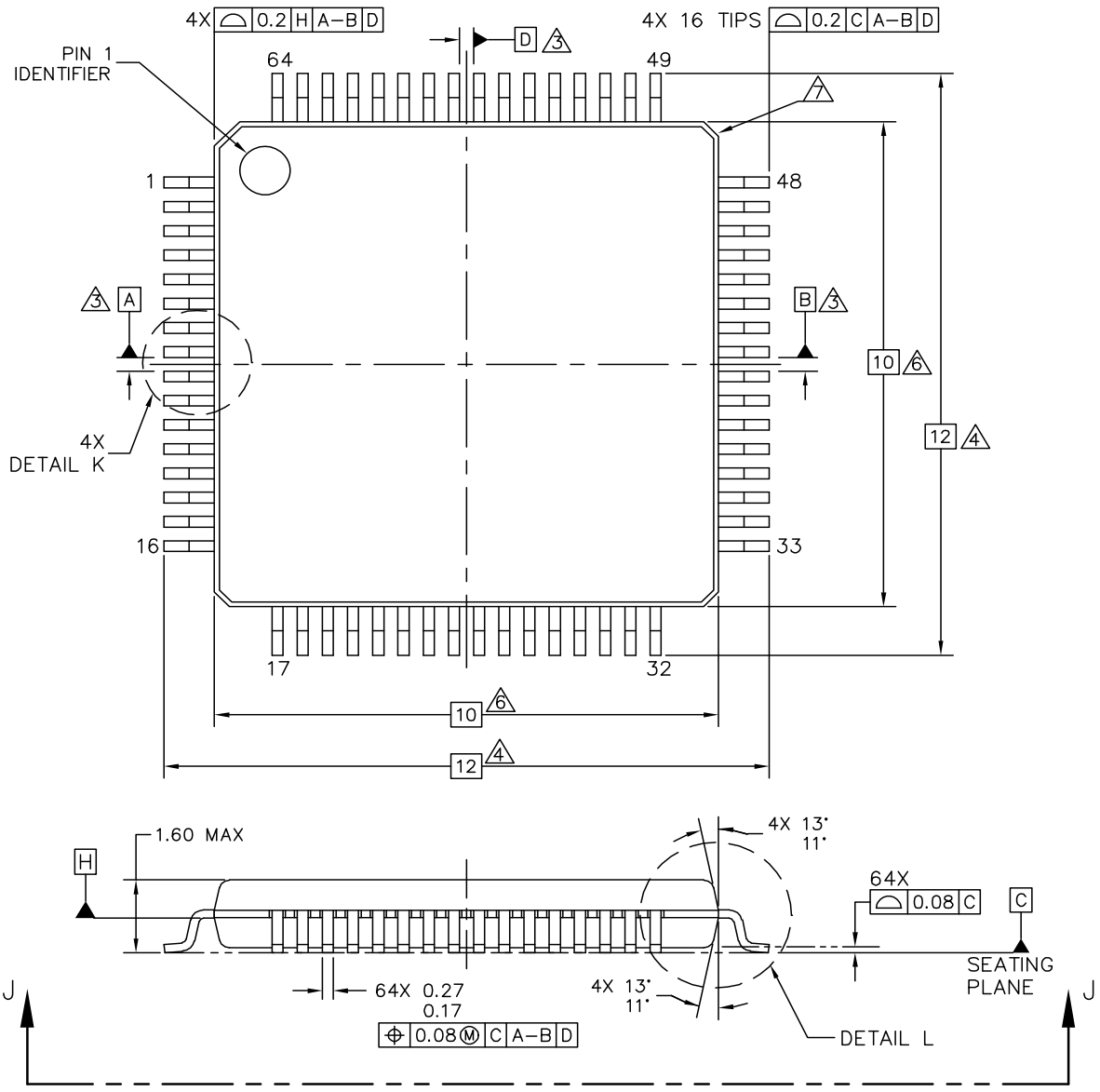
= Unimplemented or Reserved

Table 21-3. CAN Physical Layer Register Summary

K.2 64LQFP-EP Mechanical Info (all mask sets except 1N95G, 2N95G)

Figure K-2. 64LQFP-EP Mechanical Information (all mask sets except 1N95G, 2N95G)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA10763D
		PAGE: 1899
	DO NOT SCALE THIS DRAWING	REV: B



TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER:	1899-03
		STANDARD:	JEDEC MS-026 BCD
		SHEET:	1 OF 5