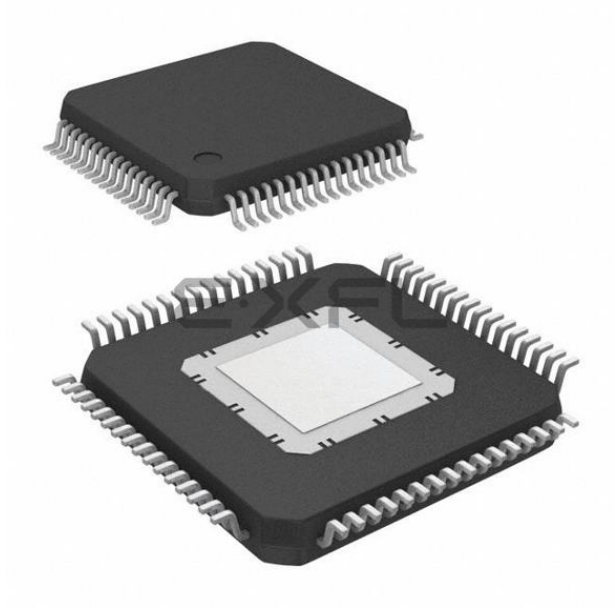

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Product Status	Active
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Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml32f3wkhr

Table 1-9. Pin Summary For 80-Pin Package Option (ZVMC256 Only) (Sheet 2 of 5)

Pin #	Pin Name	Function (Priority and routing options defined in PIM chapter)							Supply	Internal Pull Resistor	
		1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.	6th Func.	7th Func.		CTRL	Reset State
11	BCTLS 1	—	—	—	—	—	—		—	—	—
12	VDDS1	VRH0_1	VRH1_1	—	—	—	—		—	—	—
13	SNPS2	—	—	—	—	—	—		—	—	—
14	BCTLS 2	—	—	—	—	—	—		—	—	—
15	VDDS2	VRH0_2	VRH1_2	—	—	—	—		—	—	—
16	LD0	—	—	—	—	—	—		—	—	—
17	LD1	—	—	—	—	—	—		—	—	—
18	LD2	—	—	—	—	—	—		—	—	—
19	PAD0	KWAD0	AN0_0	AMP0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
20	PAD1	KWAD1	AN0_1	AMPM0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
21	PAD2	KWAD2	AN0_2	AMPP0	—	—	—		V_{DDA}	PERADL/PPSADL	Off
22	PAD3	KWAD3	AN0_3	—	—	—	—		V_{DDA}	PERADL/PPSADL	Off
23	PAD4	KWAD4	AN0_4	—	—	—	—		V_{DDA}	PERADL/PPSADL	Off
24	PAD5	KWAD5	AN1_0	AMP1	—	—	—		V_{DDA}	PERADL/PPSADL	Off
25	PAD6	KWAD6	AN1_1	$\overline{SS0}$	AMPM1	—	—		V_{DDA}	PERADL/PPSADL	Off
26	PAD7	KWAD7	AN1_2	AMPP1	—	—	—		V_{DDA}	PERADL/PPSADL	Off
27	PAD8	KWAD8	AN1_3	—	—	—	—		V_{DDA}	PERADH/PPSADH	Off

StoredReference: Value in IFR location
n: ADC resolution (12 bit)

NOTE

The ADC reference voltage V_{RH} must remain at a constant level throughout the conversion process.

1.13.2 SCI Baud Rate Detection

The baud rate for SCI0 and SCI1 is achieved by using a timer channel to measure the data rate on the RXD signal.

1. Establish the link:
   — For SCI0: Set [T0IC3RR1:T0IC3RR0]=0b01 to disconnect IOC0_3 from TIM0 input capture channel 3 and reroute the timer input to the RXD0 signal of SCI0.
   — For SCI1: Set [T0IC3RR1:T0IC3RR0]=0b10 to disconnect IOC0_3 from TIM0 input capture channel 3 and reroute the timer input to the RXD1 signal of SCI1.
2. Determine pulse width of incoming data: Configure TIM0 IC3 to measure time between incoming signal edges.

1.13.3 Motor Control Application Overview

The following sections provide information for using the device in motor control applications. These sections provide a description of motor control loop considerations that are not detailed in the individual module sections, since they concern device level inter module operation specific for motor control. More detailed information is available in application notes**.** The applications described are as follows:

1. BDCM - wiper pumps fans
2. BLDCM - pumps, fans and blowers
   – based on Hall sensors
   – sensorless based on back-EMF zero crossing comparators
   – sensorless based on back-EMF ADC measurements
3. PMSM - high-end wiper, pumps, fans and blowers
   – simple sinewave commutation with position sensor Hall effect, sine-cos
   – FOC with sine-cos position sensor
   – sensorless 3-phase sinewave control

Table 4-3. INT Memory Map

0x000019	Interrupt Request Configuration Data Register 1 (INT_CFDATA1)	R/W
0x00001A	Interrupt Request Configuration Data Register 2 (INT_CFDATA2	R/W
0x00001B	Interrupt Request Configuration Data Register 3 (INT_CFDATA3)	R/W
0x00001C	Interrupt Request Configuration Data Register 4 (INT_CFDATA4)	R/W
0x00001D	Interrupt Request Configuration Data Register 5 (INT_CFDATA5)	R/W
0x00001E	Interrupt Request Configuration Data Register 6 (INT_CFDATA6)	R/W
0x00001F	Interrupt Request Configuration Data Register 7 (INT_CFDATA7)	R/W

4.3.2 Register Descriptions

This section describes in address order all the INT module registers and their individual bits.

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000010	IVBR	R	IVB_ADDR[15:8]							
		W								
0x000011		R	IVB_ADDR[7:1]							0
		W								
0x000017	INT_CFADDR	R	0	INT_CFADDR[6:3]				0	0	0
		W								
0x000018	INT_CFDATA0	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x000019	INT_CFDATA1	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001A	INT_CFDATA2	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001B	INT_CFDATA3	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								
0x00001C	INT_CFDATA4	R	0	0	0	0	0	PRIOLVL[2:0]		
		W								

= Unimplemented or Reserved

Figure 4-2. INT Register Summary

5.3.2 Register Descriptions

The BDC registers are shown in Figure 5-2. Registers are accessed only by host-driven communications to the BDC hardware using READ_BDCCSR and WRITE_BDCCSR commands. They are not accessible in the device memory map.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
Not Applicable	BDCCSRH	R	ENBDC	BDMACT	BDCCIS	0	STEAL	CLKSW	UNSEC	ERASE
		W								
Not Applicable	BDCCSRL	R	WAIT	STOP	RAMWF	OVRUN	NORESP	RDINV	ILLACC	ILLCMD
		W								

= Unimplemented, Reserved 0 = Always read zero

Figure 5-2. BDC Register Summary

5.3.2.1 BDC Control Status Register High (BDCCSRH)

Register Address: This register is not in the device memory map. It is accessible using BDC inherent addressing commands

	7	6	5	4	3	2	1	0
R	ENBDC	BDMACT	BDCCIS	0	STEAL	CLKSW	UNSEC	ERASE
W								
Reset								
Secure AND SSC-Mode	1	1	0	0	0	0	0	0
Unsecure AND SSC-Mode	1	1	0	0	0	0	1	0
Secure AND NSC-Mode	0	0	0	0	0	0	0	0
Unsecure AND NSC-Mode	0	0	0	0	0	0	1	0

= Unimplemented, Reserved

0 = Always read zero

Figure 5-3. BDC Control Status Register High (BDCCSRH)

Read: All modes through BDC operation only.

Write: All modes through BDC operation only, when not secured, but subject to the following:

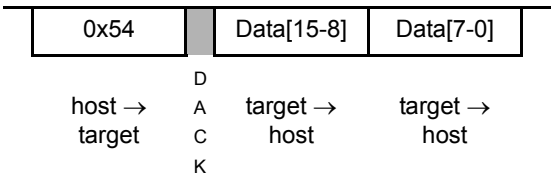
- Bits 7,3 and 2 can only be written by WRITE_BDCCSR commands.
- Bit 5 can only be written by WRITE_BDCCSR commands when the device is not in stop mode.
- Bits 6, 1 and 0 cannot be written. They can only be updated by internal hardware.

bits[31:0]; the second to trace buffer line bits[63:32]. If ACK handshaking is disabled, the host must wait 16 clock cycles (DLY) after completing the first 32-bit read before starting the second 32-bit read.

5.4.4.13 READ_SAME.sz, READ_SAME.sz_WS

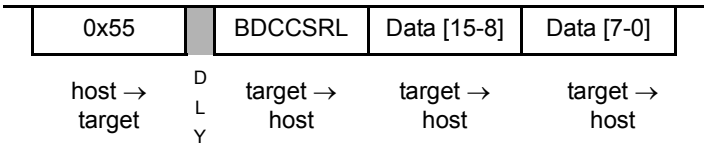
READ_SAME

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



READ_SAME_WS

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



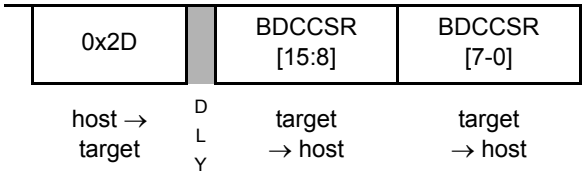
Read from location defined by the previous READ_MEM. The previous READ_MEM command defines the address, subsequent READ_SAME commands return contents of same address. The example shows the sequence for reading a 16-bit word size. Byte alignment details are described in Section 5.4.5.2”. If enabled, an ACK pulse is driven before the data bytes are transmitted.

NOTE

READ_SAME{_WS} is a valid command only when preceded by SYNC, NOP, READ_MEM{_WS}, or another READ_SAME{_WS} command. Otherwise, an illegal command response is returned, setting the ILLCMD bit. NOP can be used for inter-command padding without corrupting the address pointer.

5.4.4.14 READ_BDCCSR

Read BDCCSR Status Register **Always Available**



Read the BDCCSR status register. This command can be executed in any mode.

Table 8-17. CPMUHTCTL Field Descriptions

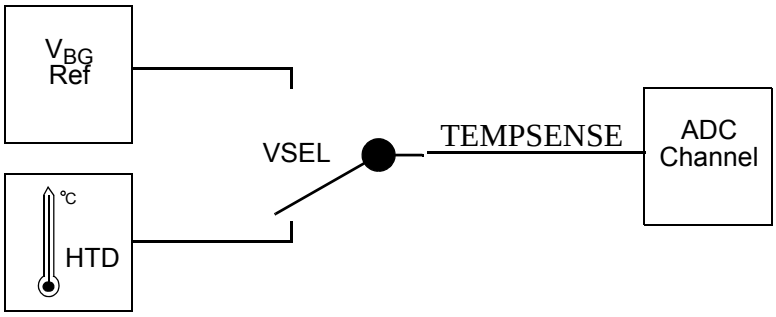
Field	Description
5 VSEL	**Voltage Access Select Bit** — If set, the bandgap reference voltage V_{BG} can be accessed internally (i.e. multiplexed to an internal Analog to Digital Converter channel). If not set, the die temperature proportional voltage V_{HT} of the temperature sensor can be accessed internally. See device level specification for connectivity. For any of these access the HTE bit must be set. 0 An internal temperature proportional voltage V_{HT} can be accessed internally. 1 Bandgap reference voltage V_{BG} can be accessed internally.
3 HTE	**High Temperature Sensor/Bandgap Voltage Enable Bit** — This bit enables the high temperature sensor and bandgap voltage amplifier. 0 The temperature sensor and bandgap voltage amplifier is disabled. 1 The temperature sensor and bandgap voltage amplifier is enabled.
2 HTDS	**High Temperature Detect Status Bit** — This read-only status bit reflects the temperature status. Writes have no effect. 0 Junction Temperature is below level T_{HTID} or RPM. 1 Junction Temperature is above level T_{HTIA} and FPM.
1 HTIE	High Temperature Interrupt Enable Bit 0 Interrupt request is disabled. 1 Interrupt will be requested whenever HTIF is set.
0 HTIF	**High Temperature Interrupt Flag** — HTIF is set to 1 when HTDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (HTIE=1), HTIF causes an interrupt request. 0 No change in HTDS bit. 1 HTDS bit has changed.

NOTE

The voltage at the temperature sensor can be computed as follows:

$V_{HT}(temp) = V_{HT(150)} - (150 - temp) * dV_{HT}$

Figure 8-22. Voltage Access Select



8.7.3 Application Information for PLL and Oscillator Startup

The following C-code example shows a recommended way of setting up the system clock system using the PLL and Oscillator:

```
/* Procedure proposed by to setup PLL and Oscillator */
/* example for OSC = 4 MHz and Bus Clock = 25MHz, That is VCOCLK = 50MHz */

/* Initialize */
/* PLL Clock = 50 MHz, divide by one */
CPMUPOSTDIV = 0x00;

/* Generally: Whenever changing PLL reference clock (REFCLK) frequency to a higher value */
/* it is recommended to write CPMUSYNR = 0x00 in order to stay within specified */
/* maximum frequency of the MCU */
CPMUSYNR = 0x00;

/* configure PLL reference clock (REFCLK) for usage with Oscillator */
/* OSC=4MHz divide by 4 (3+1) = 1MHz, REFCLK range 1MHz to 2 MHz (REFFRQ[1:0] = 00) */
CPMUREFDIV = 0x03;

/* enable external Oscillator, switch PLL reference clock (REFCLK) to OSC */
CPMUOSC = 0x80;

/* multiply REFCLK = 1MHz by 2*(24+1)*1MHz = 50MHz */
/* VCO range 48 to 80 MHz (VCOFRQ[1:0] = 01) */
CPMUSYNR = 0x58;

/* clear all flags, especially LOCKIF and OSCIF */
CPMUIFLG = 0xFF;

/* put your code to loop and wait for the LOCKIF and OSCIF or */
/* poll CPMUIFLG register until both UPOSC and LOCK status are "1" */
/* that is CPMUIFLG == 0x1B */

/*..............continue to your main code execution here..............*/

/* in case later in your code you want to disable the Oscillator and use the */
/* 1MHz IRCCLK as PLL reference clock */

/* Generally: Whenever changing PLL reference clock (REFCLK) frequency to a higher value */
/* it is recommended to write CPMUSYNR = 0x00 in order to stay within specified */
/* maximum frequency of the MCU */
CPMUSYNR = 0x00;

/* disable OSC and switch PLL reference clock to IRC */
CPMUOSC = 0x00;

/* multiply REFCLK = 1MHz by 2*(24+1)*1MHz = 50MHz */
/* VCO range 48 to 80 MHz (VCOFRQ[1:0] = 01) */
CPMUSYNR = 0x58;

/* clear all flags, especially LOCKIF and OSCIF */
CPMUIFLG = 0xFF;
```

9.5.2.18 ADC Command Register 3 (ADCCMD_3)

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved					
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-21. ADC Command Register 3 (ADCCMD_3)

9.9.10 Fully Timing Controlled Conversion

As described previously, in “Trigger Mode” a Restart Event automatically causes a trigger. To have full and precise timing control of the beginning of any conversion/sequence the “Restart Mode” is available. In “Restart Mode” a Restart Event does not cause a Trigger automatically; instead, the Trigger must be issued separately and with correct timing, which means the Trigger is not allowed before the Restart Event (conversion command loading) is finished (bit RSTA=1’b0 again). The time required from Trigger until sampling phase starts is given (refer to Section 9.5.2.6, “ADC Conversion Flow Control Register (ADCFLWCTL), Timing considerations) and hence timing is fully controllable by the application. Additionally, if a Trigger occurs before a Restart Event is finished, this causes the TRIG_EIF flag being set. This allows detection of false flow control sequences.

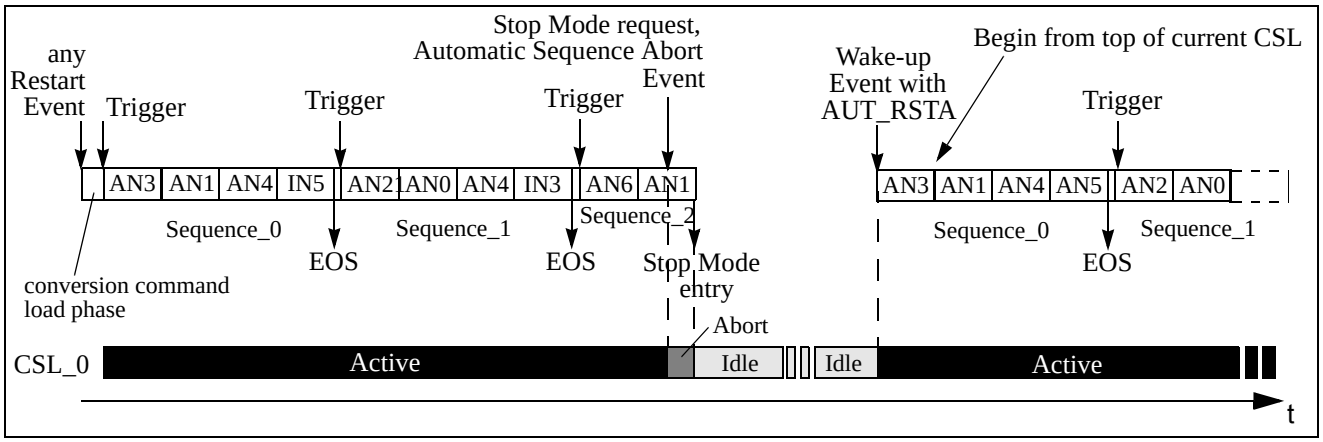


Figure 9-44. Conversion Flow Control Diagram — Fully Timing Controlled Conversion (with Stop Mode)

Unlike the Stop Mode entry shown in Figure 9-43 and Figure 9-44 it is recommended to issue the Stop Mode at sequence boundaries (when ADC is idle and no conversion/conversion sequence is ongoing).

Any of the Conversion flow control application use cases described above (Continuous, Triggered, or Fully Timing Controlled Conversion) can be used with CSL single buffer mode or with CSL double buffer mode. If using CSL double buffer mode, CSL swapping is performed by issuing a Restart Event with bit LDOK set.

Table 14-6. PTUIEL Register Field Descriptions

Field	Description
5 TG1TEIE	Trigger Generator 1 Timing Error Interrupt Enable — Enables trigger generator timing error interrupt. 0 No interrupt will be requested whenever TG1TEIF is set 1 Interrupt will be requested whenever TG1TEIF is set
4 TG1DIE	Trigger Generator 1 Done Interrupt Enable — Enables trigger generator done interrupt. 0 No interrupt will be requested whenever TG1DIF is set 1 Interrupt will be requested whenever TG1DIF is set
3 TG0AEIE	Trigger Generator 0 Memory Access Error Interrupt Enable — Enables trigger generator memory access error interrupt. 0 No interrupt will be requested whenever TG0AEIF is set 1 Interrupt will be requested whenever TG0AEIF is set
2 TG0REIE	Trigger Generator 0 Reload Error Interrupt Enable — Enables trigger generator reload error interrupt. 0 No interrupt will be requested whenever TG0REIF is set 1 Interrupt will be requested whenever TG0REIF is set
1 TG0TEIE	Trigger Generator 0 Timing Error Interrupt Enable — Enables trigger generator timing error interrupt. 0 No interrupt will be requested whenever TG0TEIF is set 1 Interrupt will be requested whenever TG0TEIF is set
0 TG0DIE	Trigger Generator 0 Done Interrupt Enable — Enables trigger generator done interrupt. 0 No interrupt will be requested whenever TG0DIF is set 1 Interrupt will be requested whenever TG0DIF is set

Figure 15-23. PMF Compare Invert Register (PMFCINV) Descriptions (continued)

Field	Description
1 CINV1	**PWM Compare Invert 1** — This bit controls the polarity of PWM compare output 1. Please see the output operations in Figure 15-42 and Figure 15-43. 0 PWM output 1 is high when PMFCNTA is less than PMFVAL1 1 PWM output 1 is high when PMFCNTA is greater than PMFVAL1.
0 CINV0	**PWM Compare Invert 0** — This bit controls the polarity of PWM compare output 0. Please see the output operations in Figure 15-42 and Figure 15-43. 0 PWM output 0 is high when PMFCNTA is less than PMFVAL0. 1 PWM output 0 is high when PMFCNTA is greater than PMFVAL0

NOTE

Changing CINV*n* can affect the present PWM cycle, if the related PMFVAL*n* is zero.

15.3.2.19 PMF Enable Control A Register (PMFENCA)

Address: Module Base + 0x0020 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	PWMENA	GLDOKA	0	0	0	RSTRTA	LDOKA	PWMRIEA
W								
Reset	0	0	0	0	0	0	0	0

Figure 15-24. PMF Enable Control A Register (PMFENCA)

1. Read: Anytime
   Write: Anytime except GLDOKA and RSTRTA which cannot be modified after the WP bit is set.

Table 15-25. PMFENCA Field Descriptions

Field	Description
7 PWMENA	**PWM Generator A Enable** — When MTG is clear, this bit when set enables the PWM generators A, B and C and PWM0–5 outputs. When PWMENA is clear, PWM generators A, B and C are disabled, and the PWM0–5 outputs are in their inactive states unless the corresponding OUTCTL bits are set. When MTG is set, this bit when set enables the PWM generator A and the PWM0 and PWM1 outputs.When PWMENA is clear, the PWM generator A is disabled and PWM0 and PWM1 outputs are in their inactive states unless the OUTCTL0 and OUTCTL1 bits are set. After setting this bit a reload event is generated at the beginning of the PWM cycle. 0 PWM generator A and PWM0-1 (2–5 if MTG = 0) outputs disabled unless the respective OUTCTL bit is set 1 PWM generator A and PWM0-1 (2–5 if MTG = 0) outputs enabled
6 GLDOKA	**Global Load Okay A** — When this bit is set, a PMF external global load OK defined on device level replaces the function of LDOKA. This bit cannot be modified after the WP bit is set. 0 LDOKA controls reload of double buffered registers 1 PMF external global load OK controls reload of double buffered registers
2 RSTRTA	**Restart Generator A** — When this bit is set, PWM generator A will be restarted at the next commutation event. This bit cannot be modified after the WP bit is set. 0 No PWM generator A restart at the next commutation event. 1 PWM generator A restarts at the next commutation event

16.5.3.1.6 RXEDGIF Description

The RXEDGIF interrupt is set when an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD pin is detected. Clear RXEDGIF by writing a “1” to the SCIASR1 SCI alternative status register 1.

16.5.3.1.7 BERRIF Description

The BERRIF interrupt is set when a mismatch between the transmitted and the received data in a single wire application like LIN was detected. Clear BERRIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if the bit error detect feature is disabled.

16.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

16.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

16.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

Table 18-6. GDUDSE Register Field Descriptions

Field	Description
6-4 GDHSIF[2:0]	GDU High-Side Driver Desaturation Interrupt Flags — The flag is set by hardware to “1” when a desaturation error on associated high-side driver pin HS[2:0] occurs. If the GDSEIE bit is set an interrupt is requested. Writing a logic “1” to the bit field clears the flag. 0 No desaturation error on high-side driver 1 Desaturation error on high-side driver
2-0 GDLSIF[2:0]	GDU Low-Side Driver Desaturation Interrupt Flag — The flag is set to “1” when a desaturation error on associated low-side driver pin LS[2:0] occurs. If the GDSEIE bit is set an interrupt is requested. Writing a logic “1” to the bit field clears the flag. 0 No desaturation error on low-side driver 1 Desaturation error on low-side driver

21.2.1 CANH — CAN Bus High Pin

The CANH signal either connects directly to CAN bus high line or through an optional external common mode choke.

21.2.2 CANL — CAN Bus Low Pin

The CANL signal either connects directly to CAN bus low line or through an optional external common mode choke.

21.2.3 SPLIT — CAN Bus Termination Pin

The SPLIT pin can drive a 2.5 V bias for bus termination purpose (CAN bus middle point). Usage of this pin is optional and depends on bus termination strategy for a given bus network.

21.2.4 VDDC — Supply Pin for CAN Physical Layer

The VDDC pin is used to supply the CAN Physical Layer with 5 V from an external source.

21.2.5 VSSC — Ground Pin for CAN Physical Layer

The VSSC pin is the return path for the 5 V supply (VDDC).

21.3 Internal Signal Description

21.3.1 CPTXD — TXD Input to CAN Physical Layer

CPTXD is the input signal to the CAN Physical Layer. A logic 1 on this input is considered CAN recessive and a logic 0 as dominant level.

Per default, CPTXD is connected device-internally to the TXCAN transmitter output of the MSCAN module. For optional routing options consult the device level documentation.

21.3.2 CPRXD — RXD Output of CAN Physical Layer

CPRXD is the output signal of the CAN Physical Layer. A logic 1 on this output represents CAN recessive and a logic 0 a dominant level.

In stand-by mode the wake-up receiver is routed to this output. A dominant pulse filter can optionally be enabled to increase robustness against false wake-up pulses. In any other mode this signal defaults to the precision receiver without a pulse filter.

Per default, CPRXD is connected device-internally to the RXCAN receiver input of the MSCAN module. For optional routing options consult the device level documentation.

Table 22-9. PWMCAE Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7–0 CAE[7:0]	Center Aligned Output Modes on Channels 7–0 0 Channels 7–0 operate in left aligned output mode. 1 Channels 7–0 operate in center aligned output mode.

22.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 22-8. PWM Control Register (PWMCTL)

Read: Anytime

Write: Anytime

There are up to four control bits for concatenation, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. If the corresponding channels do not exist on a particular derivative, then writes to these bits have no effect and reads will return zeroes. When channels 6 and 7are concatenated, channel 6 registers become the high order bytes of the double byte channel. When channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

See Section 22.4.2.7, “PWM 16-Bit Functions” for a more detailed description of the concatenation PWM Function.

NOTE

Change these bits only when both corresponding channels are disabled.

Appendix D
LIN/HV PHY Electrical Specifications

D.1 Static Electrical Characteristics

Table D-1. Static electrical characteristics of the LIN/HV PHY (Junction Temperature From -40°C To +175°C)

Characteristics noted under conditions 5.5V <= V_{LINSUP} <= 18V unless otherwise noted(1) (2) (3). Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.							
Num	**C**	Ratings	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		V_{LINSUP} range for LIN compliant electrical characteristics	V_{LINSUP_LIN}	5.5[1 2]	12	18	V
2		Current limitation into the LIN pin in dominant state(4) V_{LIN} = $V_{LINSUP\_LIN\_MAX}$	I_{LIN_LIM}	40	—	200	mA
3		Input leakage current in dominant state, driver off, internal pull-up on (V_{LIN} = 0V, V_{LINSUP} = 12V)	$I_{LIN\_PAS\_dom}$	-1	—	—	mA
4		Input leakage current in recessive state, driver off (5V<V_{LINSUP}<18V, 5V<V_{LIN}<18V, V_{LIN} => V_{LINSUP})	$I_{LIN\_PAS\_rec}$	—	—	20	µA
5		Input leakage current when ground disconnected (GND_{Device} = V_{LINSUP}, 0V<V_{LIN}<18V, V_{LINSUP} = 12V)	$I_{LIN\_NO\_GND}$	-1	—	1	mA
6		Input leakage current when battery disconnected (V_{LINSUP} = GND, 0<V_{LIN}<18V)	$I_{LIN\_NO\_BAT}$	—	—	30	µA
7		Receiver dominant state	V_{LINdom}	—	—	0.4	V_{LINSUP}
8		Receiver recessive state	V_{LINrec}	0.6	—	—	V_{LINSUP}
9		V_{LIN_CNT} =(V_{th_dom}+ V_{th_rec})/2	V_{LIN_CNT}	0.475	0.5	0.525	V_{LINSUP}
10		V_{HYS} = V_{th_rec} -V_{th_dom}	V_{HYS}	—	—	0.175	V_{LINSUP}
11		Maximum capacitance allowed on slave node	C_{slave}	—	220	250	pF
12a		Capacitance of LIN pin -40°C < T_J < 150°C, Recessive state	C_{int}	—	20	—	pF
12b		Capacitance of LIN pin -40°C < T_J < 150°C, Recessive state	C_{int}	—	—	45	pF
12c		Capacitance of LIN pin 150°C < T_J < 175°C, Recessive state	C_{int}	—	—	39	pF
13		Internal pull-up (slave)	R_{slave}	27	34	40	kΩ

1. For 3.5V<= V_{LINSUP} <5V, the LIN/HV PHY is still working but with degraded parametrics.

2. For 5V<= V_{LINSUP} <5.5V, characterization showed that all parameters generally stay within the indicated specification, except the duty cycles D2 and D4 which may increase and potentially go beyond their maximum limits for highly loaded buses.

3. The V_{LINSUP} voltage is provided by the VLINSUP supply. This supply mapping is described in device level documentation.

Table F-4. FTMRZ32K128 NVM Timing Characteristics (Junction Temperature From 150°C To +175°C)

Derivatives ZVML31, ZVM32, ZVM16									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	40	40	40	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	8992	t_{RD1ALL}	0.22	0.22	0.45	17.98	ms
4	Erase Verify Block (Pflash)	0	8750	t_{RD1BLK_P}	0.22	0.22	0.44	17.50	ms
5	Erase Verify Block (EEPROM)	0	631	t_{RD1BLK_D}	0.02	0.02	0.03	1.26	ms
6	Erase Verify P-Flash Section	0	511	t_{RD1SEC}	0.01	0.01	0.03	1.02	ms
7	Read Once	0	481	t_{RDONCE}	12.03	12.03	12.03	481.00	us
8	Program P-Flash (4 Word)	164	3136	t_{PGM_4}	0.23	0.24	0.48	12.75	ms
9	Program Once	164	3107	$t_{PGMONCE}$	0.23	0.24	0.24	3.31	ms
10	Erase All Blocks	100066	9455	t_{ERSALL}	95.54	100.30	100.54	143.99	ms
11	Erase Flash Block (Pflash)	100060	9119	t_{ERSBLK_P}	95.52	100.29	100.52	143.31	ms
12	Erase Flash Block (EEPROM)	100060	970	t_{ERSBLK_D}	95.32	100.08	100.11	127.02	ms
13	Erase P-Flash Sector	20015	927	t_{ERSPG}	19.09	20.04	20.06	26.87	ms
14	Unsecure Flash	100066	9533	t_{UNSECU}	95.54	100.30	100.54	144.15	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	12.33	12.33	12.33	493.00	us
16	Set User Margin Level	0	439	t_{MLOADU}	10.98	10.98	10.98	439.00	us
17	Set Factory Margin Level	0	448	t_{MLOADF}	11.20	11.20	11.20	448.00	us
18	Erase Verify EEPROM Sector	0	583	$t_{DRD1SEC}$	0.01	0.01	0.03	1.17	ms
19	Program EEPROM (1 Word)	68	1678	t_{DPGM_1}	0.11	0.11	0.24	6.80	ms
20	Program EEPROM (2 Word)	136	2702	t_{DPGM_2}	0.20	0.20	0.41	10.98	ms
21	Program EEPROM (3 Word)	204	3726	t_{DPGM_3}	0.29	0.30	0.58	15.16	ms
22	Program EEPROM (4 Word)	272	4750	t_{DPGM_4}	0.38	0.39	0.75	19.34	ms
23	Erase EEPROM Sector	5015	817	t_{DERSPG}	4.80	5.04	20.41	38.96	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	11.88	11.88	11.88	475.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

freescale semiconductor	**MECHANICAL OUTLINES DICTIONARY**	DOCUMENT NO: 98ASA00237D
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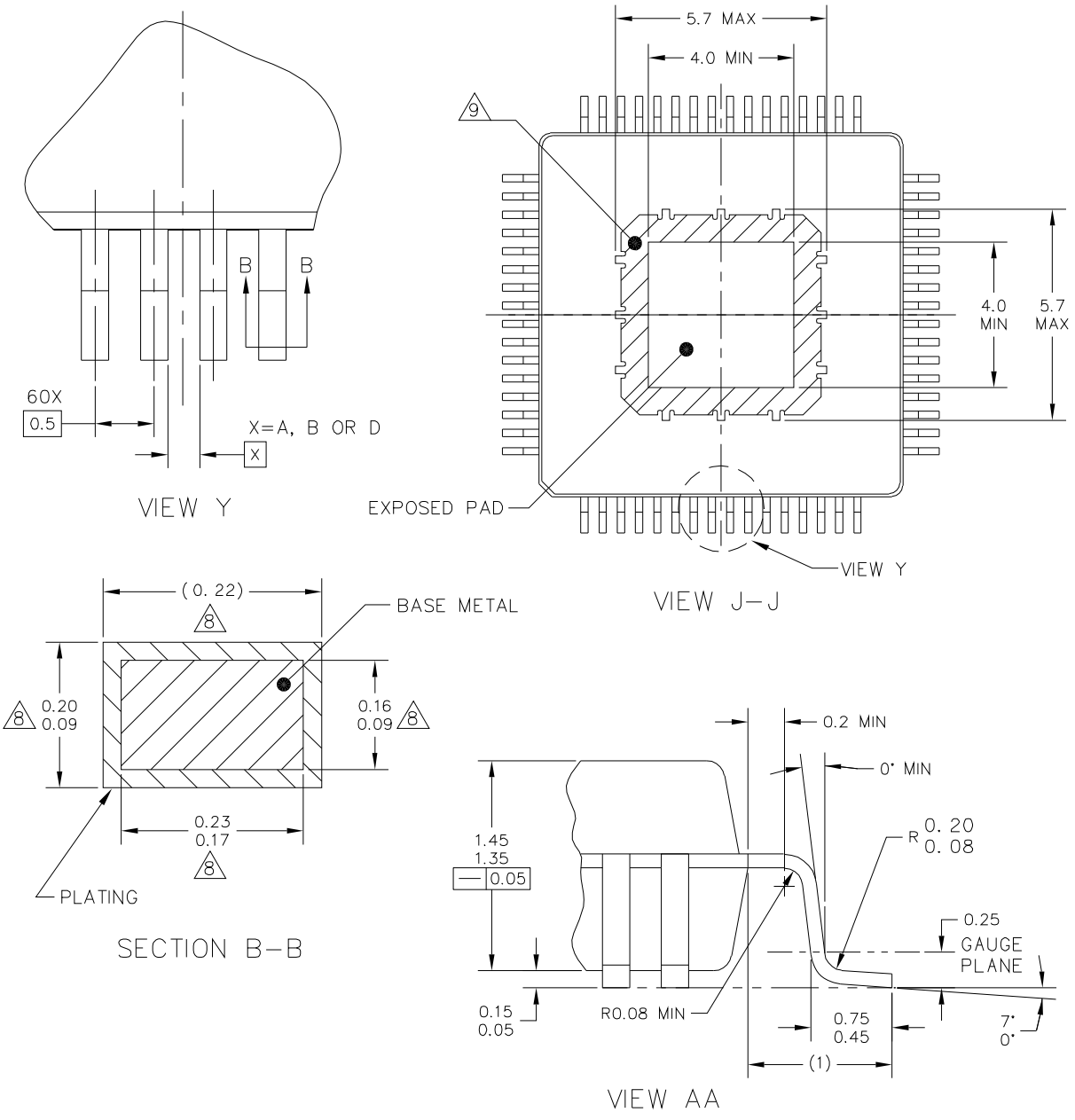

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 4.9 X 4.9 EXPOSED PAD	CASE NUMBER: 2139–01	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: IN AGILE	SHEET: 2 OF 4

M.14 0x0640-0x067F ADC1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0656	ADC1CMD_2	R	SMP[4:0]					0	0	Reserved
		W								
0x0657	ADC1CMD_3	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0658	Reserved	R	Reserved							
		W								
0x0659	Reserved	R	Reserved							
		W								
0x065A	Reserved	R	Reserved							
		W								
0x065B	Reserved	R	Reserved							
		W								
0x065C	ADC1CIDX	R	0	0	CMD_IDX[5:0]					
		W								
0x065D	ADC1CBP_0	R	CMD_PTR[23:16]							
		W								
0x065E	ADC1CBP_1	R	CMD_PTR[15:8]							
		W								
0x065F	ADC1CBP_2	R	CMD_PTR[7:2]						0	0
		W								
0x0660	ADC1RIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0661	ADC1RBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0662	ADC1RBP_1	R	RES_PTR[15:8]							
		W								
0x0663	ADC1RBP_2	R	RES_PTR[7:2]						0	0
		W								
0x0664	ADC1CROFF0	R	0	CMDRES_OFF0[6:0]						
		W								
0x0665	ADC1CROFF1	R	0	CMDRES_OFF1[6:0]						
		W								
0x0666	Reserved	R	0	0	0	0	Reserved			
		W								
0x0667	Reserved	R	Reserved							
		W								
0x0668	Reserved	R	Reserved						0	0
		W								
0x0669	Reserved	R	Reserved	0	Reserved					
		W								
0x066A-0x067F	Reserved	R	0	0	0	0	0	0	0	0
		W								