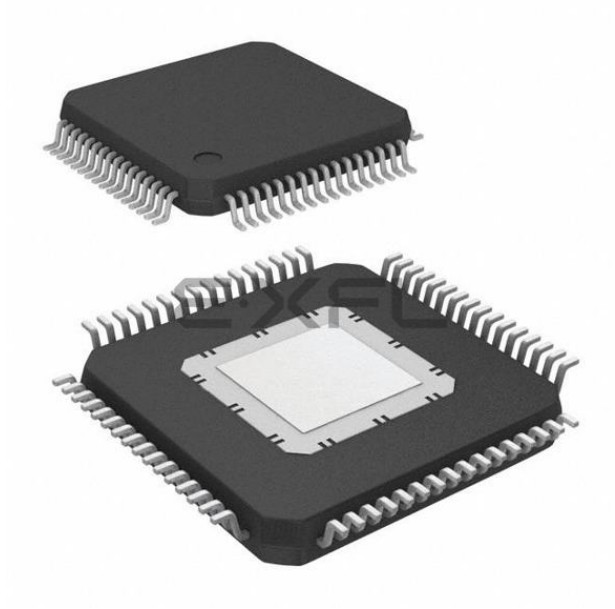

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml64f1mkh

The exposed pad on the package bottom must be connected to a grounded contact pad on the PCB.

The LIN0 pin is mapped to the HV physical interface

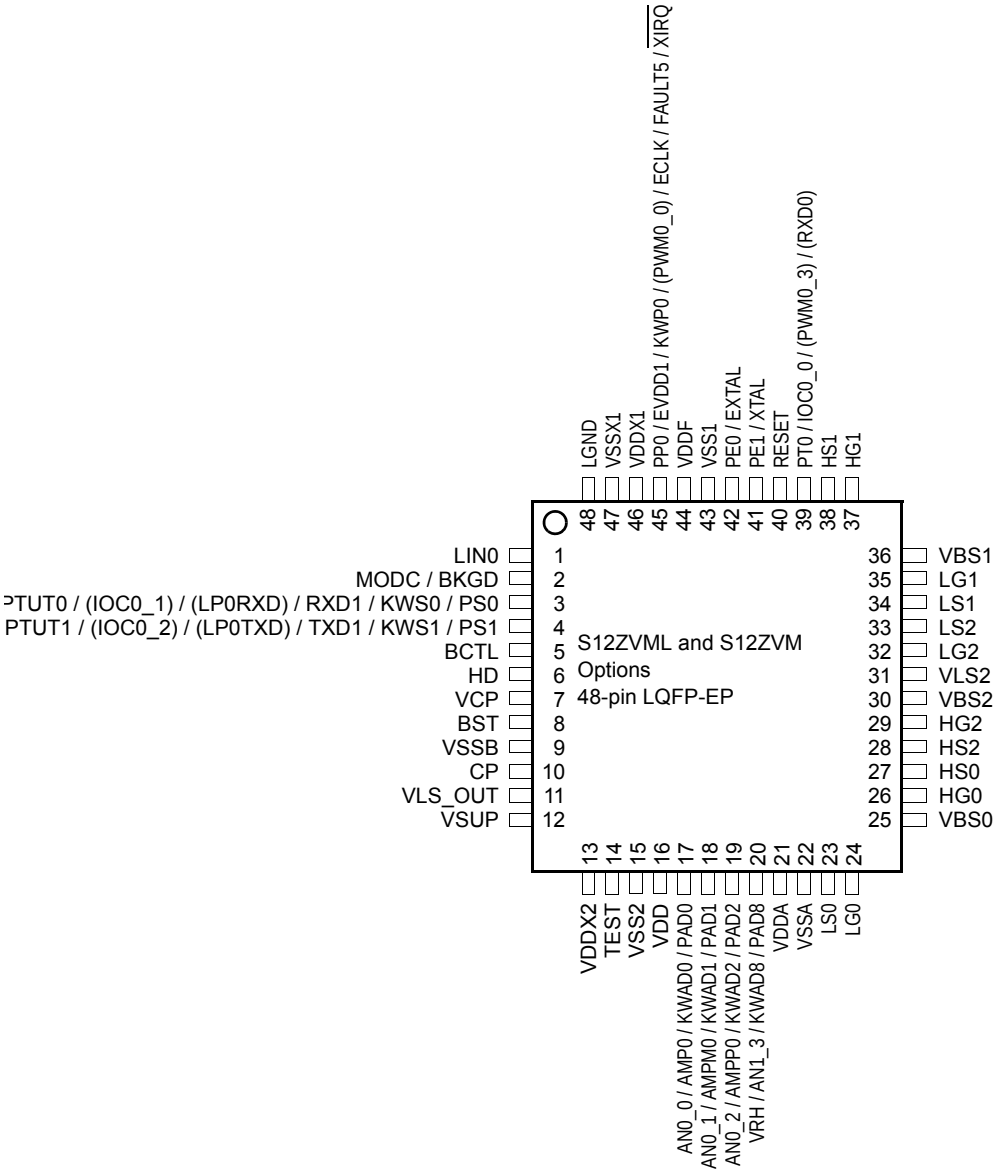


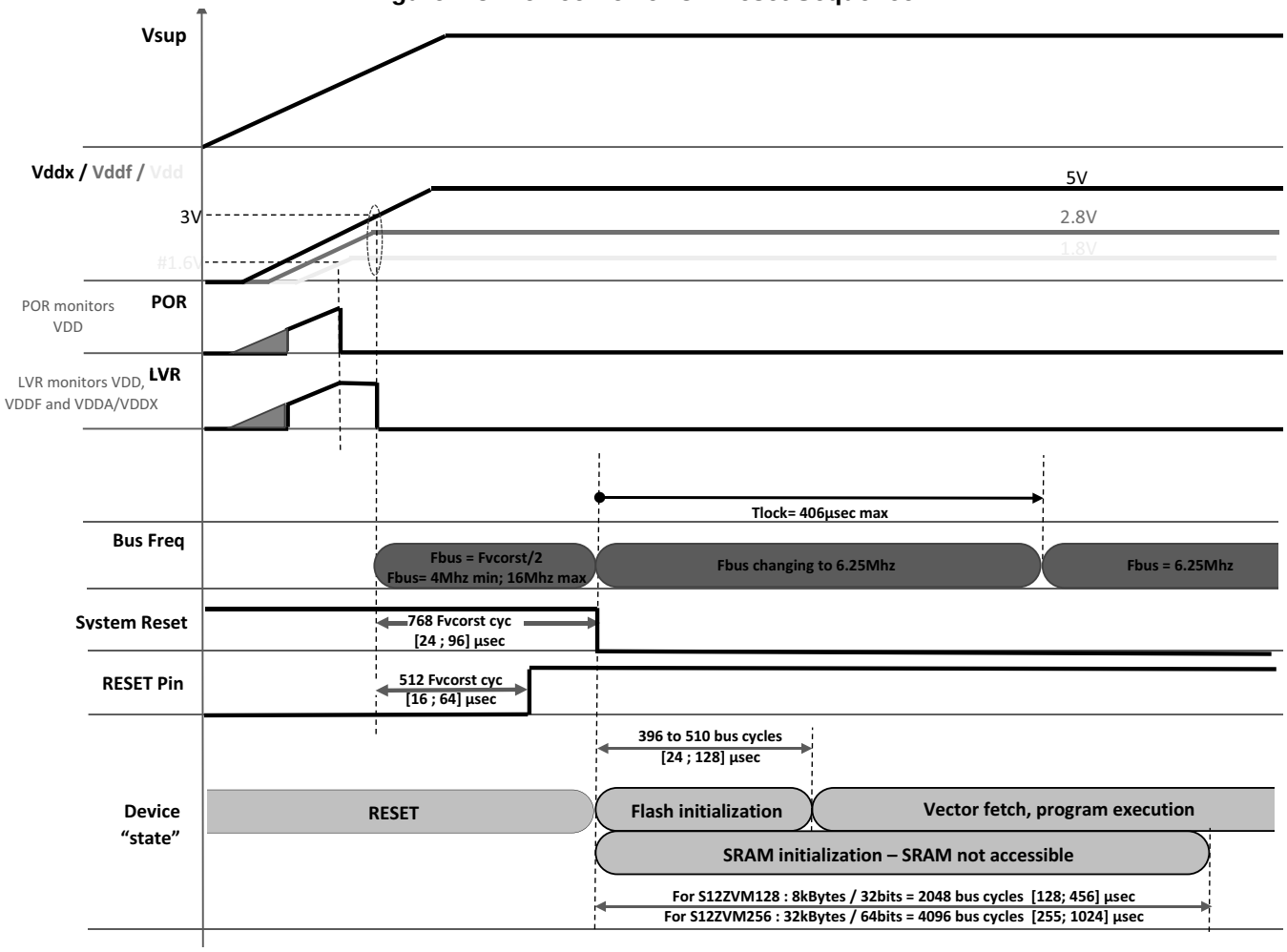
Figure 1-6. S12ZVM, S12ZVML Option 48-pin LQFP

is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

The system RAM arrays, including their ECC syndromes, are initialized following a power on reset. All other RAM arrays are not initialized out of any type of reset. With the exception of a power-on-reset the RAM content is unaltered by a reset occurrence.

The power on reset sequence including flash and SRAM initialization is shown in Figure 1-8

Figure 1-8. Device Power On Reset Sequence

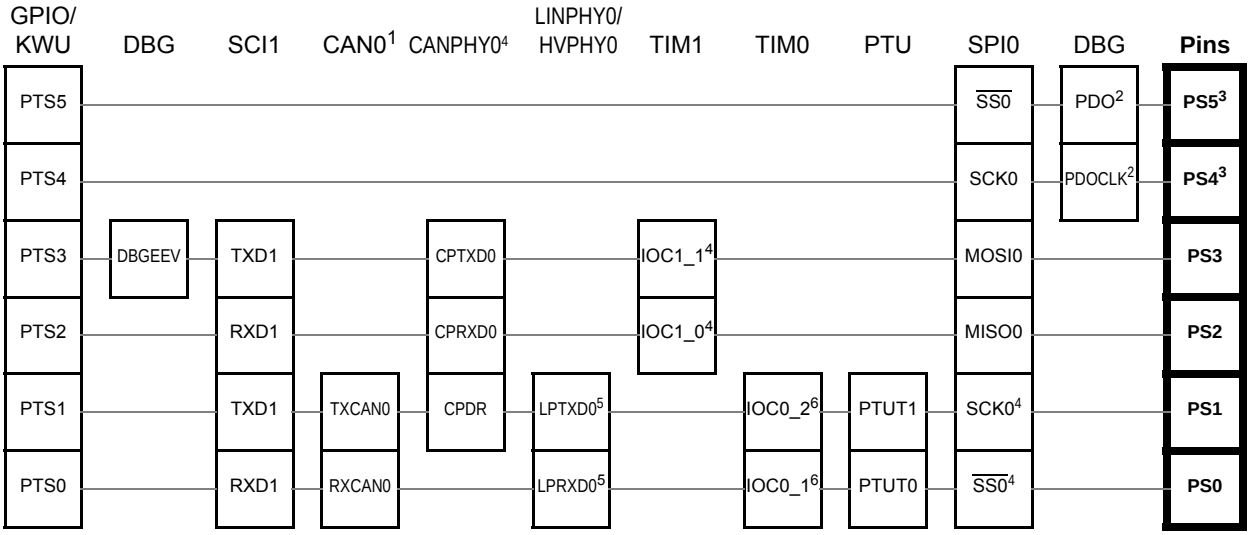


1.12 Module device level dependencies

1.12.1 CPMU COP and GDU Configuration

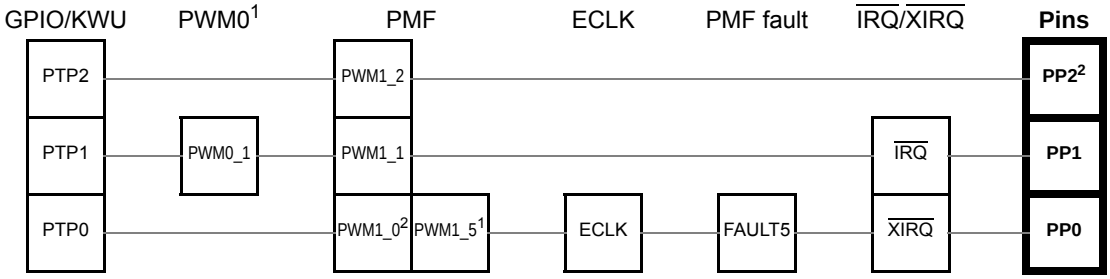
The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register are loaded from the Flash configuration field byte at global address 0xFF_FE0E during the flash initialization phase of the

- Port S



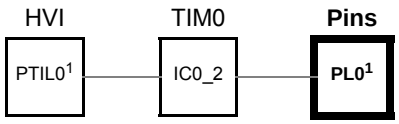
1. Only available for ZVMC256, ZVMC128, ZVML128, ZVMC64, ZVML64, and ZVML32
2. Only available for ZVMC128, ZVML128, ZVMC64, ZVML64, and ZVML32
3. Not available for ZVMC256
4. Only available for ZVMC256
5. Only available for ZVML128, ZVML64, ZVML32, ZVML31, ZVM32, and ZVM16
6. Only available for ZVMC256, ZVML31, ZVM32, and ZVM16

- Port P



1. Only available for ZVMC256
2. Not available for ZVMC256

- Port L



1. Only available for ZVMC256

Write: Anytime

Table 4-5. INT_CFADDR Field Descriptions

Field	Description
6–3 INT_CFADDR[6:3]	**Interrupt Request Configuration Data Register Select Bits** — These bits determine which of the 128 configuration data registers are accessible in the 8 register window at INT_CFDATA0–7. The hexadecimal value written to this register corresponds to the upper 4 bits of the vector number (multiply with 4 to get the vector address offset). If, for example, the value 0x70 is written to this register, the configuration data register block for the 8 interrupt vector requests starting with vector at address (vector base + (0x70*4 = 0x0001C0)) is selected and can be accessed as INT_CFDATA0–7.

4.3.2.3 Interrupt Request Configuration Data Registers (INT_CFDATA0–7)

The eight register window visible at addresses INT_CFDATA0–7 contains the configuration data for the block of eight interrupt requests (out of 128) selected by the interrupt configuration address register (INT_CFADDR) in ascending order. INT_CFDATA0 represents the interrupt configuration data register of the vector with the lowest address in this block, while INT_CFDATA7 represents the interrupt configuration data register of the vector with the highest address, respectively.

Address: 0x000018

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1(1)

= Unimplemented or Reserved

Figure 4-5. Interrupt Request Configuration Data Register 0 (INT_CFDATA0)

1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x000019

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1(1)

= Unimplemented or Reserved

Figure 4-6. Interrupt Request Configuration Data Register 1 (INT_CFDATA1)

1. Please refer to the notes following the PRIOLVL[2:0] description below.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0128-0x012F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0130	DBGCCTL	R	0	NDB	INST	0	RW	RWE	reserved	COMPE
		W								
0x0131-0x0134	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0135	DBGCAH	R	DBGCA[23:16]							
		W								
0x0136	DBGCAM	R	DBGCA[15:8]							
		W								
0x0137	DBGCAL	R	DBGCA[7:0]							
		W								
0x0138	DBGCD0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x0139	DBGCD1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013A	DBGCD2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013B	DBGCD3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x013C	DBGCDM0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x013D	DBGCDM1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013E	DBGCDM2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013F	DBGCDM3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								

Figure 6-2. Quick Reference to DBG Registers

When using the AB comparator pair for a range comparison, the data bus can be used for qualification by using the comparator A data and data mask registers. Similarly when using the CD comparator pair for a range comparison, the data bus can be used for qualification by using the comparator C data and data mask registers. The DBGACTL/DBGCCTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL/DBGDCTL bits are ignored. The DBGACTL/DBGCCTL COMPE/INST bits are used for range comparisons. The DBGBCTL/DBGDCTL COMPE/INST bits are ignored in range modes.

6.4.2.4.1 Inside Range (CompAC_Addr ≤ address ≤ CompBD_Addr)

In the Inside Range comparator mode, either comparator pair A and B or comparator pair C and D can be configured for range comparisons by the control register (DBGC2). The match condition requires a simultaneous valid match for both comparators. A match condition on only one comparator is not valid.

6.4.2.4.2 Outside Range (address < CompAC_Addr or address > CompBD_Addr)

In the Outside Range comparator mode, either comparator pair A and B or comparator pair C and D can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. Outside range mode in combination with opcode address matches can be used to detect if opcodes are from an unexpected range.

NOTE

When configured for data access matches, an outside range match would typically occur at any interrupt vector fetch or register access. This can be avoided by setting the upper or lower range limit to $FFFFFF or $000000 respectively. Interrupt vector fetches do not cause opcode address matches.

6.4.3 Events

Events are used as qualifiers for a state sequencer change of state. The state control register for the current state determines the next state for each event. An event can immediately initiate a transition to the next state sequencer state whereby the corresponding flag in DBGSR is set.

6.4.3.1 Comparator Match Events

6.4.3.1.1 Opcode Address Comparator Match

The comparator is loaded with the address of the selected instruction and the comparator control register INST bit is set. When the opcode reaches the execution stage of the instruction queue a match occurs just before the instruction executes, allowing a breakpoint immediately before the instruction boundary. The comparator address register must contain the address of the first opcode byte for the match to occur. Opcode address matches are data independent thus the RWE and RW bits are ignored. CPU compares are disabled when BDM becomes active.

Table 8-16. COP Watchdog Rates if COPOSCSEL1=1.

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is ACLK divided by 2)
0	0	0	COP disabled
0	0	1	2^{7}
0	1	0	2^{9}
0	1	1	2^{11}
1	0	0	2^{13}
1	0	1	2^{15}
1	1	0	2^{16}
1	1	1	2^{17}

9.4 Signal Description

This section lists all inputs to the ADC12B_LBA block.

9.4.1 Detailed Signal Descriptions

9.4.1.1 AN*x* (*x* = *n*,..., 2, 1, 0)

This pin serves as the analog input Channel *x*. The maximum input channel number is *n*. Please refer to the device reference manual for the maximum number of input channels.

9.4.1.2 VRH_0, VRH_1, VRH_2, VRL_0, VRL_1

VRH_0/1/2 are the high reference voltages, VRL0/1 are the low reference voltages for a ADC conversion selectable on a conversion command basis. Please refer to the device overview information for availability and connectivity of these pins.

VRH_2 is only available on ADC12B_LBA V3.

VRL_1 is only available on ADC12B_LBA V1 and V2.

See also Table 9-2.

9.4.1.3 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B_LBA block.

9.5.2.3 ADC Status Register (ADCSTS)

It is important to note that if flag DBECC_ERR is set the ADC ceases operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. An ADC Soft-Reset clears bits CSL_SEL and RVL_SEL.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
W								
Reset	0	0	0	0	1	0	0	0

= Unimplemented or Reserved

Figure 9-6. ADC Status Register (ADCSTS)

Read: Anytime

Write:

- Bits CSL_SEL and RVL_SEL anytime if bit ADC_EN is clear or bit SMOD_ACC is set
- Bits DBECC_ERR and READY not writable

Table 9-6. ADCSTS Field Descriptions

Field	Description
7 CSL_SEL	**Command Sequence List Select bit** — This bit controls and indicates which ADC Command List is active. This bit can only be written if ADC_EN bit is clear. This bit toggles in CSL double buffer mode when no conversion or conversion sequence is ongoing and bit LDOK is set and bit RSTA is set. In CSL single buffer mode this bit is forced to 1'b0 by bit CSL_BMOD. 0 ADC Command List 0 is active. 1 ADC Command List 1 is active.
6 RVL_SEL	**Result Value List Select Bit** — This bit controls and indicates which ADC Result List is active. This bit can only be written if bit ADC_EN is clear. After storage of the initial Result Value List this bit toggles in RVL double buffer mode whenever the conversion result of the first conversion of the current CSL is stored or a CSL got aborted. In RVL single buffer mode this bit is forced to 1'b0 by bit RVL_BMOD. Please see also Section 9.3.1.2, "MCU Operating Modes for information regarding Result List usage in case of Stop or Wait Mode. 0 ADC Result List 0 is active. 1 ADC Result List 1 is active.
5 DBECC_ERR	**Double Bit ECC Error Flag** — This flag indicates that a double bit ECC error occurred during conversion command load or result storage and ADC ceases operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. This bit is cleared if bit ADC_EN is clear. 0 No double bit ECC error occurred. 1 A double bit ECC error occurred.
3 READY	**Ready For Restart Event Flag** — This flag indicates that ADC is in its idle state and ready for a Restart Event. It can be used to verify after exit from Wait Mode if a Restart Event can be issued and processed immediately without any latency time due to an ongoing Sequence Abort Event after exit from MCU Wait Mode (see also the Note in Section 9.3.1.2, "MCU Operating Modes). 0 ADC not in idle state. 1 ADC is in idle state.

Table 9-22. Conversion Interrupt Flag Select

CON_IF[15:1]	INTFLG_SEL[3]	INTFLG_SEL[2]	INTFLG_SEL[1]	INTFLG_SEL[0]	Comment
0x0000	0	0	0	0	No flag set
0x0001	0	0	0	1	Only one flag can be set (one hot coding)
0x0002	0	0	1	0	
0x0004	0	0	1	1	
0x0008	0	1	0	0	
0x0010	0	1	0	1	
....	...	...	...	...	
0x0800	1	1	0	0	
0x1000	1	1	0	1	
0x2000	1	1	1	0	
0x4000	1	1	1	1	

13.3.3.3 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.

Module Base + 0x00XC

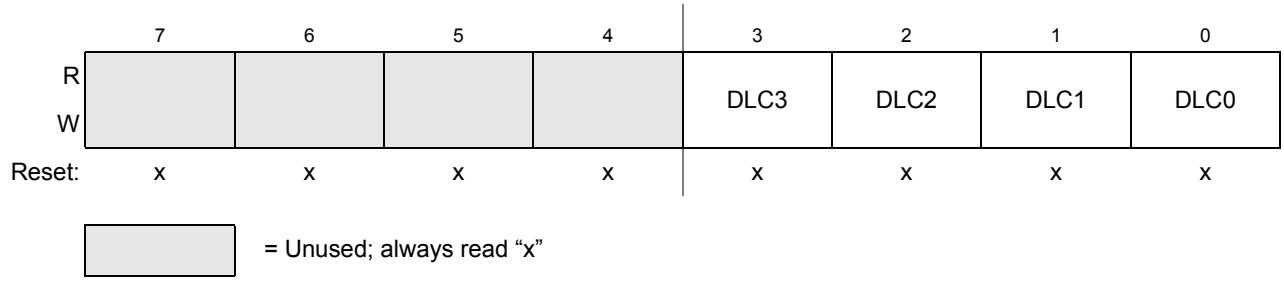


Figure 13-35. Data Length Register (DLR) — Extended Identifier Mapping

Table 13-33. DLR Register Field Descriptions

Field	Description
3-0 DLC[3:0]	**Data Length Code Bits** — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 13-34 shows the effect of setting the DLC bits.

Table 13-34. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

13.3.3.4 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.

in center-aligned operation and at the end of cycle in edge-aligned operation. Using this mode requires external circuitry to sense current direction.

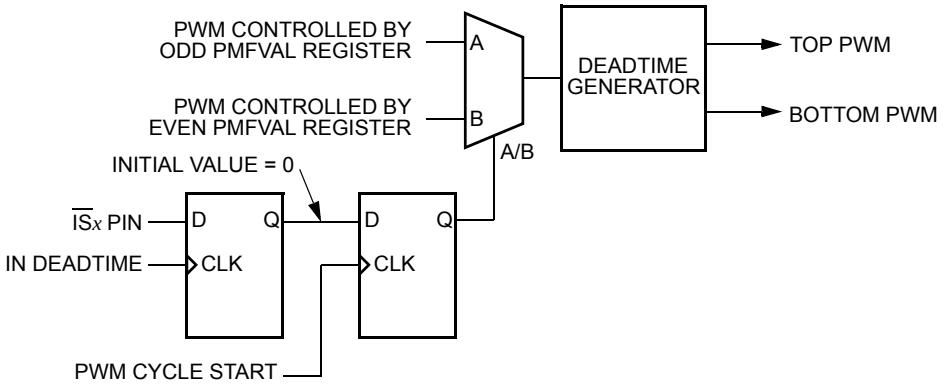


Figure 15-58. Internal Correction Logic when ISENS = 10

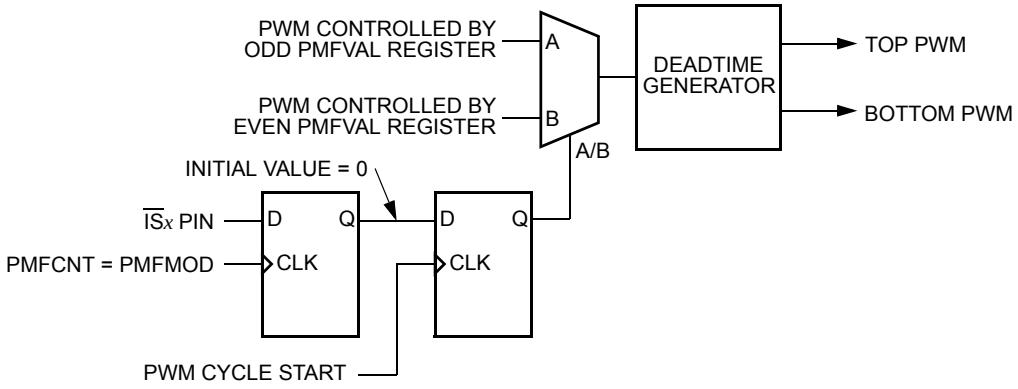


Figure 15-59. Internal Correction Logic when ISENS = 11

NOTE

Values latched on the $\overline{IS}x$ inputs are buffered so only one PWM register is used per PWM cycle. If a current status changes during a PWM period, the new value does not take effect until the next PWM period.

When initially enabled by setting the PWMEN bit, no current status has previously been sampled. PWM value registers one, three, and five initially control the three PWM pairs when configured for current status correction.

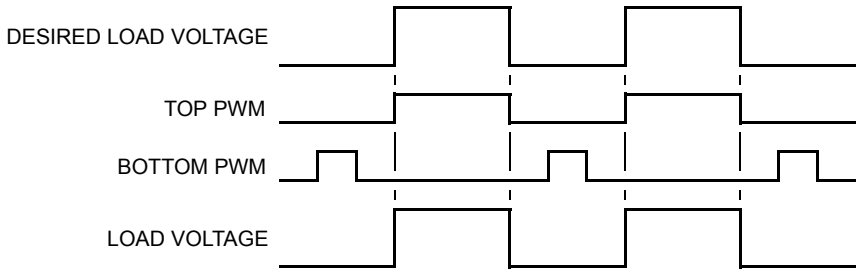


Figure 15-60. Correction with Positive Current

15.4.12 PWM Generator Loading

15.4.12.1 Load Enable

The load okay bit, LDOK, enables loading the PWM generator with:

- A prescaler divisor—from the PRSC bits in PMFFQC register
- A PWM period—from the PWM counter modulus registers
- A PWM pulse width—from the PWM value registers

LDOK prevents reloading of these PWM parameters before software is finished calculating them. Setting LDOK allows the prescaler bits, PMFMOD and PMFVAL registers to be loaded into a set of buffers. The loaded buffers are used by the PWM generator at the beginning of the next PWM reload cycle. Set LDOK by reading it when it is a logic zero and then writing a logic one to it. After the PWM reload event, LDOK is automatically cleared.

If LDOK is set in the same cycle as the PWM reload event occurs, then the current buffers will be used and the LDOK is valid at the next PWM reload event. See Figure 15-71.

If an asserted LDOK bit is attempted to be set again one cycle prior to the PWM reload event, then the buffers will loaded and LDOK will be cleared automatically. Else if the write access to the set LDOK bit occurs in the same cycle with the reload event, the buffers will also be loaded but the LDOK remains valid also for the next PWM reload event. See Figure 15-72.

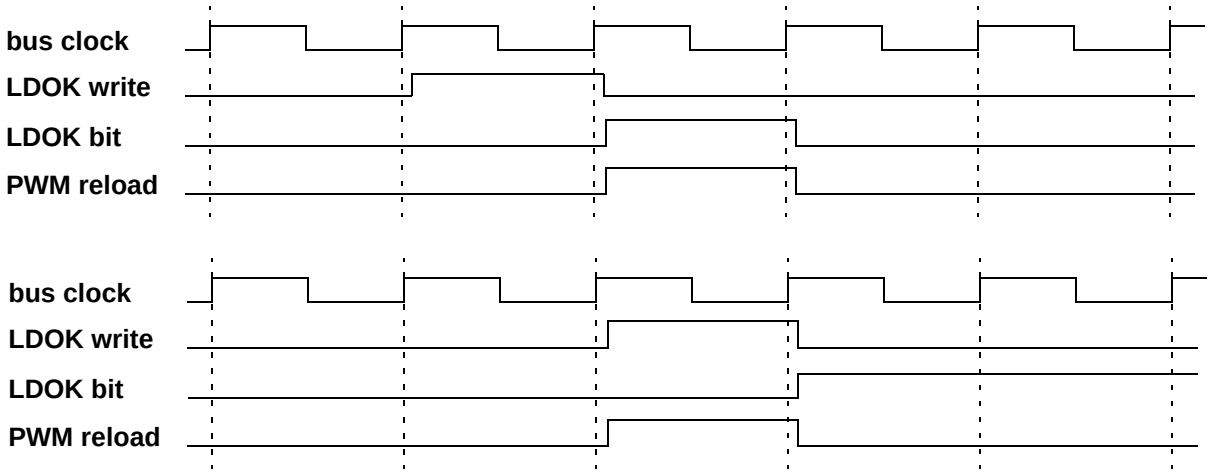


Figure 15-71. Setting cleared LDOK bit at PWM reload event

Table 16-3. SCICR1 Field Descriptions (continued)

Field	Description
1 PE	**Parity Enable Bit** — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	**Parity Type Bit** — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 16-4. Loop Functions

LOOPS	RSRC	Function
0	x	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0007 Reserved	R								
	W								

= Unimplemented or Reserved

Figure 17-2. SPI Register Summary

17.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

17.3.2.1 SPI Control Register 1 (SPICR1)

Module Base +0x0000

	7	6	5	4	3	2	1	0
R W	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

Figure 17-3. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

Table 17-2. SPICR1 Field Descriptions

Field	Description
7 SPIE	**SPI Interrupt Enable Bit** — This bit enables SPI interrupt requests, if SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	**SPI System Enable Bit** — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	**SPI Transmit Interrupt Enable** — This bit enables SPI interrupt requests, if SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	**SPI Master/Slave Mode Select Bit** — This bit selects whether the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode. 1 SPI is in master mode.

19.1.1 Features

The LIN Physical Layer module includes the following distinctive features:

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4 kbit/s, 20 kbit/s and Fast Mode (up to 250 kbit/s).
- Switchable 34 kΩ/330 kΩ pullup resistors (in shutdown mode, 330 kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.
- Automatic transmitter shutdown in case of an overcurrent or TxD-dominant timeout.
- Fulfills the OEM “Hardware Requirements for LIN (CAN and FlexRay) Interfaces in Automotive Applications” v1.3.

The HV Physical Layer module includes the following distinctive features:

- Compliant with the ISO9141 (K-line) standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for: 5.2 kHz, 10 kHz and Fast Mode (up to 125 kHz).
- Switchable 34 kΩ/330 kΩ pullup resistors (in shutdown mode, 330 kΩ only).
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.

The LIN/HV transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pullup resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

19.1.2 Modes of Operation

The LIN/HV Physical Layer can operate in the following four modes:

1. Shutdown Mode

   The LIN/HV Physical Layer is fully disabled. No wake-up functionality is available. The internal pullup resistor is replaced by a high ohmic one (330 kΩ) to maintain the LIN Bus pin in the recessive state. All registers are accessible.

Table 20-65. Program EEPROM Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the EEPROM block
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.16 Erase EEPROM Sector Command

The Erase EEPROM Sector operation will erase all addresses in a sector of the EEPROM block.

Table 20-66. Erase EEPROM Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x12	Global address [23:16] to identify EEPROM block
FCCOB1	Global address [15:0] anywhere within the sector to be erased. See Section 20.1.2.2 for EEPROM sector size.	

Upon clearing CCIF to launch the Erase EEPROM Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase EEPROM Sector operation has completed.

Table 20-67. Erase EEPROM Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied see Table 20-3
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table A-1. Power Supplies

Mnemonic	Nominal Voltage	Description
VDD	1.8 V	1.8V core supply voltage generated by on chip voltage regulator
VSS1	0 V	Ground pin for 2.8V flash supply voltage generated by on chip voltage regulator
VSS2	0 V	Ground pin for 1.8V core supply voltage generated by on chip voltage regulator
VDDF	2.8 V	2.8V flash supply voltage generated by on chip voltage regulator
VDDX1 (1)	5.0 V	5V power supply output for I/O drivers generated by on chip voltage regulator
$VSSX_1$	0 V	Ground pin for I/O drivers
VDDX2	5.0 V	5V power supply output for I/O drivers generated by on chip voltage regulator
VDDA	5.0 V	5V Power supply for the analog-to-digital converter and for the reference circuit of the internal voltage regulator
VSSA	0 V	Ground pin for VDDA analog supply
LGND	0 V	Ground pin for LIN physical interface
HD	12 V	GDU Highside Drain. Also used as LIN supply, VLINSUP.
VSUP	12 V/18 V	External power supply for voltage regulator
VDDC	5 V	Power supply output for CANPHY
VDDS2	5 V	Power supply output (5V) for external sensors
VDDS1	5 V	Power supply output (5V) for external sensors
VLS_OUT	11 V	GDU voltage regulator output for low side FET-predriver power supply.
VSSB	0 V	Ground pin for boost supply.

1. All VDDX pins are internally connected by metal

NOTE

VDDA is connected to VDDX pins by diodes for ESD protection such that VDDX must not exceed VDDA by more than a diode voltage drop. VSSA and VSSX are connected by anti-parallel diodes for ESD protection.

A.1.2 Pins

There are 4 groups of functional pins.

A.1.2.1 General Purpose I/O Pins (GPIO)

The I/O pins have a level in the range of 4.5V to 5.5V. This class of pins is comprised of all port I/O pins, BKGD and the $\overline{\text{RESET}}$ pins.

A.1.2.2 High Voltage Pins

These consist of the LIN, BST, HD, VCP, CP, VLS_OUT, VLS[2:0], VBS[2:0], HG[2:0], HS[2:0], LG[2:0], LD[2:0], PL0, CANH0, CANL0, SPLIT0, VDDS1, VDDS2, BCTLS1, BCTLS2, SNPS1,

NOTE

Please refer to the temperature rating of the device with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to Section A.1.8, “Power Dissipation and Thermal Characteristics”.

Table A-6. Operating Conditions

Num	Rating	Symbol	Min	Typ	Max	Unit
1	Voltage regulator and LINPHY supply voltage(1)	V_{SUP}	3.5	12	40	V
2	Voltage difference V_{DDX} to V_{DDA}	ΔVDDX	–0.1	—	0.1	V
3	Voltage difference V_{SSX} to V_{SSA}	ΔVSSX	–0.1	—	0.1	V
	Digital logic supply voltage	V_{DD}	1.72	1.8	1.98	V
4	Oscillator	f_{osc}	4	—	20	MHz
5	Bus frequency(2) -40°C < T_j < 150°C 150°C < T_j < 175°C (Temp option W only)	f_{bus}	(4)	— —	50 40	MHz
6	Bus frequency without flash wait states -40°C < T_j < 150°C 150°C < T_j < 175°C (Temp option W only)	f_{WSTAT}	— —	— —	25 20	MHz
7a	Operating junction temperature range Operating ambient temperature range(3) (option V)	T_J T_A	–40 –40	— —	125 105	°C
7b	Operating junction temperature range Operating ambient temperature range(3) (option M)	T_J T_A	–40 –40	— —	150 125	°C
7c	Operating junction temperature range Operating ambient temperature range(3) (option W)	T_J T_A	–40 –40	— —	175 150	°C

1. Normal operating range is 5.5 V - 18 V. Continuous operation at 40 V is not allowed. Only Transient Conditions (Load Dump) single pulse t_{max}<400 ms. Operation down to 3.5V is guaranteed without reset, however some electrical parameters are specified only in the range above 4.5 V. Operation in the range 20V<VSUP<26.5V is limited to 1 hour over lifetime of the device. In this range the device continues to function but electrical parameters are degraded.

2. The flash program and erase operations must configure f_{NVMOP} as specified in the NVM electrical section.

3. Please refer to Section A.1.8, “Power Dissipation and Thermal Characteristics” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

4. Refer to f_{ATDCLK} for minimum ADC operating frequency. This is derived from the bus clock.

NOTE

Operation is guaranteed when powering down until low voltage reset assertion.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

Table F-4. FTMRZ32K128 NVM Timing Characteristics (Junction Temperature From 150°C To +175°C)

Derivatives ZVML31, ZVM32, ZVM16									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min(1)**	**Typ(2)**	**Max(3)**	**Worst (4)**	**Unit**
1	Bus frequency	—	1	f_{NVMBUS}	1	40	40	40	MHz
2	NVM Operating frequency	1	—	f_{NVMOP}	0.8	1.0	1.05	1.05	MHz
3	Erase Verify All Blocks	0	8992	t_{RD1ALL}	0.22	0.22	0.45	17.98	ms
4	Erase Verify Block (Pflash)	0	8750	t_{RD1BLK_P}	0.22	0.22	0.44	17.50	ms
5	Erase Verify Block (EEPROM)	0	631	t_{RD1BLK_D}	0.02	0.02	0.03	1.26	ms
6	Erase Verify P-Flash Section	0	511	t_{RD1SEC}	0.01	0.01	0.03	1.02	ms
7	Read Once	0	481	t_{RDONCE}	12.03	12.03	12.03	481.00	us
8	Program P-Flash (4 Word)	164	3136	t_{PGM_4}	0.23	0.24	0.48	12.75	ms
9	Program Once	164	3107	$t_{PGMONCE}$	0.23	0.24	0.24	3.31	ms
10	Erase All Blocks	100066	9455	t_{ERSALL}	95.54	100.30	100.54	143.99	ms
11	Erase Flash Block (Pflash)	100060	9119	t_{ERSBLK_P}	95.52	100.29	100.52	143.31	ms
12	Erase Flash Block (EEPROM)	100060	970	t_{ERSBLK_D}	95.32	100.08	100.11	127.02	ms
13	Erase P-Flash Sector	20015	927	t_{ERSPG}	19.09	20.04	20.06	26.87	ms
14	Unsecure Flash	100066	9533	t_{UNSECU}	95.54	100.30	100.54	144.15	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	12.33	12.33	12.33	493.00	us
16	Set User Margin Level	0	439	t_{MLOADU}	10.98	10.98	10.98	439.00	us
17	Set Factory Margin Level	0	448	t_{MLOADF}	11.20	11.20	11.20	448.00	us
18	Erase Verify EEPROM Sector	0	583	$t_{DRD1SEC}$	0.01	0.01	0.03	1.17	ms
19	Program EEPROM (1 Word)	68	1678	t_{DPGM_1}	0.11	0.11	0.24	6.80	ms
20	Program EEPROM (2 Word)	136	2702	t_{DPGM_2}	0.20	0.20	0.41	10.98	ms
21	Program EEPROM (3 Word)	204	3726	t_{DPGM_3}	0.29	0.30	0.58	15.16	ms
22	Program EEPROM (4 Word)	272	4750	t_{DPGM_4}	0.38	0.39	0.75	19.34	ms
23	Erase EEPROM Sector	5015	817	t_{DERSPG}	4.80	5.04	20.41	38.96	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	11.88	11.88	11.88	475.00	us

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4. Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging