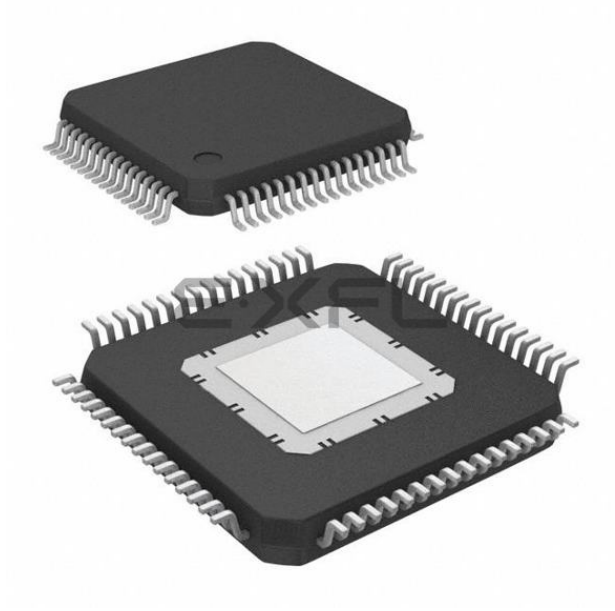

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Chapter 9
Analog-to-Digital Converter (ADC12B_LBA)

2.3.2.1 Module Routing Register 0 (MODRR0)

Address 0x0200 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	SPI0SSRR	SPI0RR	SCI1RR	S0L0RR2-0[2]		
W								
	—	—	SPI0 $\overline{SS0}$	SPI0	SCI1	SCI0-LINPHY0/HVPHY0 (see Figure 2-2)		
Reset	0	0	0	0	0	0	0	0

Figure 2-1. Module Routing Register 0 (MODRR0)

1. Read: Anytime
   Write: Once in normal, anytime in special mode
2. Only available for ZVML128, ZVML64, ZVML32, and ZVML31

Table 2-9. MODRR0 Routing Register Field Descriptions

Field	Description
5 SPI0SSRR	**Module Routing Register** — SPI0 SS0 routing **Note:** This bit takes precedence over SPI0RR. 1 $\overline{SS0}$ on PAD6 0 $\overline{SS0}$ based on SPI0RR
4 SPI0RR	**Module Routing Register** — SPI0 routing 1 MISO0 on PT0; MOSI0 on PT1; SCK0 on PT2; $\overline{SS0}$ on PT3 or on pin selected by SPI0SSRR 0 MISO0 on PS2; MOSI0 on PS3; SCK0 on PS4 (PS1 for S12ZVMC256); $\overline{SS0}$ on PS5 (PS0 for S12ZVMC256) or on pin selected by SPI0SSRR
3 SCI1RR	**Module Routing Register** — SCI1 routing 1 TXD1 on PS3; RXD1 on PS2 0 TXD1 on PS1; RXD1 on PS0
2-0 S0L0RR2-0	**Module Routing Register** — SCI0-LINPHY0/HVPHY0 routing Selection of SCI0-LINPHY0/HVPHY0 interface routing options to support probing and conformance testing. Refer to Figure 2-2 for an illustration and Table 2-10 for preferred settings. SCI0 must be enabled for TXD0 routing to take effect on pins. LINPHY0/HVPHY0 must be enabled for LPRXD0 and LPDC0 routings to take effect on pins.

2.3.4.4 Port L Input Register (PTIL)

Address 0x0331 Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTIL0[2]
W								
Reset	0	0	0	0	0	0	0	-

Figure 2-26. Port L Input Register (PTIL)

1. Read: Anytime
   Write: No Write
2. Only available for S12ZVMC256

Table 2-30. PTIL - Register Field Descriptions

Field	Description
0 PTIL0	**Port Input Data Register Port L —** A read returns the synchronized input state if the associated pin is used in digital mode, that is the related DIENL bit is set to 1 and the pin is not used in analog mode (PTAENL[PTAENL0]=0). See Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL)”. A one is read in any other case[1].

1. Refer to PTTEL bit description in Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL) for an override condition.

2.3.4.5 Port L Pull Select Register (PTPSL)

Address 0x0333 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTPSL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-27. Port L Pull Select Register (PTPSL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-31. PTPSL Register Field Descriptions

Field	Description
1-0 PTPSL0	**Port L Pull Select —** This bit selects a pull device on the HVI pin in analog mode for open input detection. By default a pulldown device is active as part of the input voltage divider. If this bit set to 1 and PTTEL=1 and not in stop mode a pullup to a level close to V_{DDX} takes effect and overrides the weak pulldown device. Refer to Section 2.5.2, “Open Input Detection on HVI”). 1 Pullup enabled 0 Pulldown enabled

2.3.4.8 Port L ADC Direct Register (PTADIRL)

Address 0x033B Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PTADIRL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-30. Port L ADC Direct Register (PTADIRL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-34. PTADIRL Register Field Descriptions

Field	Description
1-0 PTADIRL0	**Port L ADC Direct Connection** — This bit connects the analog input signal directly to the ADC channel bypassing the voltage divider. This bit takes effect only in analog mode (PTAENL=1). 1 Input pin directly connected to ADC channel 0 Input voltage divider active on analog input to ADC channel

2.3.4.9 Port L Digital Input Enable Register (DIENL)

Address 0x33C Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	DIENL0[2]
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-31. Port L Digital Input Enable Register (DIENL)

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

Table 2-35. DIENL Register Field Descriptions

Field	Description
0 DIENL0	**Digital Input Enable Port L** — Input buffer control This bit controls the HVI digital input function. If set to 1 the input buffers are enabled and the pin can be used with the digital function. If the analog input function is enabled (PTAENL[PTAENL0]=1) the input buffer of the selected HVI pin is forced off[1] in run mode and is released to be active in stop mode only if DIENL=1. 1 Associated pin digital input is enabled if not used as analog input in run mode[1] 0 Associated pin digital input is disabled[1]

1. Refer to PTTEL bit description in Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL) for an override condition.

3.3.2.2 Error Code Register (MMCECH, MMCECL)

Address: 0x0080 (MMCECH)

	7	6	5	4	3	2	1	0
R W	ITR[3:0]				TGT[3:0]			
Reset	0	0	0	0	0	0	0	0

Address: 0x0081 (MMCECL)

	7	6	5	4	3	2	1	0
R W	ACC[3:0]				ERR[3:0]			
Reset	0	0	0	0	0	0	0	0

Figure 3-5. Error Code Register (MMCEC)

Read: Anytime

Write: Write of 0xFFFF to MMCECH:MMCECL resets both registers to 0x0000

Table 3-5. MMCECH and MMCECL Field Descriptions

Field	Description
7-4 (MMCECH) ITR[3:0]	**Initiator Field** — The ITR[3:0] bits capture the initiator which caused the access violation. The initiator is captured in form of a 4 bit value which is assigned as follows: 0: none (no error condition detected) 1: S12ZCPU 2: reserved 3: ADC0 4: ADC1 5: PTU 6-15: reserved
3-0 (MMCECH) TGT[3:0]	**Target Field** — The TGT[3:0] bits capture the target of the faulty access. The target is captured in form of a 4 bit value which is assigned as follows: 0: none 1: register space 2: RAM 3: EEPROM 4: program flash 5: IFR 6-15: reserved

8.3.2.17 Low Voltage Control Register (CPMULVCTL)

The CPMULVCTL register allows the configuration of the low-voltage detect features.

Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	VDDSIE(1)	LVDS	LVIE	LVIF
W								
Reset	0	0	0	0	0	U	0	U

The Reset state of LVDS and LVIF depends on the external supplied VDDA level

= Unimplemented or Reserved

Figure 8-23. Low Voltage Control Register (CPMULVCTL)

1. Only available in V10

Read: Anytime

Write: LVIE and LVIF are write anytime, LVDS is read only

Table 8-18. CPMULVCTL Field Descriptions

Field	Description
3 VDDSIE	VDDS Integrity Interrupt Enable Bit 0 Interrupt request is disabled. 1 Interrupt will be requested on VDDS integrity fails, that means whenever one of the following flags in CPMUVDDS register is set: SCS2IF, SCS1IF, LVS2IF, LVS1IF.
2 LVDS	**Low-Voltage Detect Status Bit** — This read-only status bit reflects the voltage level on VDDA. Writes have no effect. 0 Input voltage VDDA is above level V_{LVID} or RPM. 1 Input voltage VDDA is below level V_{LVIA} and FPM.
1 LVIE	Low-Voltage Interrupt Enable Bit 0 Interrupt request is disabled. 1 Interrupt will be requested whenever LVIF is set.
0 LVIF	**Low-Voltage Interrupt Flag** — LVIF is set to 1 when LVDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (LVIE = 1), LVIF causes an interrupt request. 0 No change in LVDS bit. 1 LVDS bit has changed.

Table 8-33. CPMUVDDS Field Descriptions (continued)

Field	Description
3 SCS2IF	**Short circuit VDDS2 Interrupt Flag** — SCS2IF is set to 1 when SCS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS2IF causes an interrupt request. 0 No change in SCS2 bit. 1 SCS2 bit has changed.
2 SCS1IF	**Short circuit VDDS1 Interrupt Flag** — SCS1IF is set to 1 when SCS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), SCS1IF causes an interrupt request. 0 No change in SCS1 bit. 1 SCS1 bit has changed.
1 LVS2IF	**Low-Voltage VDDS2 Interrupt Flag** — LVS2IF is set to 1 when LVDS2 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS2IF causes an interrupt request. 0 No change in LVDS2 bit. 1 LVDS2 bit has changed.
0 LVS1IF	**Low-Voltage VDDS1 Interrupt Flag** — LVS1IF is set to 1 when LVDS1 status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (VDDSIE = 1), LVS1IF causes an interrupt request. 0 No change in LVDS1 bit. 1 LVDS1 bit has changed.

error condition the trigger generator reloads the new data from the trigger list and starts to generate the trigger. During an async reload event the TGxREIF interrupt flag is not set.

If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data is ignored and the trigger generator reload error flag (TGxREIF) is not set.

14.4.5.5 Trigger Generator Timing Error

The PTU module requires a defined number of bus clock cycle to load the next trigger value from the memory. This load time defines the minimum possible distance between consecutive trigger values within one trigger list or the distance between the reload event and the first trigger value. If a smaller distance is used then it is possible, depending on device conditions, that the TGxTEIF event is generated. To evaluate the TGxTEIF handling a distance of 1 should be used. This value will generate the TGxTEIF condition independent from the device conditions.

For the specification of this number, please see the Device Overview chapter.

The trigger generator timing error flag (TGxTEIF) is set if the loaded trigger value is smaller than the current counter value. The execution of this trigger list is stopped until the next reload event. There are different reasons for the trigger generator error condition:

- reload time exceeds time of next trigger event
- reload time exceeds the time between two consecutive trigger values
- a subsequent trigger value is smaller than the predecessor trigger value

If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data are ignored and the trigger generator timing error flag (TGxTEIF) is not set.

If enabled (TGxEIE is set) an interrupt will be generated.

14.4.5.6 Trigger Generator Done

The trigger generator done flag (TGxDIF) is set if the loaded trigger value contains 0x0000 or if the number of maximum trigger events (32) was reached. Please note, that the time which is required to load the next trigger value defines the delay between the generation of the last trigger and the assertion of the done flag. If enabled (TGxDIE is set) an interrupt is generated.If the trigger value loaded from the memory contains double bit ECC errors (PTUDEEF flag is set) then the data are ignored and the trigger generator done flag (TGxDIF) is not set.

14.4.6 Debugging

To see the internal status of the trigger generator the register TGxLIST, TGxTNUM, and TGxTV can be used. The TGxLIST register shows the number of currently used list. The TGxTNUM shows the number of generated triggers since the last reload event. If the maximum number of triggers was generated then this register shows zero. The trigger value loaded from the memory to generate the next trigger event is visible inside the TGxTV register. If the execution of the trigger list is done then these registers are unchanged until the next reload event. The next PWM reload event clears the TGxTNUM register and toggles the used trigger list if PTULDOK was set.

15.3.2 Register Descriptions

15.3.2.1 PMF Configure 0 Register (PMFCFG0)

Address: Module Base + 0x0000 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
Reset	0	0	0	0	0	0	0	0

Figure 15-3. PMF Configure 0 Register (PMFCFG0)

1. Read: Anytime
   Write: This register cannot be modified after the WP bit is set

Table 15-6. PMFCFG0 Field Descriptions

Field	Description
7 WP	**Write Protect**— This bit enables write protection to be used for all write-protectable registers. While clear, WP allows write-protected registers to be written. When set, WP prevents any further writes to write-protected registers. Once set, WP can be cleared only by reset. 0 Write-protectable registers may be written 1 Write-protectable registers are write-protected
6 MTG	**Multiple Timebase Generators** — This bit determines the number of timebase counters used. This bit cannot be modified after the WP bit is set. If MTG is set, PWM generators B and C and registers 0x0028 – 0x0037 are availabled.The three generators have their own variable frequencies and are not synchronized. If MTG is cleared, PMF registers from 0x0028 – 0x0037 can not be written and read zeroes, and bits EDGEC and EDGEB are ignored. Pair A, Pair B, and Pair C PWMs are synchronized to PWM generator A and use registers from 0x0020 – 0x0027. 0 Single timebase generator 1 Multiple timebase generators
5 EDGEC	**Edge-Aligned or Center-Aligned PWM for Pair C —** This bit determines whether PWM4 and PWM5 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are center-aligned PWMs 1 PWM4 and PWM5 are edge-aligned PWMs
4 EDGEB	**Edge-Aligned or Center-Aligned PWM for Pair B —** This bit determines whether PWM2 and PWM3 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM2 and PWM3 are center-aligned PWMs 1 PWM2 and PWM3 are edge-aligned PWMs
3 EDGEA	**Edge-Aligned or Center-Aligned PWM for Pair A—** This bit determines whether PWM0 and PWM1 channels will use edge-aligned or center-aligned waveforms. It determines waveforms for Pair B and Pair C if the MTG bit is cleared. This bit cannot be modified after the WP bit is set. 0 PWM0 and PWM1 are center-aligned PWMs 1 PWM0 and PWM1 are edge-aligned PWMs
2 INDEPC	**Independent or Complementary Operation for Pair C**— This bit determines if the PWM channels 4 and 5 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set. 0 PWM4 and PWM5 are complementary PWM pair 1 PWM4 and PWM5 are independent PWMs

1. Read: Anytime
   Write: Anytime

Table 15-20. PMFCCTL Field Descriptions

Field	Description
5–4 ISENS[1:0]	**Current Status Sensing Method** — This field selects the top/bottom correction scheme, illustrated in Table 15-21. **Note:** The user must provide current sensing circuitry causing the voltage at the corresponding input to be low for positive current and high for negative current. The top PWMs are PWM 0, 2, and 4 and the bottom PWMs are PWM 1, 3, and 5. **Note:** The ISENS bits are not buffered. Changing the current status sensing method can affect the present PWM cycle.
2 IPOLC	**Current Polarity** — This buffered bit selects the PMF Value register for PWM4 and PWM5 in top/bottom software correction in complementary mode. 0 PMF Value 4 register in next PWM cycle 1 PMF Value 5 register in next PWM cycle
1 IPOLB	**Current Polarity** — This buffered bit selects the PMF Value register for PWM2 and PWM3 in top/bottom software correction in complementary mode. 0 PMF Value 2 register in next PWM cycle 1 PMF Value 3 register in next PWM cycle
0 IPOLA	**Current Polarity** — This buffered bit selects the PMF Value register for PWM0 and PWM1 in top/bottom software correction in complementary mode. 0 PMF Value 0 register in next PWM cycle 1 PMF Value 1 register in next PWM cycle

Table 15-21. Correction Method Selection

ISENS	Correction Method
00	No correction(1)
01	Manual correction
10	Current status sample correction on inputs $\overline{IS0}$, $\overline{IS1}$, and $\overline{IS2}$ during deadtime(2)
11	Current status sample on inputs $\overline{IS0}$, $\overline{IS1}$, and $\overline{IS2}$(3) At the half cycle in center-aligned operation At the end of the cycle in edge-aligned operation

1. The current status inputs can be used as general purpose input/output ports.

2. The polarity of the related $\overline{IS}$ input is latched when both the top and bottom PWMs are off. At the 0% and 100% duty cycle boundaries, there is no deadtime, so no new current value is sensed.

3. Current is sensed even with 0% or 100% duty cycle.

15.4.12.6 Synchronization Output (pmf_reload)

The PMF uses reload events to output a synchronization pulse, which can be used as an input to the timer module. A high-true pulse occurs for each PWM cycle start of the PWM, regardless of the state of the related LDOK bit or global load OK and load frequency.

15.4.13 Fault Protection

Fault protection can disable any combination of PWM outputs (for all FAULT0-5 inputs) or switch to output control register PMFOUTF on a fault event (for FAULT4-5 only). Faults are generated by an active level[1] on any of the FAULT inputs. Each FAULT input can be mapped arbitrarily to any of the PWM outputs.

In complementary mode, if a FAULT4 or FAULT5 event is programmed to switch to output control on a fault event resulting in a PWM active state on a particular output, then the transition will take place after deadtime insertion. Thus an asynchronous path to disable the PWM output is not available.

On a fault event the PWM generator continues to run.

The fault decoder affects the PWM outputs selected by the fault logic and the disable mapping register.

The fault protection is enabled even when the PWM is not enabled; therefore, a fault will be latched in and will be cleared in order to prevent an interrupt when the PWM is enabled.

15.4.13.1 Fault Input Sample Filter

Each fault input has a sample filter to test for fault conditions. After every bus cycle setting the FAULT*m* input at logic zero, the filter synchronously samples the input once every four bus cycles. QSMP determines the number of consecutive samples that must be logic one for a fault to be detected. When a fault is detected, the corresponding FAULT*m* flag, FIF*m*, is set. FIF*m* can only be cleared by writing a logic one to it.

If the FIE*m*, FAULT*m* interrupt enable bit is set, the FIF*m* flag generates a CPU interrupt request. The interrupt request latch remains set until:

- Software clears the FIF*m* flag by writing a logic one to it
- Software clears the FIE*m* bit by writing a logic zero to it
- A reset occurs

15.4.13.2 Automatic Fault Recovery

Setting a fault mode bit, FMOD*m*, configures faults from the FAULT*m* input for automatically reenabling the PWM outputs.

When FMOD*m* is set, disabled PWM outputs are enabled when the FAULT*m* input returns to logic zero and a new PWM half cycle begins. See Figure 15-83. Clearing the FIF*m* flag does not affect disabled PWM outputs when FMOD*m* is set.

1. The active input level may be defined or programmable at SoC level. The default for internally connected resources is active-high. For availability and configurability of fault inputs on pins refer to the device overview section.

18.1.2 Modes of Operation

The GDU module behaves as follows in the system power modes:

1. Run mode

   All features are available.

2. Wait mode
   All features are available.

3. Stop mode

   The GDU is disabled in stop mode. The high-side drivers, low-side drivers, charge pump, voltage regulator, boost circuit, and current sense amplifier are switched off. The GDU will weakly pull the gates of the MOSFET to their source potential. On entering stop mode the GDUE register bits are cleared. GFDE=0, GCPE=0, GBOE=0, GCSE1=0 and GCSE0=0.

NOTE

The device does not support putting the MOSFET in specific state during stop mode as GDU charge pump clock is not running. This means device can not be put in stop mode if FETs needs to be in specific state to protect the system from external energy supply (e.g. externally driven motor-generator).

20.3.2.13 Flash Common Command Object Registers (FCCOB)

The FCCOB is an array of six words. Byte wide reads and writes are allowed to the FCCOB registers.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 20-18. Flash Common Command Object 0 High Register (FCCOB0HI)

Offset Module Base + 0x000D

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 20-19. Flash Common Command Object 0 Low Register (FCCOB0LO)

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 20-20. Flash Common Command Object 1 High Register (FCCOB1HI)

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 20-21. Flash Common Command Object 1 Low Register (FCCOB1LO)

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 20-22. Flash Common Command Object 2 High Register (FCCOB2HI)

Table 20-36. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if an invalid global address [23:0] is supplied see Table 20-3)
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

20.4.7.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 20-37. Erase Verify P-Flash Section Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x03	Global address [23:16] of a P-Flash block
FCCOB1	Global address [15:0] of the first phrase to be verified	
FCCOB2	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 20-38. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied see Table 20-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

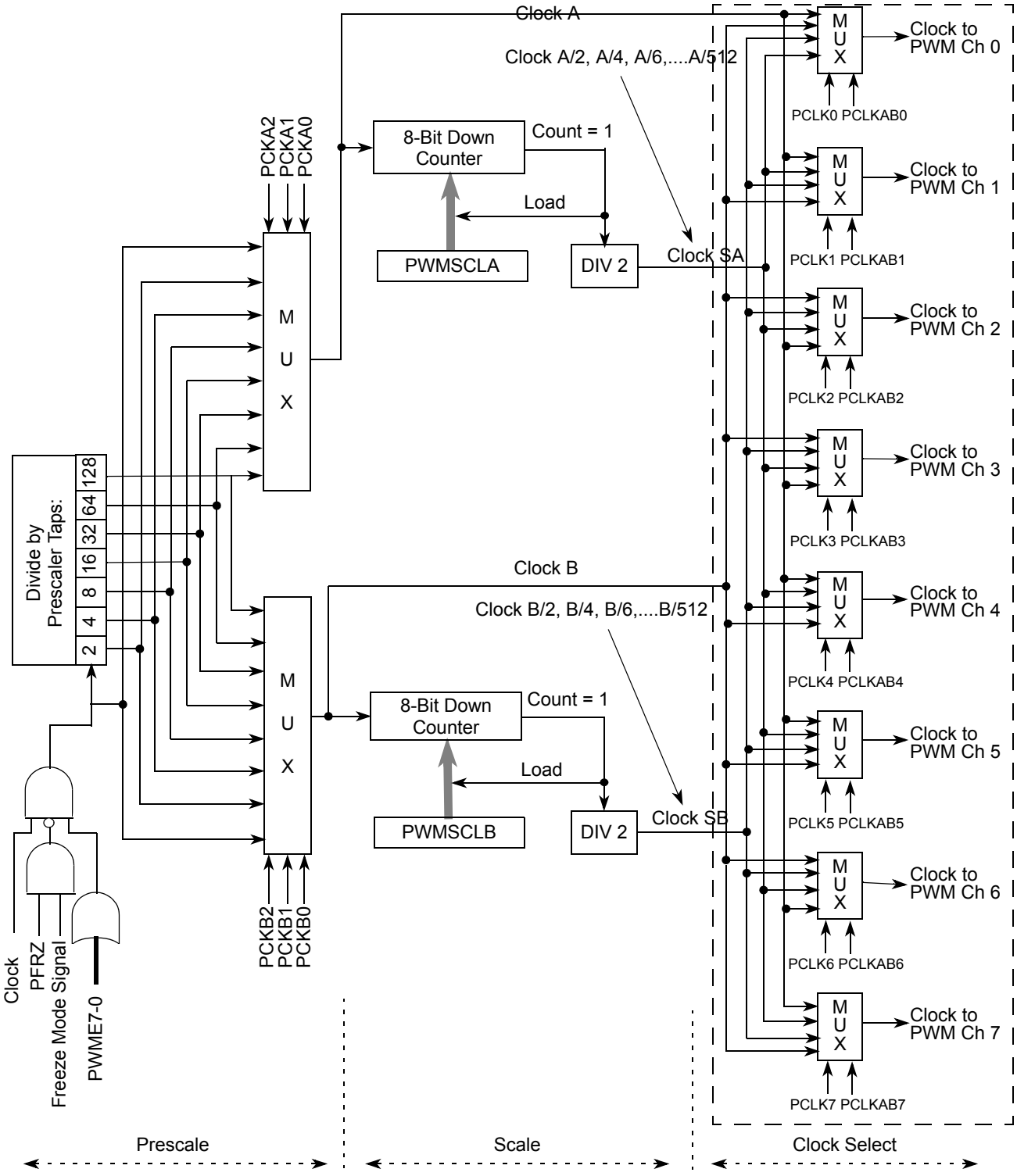

Figure 22-15. PWM Clock Select Block Diagram

Appendix A
MCU Electrical Specifications

A.1 General

This section contains the most accurate electrical information available at the time of publication.

A.1.1 Parameter Classification

The electrical parameters shown in the appendices are guaranteed by various methods.

The parameter classification is documented in the PPAP.

The parameter classification columns are for NXP internal use only.

A.2 General Purpose I/O Characteristics

Table A-12. 5V I/O Characteristics

Conditions are 4.5 V < V_{DDX}< 5.5 V , -40°C < T_j < 175°C for all GPIO pins (defined in A.1.2.1/A-876) unless otherwise noted.							
Num		**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		Input high voltage, 3.13 V < V_{DDX}< 5.5 V	V_{IH}	0.65*V_{DDX}	—	—	V
2		Input high voltage	V_{IH}	—	—	V_{DDX}+0.3	V
3		Input low voltage, 3.13 V < V_{DDX}< 5.5 V	V_{IL}	—	—	0.35*V_{DDX}	V
4		Input low voltage	V_{IL}	V_{SSX}–0.3	—	—	V
5		Input hysteresis	V_{HYS}	—	250	—	mV
6a		Input leakage current. All cases except 6b,6c,6d. (1) V_{in} = V_{DDX} or V_{SSX}	I_{in}	-1	—	1	μA
6b		Input leakage current PAD[15:0], ZVMC256 (1) V_{in} = V_{DDX} or V_{SSX} T_j = 125°C	I_{in}	-0.3	—	0.3	μA
6c		Input leakage current. PAD8 (all devices except ZVMC256), PP0 (1) V_{in} = V_{DDX} or V_{SSX}	I_{in}	-2.5	—	2.5	μA
6d		Input leakage current. PAD8, PP0 (1) -40°C < T_j < 150°C, V_{in} = V_{DDX} or V_{SSX}	I_{in}	-1	—	1	μA
7		Output high voltage (All GPIO except EVDD1) I_{OH} = –4 mA	V_{OH}	V_{DDX} – 0.8	—	—	V
8a		Output high voltage (EVDD1), V_{DDX} > 4.85V Partial Drive I_{OH} = –2 mA Full Drive IOH = –20mA	V_{OH}	V_{DDX} – 0.8	—	—	V
8b		Output high voltage (EVDD1), V_{DDX} > 4.85V Full Drive IOH = –10mA	V_{OH}	V_{DDX} – 0.1	—	—	V
9		Output low voltage (All GPIO except EVDD1) I_{OL} = +4mA	V_{OL}	—	—	0.8	V
10		Output low voltage (EVDD1) Partial drive I_{OL} = +2mA or Full drive I_{OL} = +20mA	V_{OL}	—	—	0.8	V
11		Maximum allowed continuous current on EVDD1	I_{EVDD1}	-20	—	10	mA
12		Over-current Detect Threshold EVDD1	I_{OCD}	-80	—	-40	mA
13		Internal pull up current (All GPIO except RESET) V_{IH} min > input voltage > V_{IL} max	I_{PUL}	-10	—	-130	μA
14		Internal pull up resistance (RESET pin)	R_{PUL}	2.5	5	10	KΩ
15		Internal pull down current, V_{IH} min > V_{in} > V_{IL} max	I_{PDH}	10	—	130	μA
16		Input capacitance	C_{in}	—	7	—	pF
17a		Injection current(2) Single pin limit (all GPIO pins) Total device limit, sum of all injected currents	I_{ICS} I_{ICP}	–2.5 –25	—	2.5 25	mA
17b		Injection current single pin (HG,HS,LG,LS pins)(3)	I_{ICS}	–2.5	—	2.5	mA

1. Pins in high impedance input mode. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°°C to 12°°C in the temperature range from 50°C to 125°C.

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x013C	DBGCDM0 (2)	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x013D	DBGCDM1 2	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x013E	DBGCDM2 2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x013F	DBGCDM3 2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								
0x0147	DBGDAL	R	DBGDA[7:0]							
		W								
0x0148-0x017F	Reserved	R	0	0	0	0	0	0	0	0
		W								

1. Only included on S12ZVM256

2. Not included on S12ZVM32 or S12ZVM16 devices

M.5 0x0200-0x02FF PIM (See footnotes for part specific information)

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0200	MODRR0	R	0	0	SPI0SSRR	SPI0RR	SCI1RR	S0L0RR2-0(1)		
		W								
0x0201	MODRR1	R	M0C0RR2-0(2)			PWMPRR1-0(3)		PWM54RR	PWM32RR	PWM10RR
		W								
0x0202	MODRR2	R	T0C2RR1-0(4)		T0C1RR4	T1IC0RR2	T0IC3RR1-0		T0IC1RR	T0IC1RR04
		W								
0x0203–0x0207	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0208	ECLKCTL	R	NECLK	0	0	0	0	0	0	0
		W								
0x0209	IRQCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								
0x020A	PIMMISC	R	0	0	0	0	0	0	OCPE1	0
		W								
0x020B–0x020C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x020D	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x020E	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x020F	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0210–0x025F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0260	PTE	R	0	0	0	0	0	0	PTE1	PTE0
		W								

M.6 0x0380-0x039F FTMRZ128K512 (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0396	FCCOB5HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0397	FCCOB5LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								

M.7 0x03C0-0x03CF SRAM_ECC_32D7P

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x03C0	ECCSTAT	R	0	0	0	0	0	0	0	RDY
		W								
0x03C1	ECCIE	R	0	0	0	0	0	0	0	SBEEIE
		W								
0x03C2	ECCIF	R	0	0	0	0	0	0	0	SBEEIF
		W								
0x03C3 - 0x03C6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C7	ECCDPTRH	R	DPTR[23:16]							
		W								
0x03C8	ECCDPTRM	R	DPTR[15:8]							
		W								
0x03C9	ECCDPTRL	R	DPTR[7:1]							0
		W								
0x03CA - 0x03CB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03CC	ECCDDH	R	DDATA[15:8]							
		W								
0x03CD	ECCDDL	R	DDATA[7:0]							
		W								
0x03CE	ECCDE	R	0	0	DECC[5:0]					
		W								
0x03CF	ECCDCMD	R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
		W								