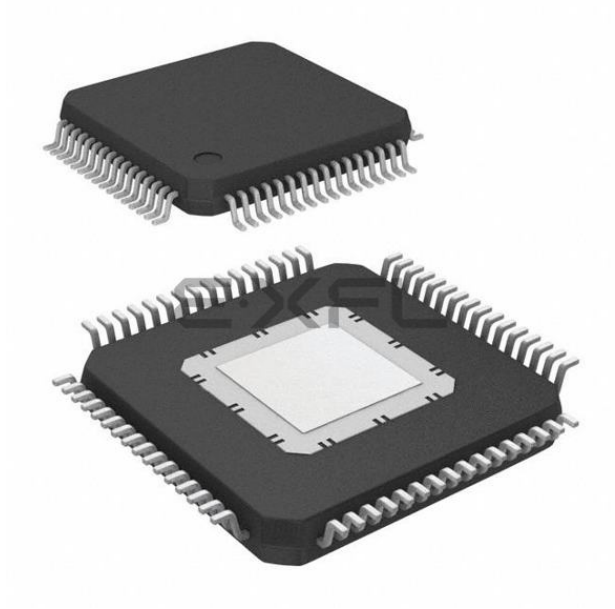

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml64f2mkh

8.3.2.23 S12CPMU_UHV_V10_V6 IRC1M Trim Registers (CPMUIRCTRIMH / CPMUIRCTRIML)

Module Base + 0x0018

	15	14	13	12	11	10	9	8
R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
W								
Reset	F	F	F	F	F	0	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Figure 8-31. S12CPMU_UHV_V10_V6 IRC1M Trim High Register (CPMUIRCTRIMH)

Module Base + 0x0019

	7	6	5	4	3	2	1	0
R	IRCTRIM[7:0]							
W								
Reset	F	F	F	F	F	F	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Figure 8-32. S12CPMU_UHV_V10_V6 IRC1M Trim Low Register (CPMUIRCTRIML)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register). Else write has no effect

NOTE

Writes to these registers while PLLSEL=1 clears the LOCK and UPOSC status bits.

Table 8-27. CPMUIRCTRIMH/L Field Descriptions

Field	Description
15-11 TCTRIM[4:0]	IRC1M temperature coefficient Trim Bits Trim bits for the Temperature Coefficient (TC) of the IRC1M frequency. Table 8-28 shows the influence of the bits TCTRIM[4:0] on the relationship between frequency and temperature. Figure 8-34 shows an approximate TC variation, relative to the nominal TC of the IRC1M (i.e. for TCTRIM[4:0]=0x00000 or 0x10000).
9-0 IRCTRIM[9:0]	**IRC1M Frequency Trim Bits** — Trim bits for Internal Reference Clock After System Reset the factory programmed trim value is automatically loaded into these registers, resulting in a Internal Reference Frequency f_{IRC1M_TRIM}.See device electrical characteristics for value of f_{IRC1M_TRIM}. The frequency trimming consists of two different trimming methods: A rough trimming controlled by bits IRCTRIM[9:6] can be done with frequency leaps of about 6% in average. A fine trimming controlled by bits IRCTRIM[5:0] can be done with frequency leaps of about 0.3% (this trimming determines the precision of the frequency setting of 0.15%, i.e. 0.3% is the distance between two trimming values). Figure 8-33 shows the relationship between the trim bits and the resulting IRC1M frequency.

Several examples of PLL divider settings are shown in Table 8-34. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 8-34. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz
off	$00	1MHz	00	$18	50MHz	01	$00	50MHz	25MHz
4MHz	$00	4MHz	01	$05	48MHz	00	$00	48MHz	24MHz

The phase detector inside the PLL compares the feedback clock (FBCLK = VCOCLK/(SYNDIV+1)) with the reference clock (REFCLK = (IRC1M or OSCCLK)/(REFDIV+1)). Correction pulses are generated based on the phase difference between the two signals. The loop filter alters the DC voltage on the internal filter capacitor, based on the width and direction of the correction pulse which leads to a higher or lower VCO frequency.

The user must select the range of the REFCLK frequency (REFFRQ[1:0] bits) and the range of the VCOCLK frequency (VCOFRQ[1:0] bits) to ensure that the correct PLL loop bandwidth is set.

The lock detector compares the frequencies of the FBCLK and the REFCLK. Therefore the speed of the lock detector is directly proportional to the reference clock frequency. The circuit determines the lock condition based on this comparison. So e.g. a failure in the reference clock will cause the PLL not to lock.

If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and for instance check the LOCK bit. If interrupt requests are disabled, software can poll the LOCK bit continuously (during PLL start-up) or at periodic intervals. In either case, only when the LOCK bit is set, the VCOCLK will have stabilized to the programmed frequency.

- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within the tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of the tolerance, Δ_{unl}.

Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.In case of loss of reference clock (e.g. IRCCLK) the PLL will not lock or if already locked, then it will unlock. The frequency of the VCOCLK will be very low and will depend on the value of the VCOFRQ[1:0] bits.

8.5.4 PLL Clock Monitor Reset

In case of loss of PLL clock oscillation or the PLL clock frequency is below the failure assert frequency f_{PMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V10_V6 generates a PLL Clock Monitor Reset. In Full Stop Mode the PLL and the PLL clock monitor are disabled.

8.5.5 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus COP reset is generated.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit.

Depending on the COP configuration there might be a significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

Table 8-36 gives an overview of the COP condition (run, static) in Stop Mode depending on legal configuration and status bit settings:

Table 8-36. COP condition (run, static) in Stop Mode

COPOSCSEL1	CSAD	PSTP	PCE	COPOSCSEL0	OSCE	UPOSC	COP counter behavior in Stop Mode (clock source)
1	0	x	x	x	x	x	Run (ACLK)
1	1	x	x	x	x	x	Static (ACLK)
0	x	1	1	1	1	1	Run (OSCCLK)
0	x	1	1	0	0	x	Static (IRCCLK)
0	x	1	1	0	1	x	Static (IRCCLK)
0	x	1	0	0	x	x	Static (IRCCLK)
0	x	1	0	1	1	1	Static (OSCCLK)
0	x	0	1	1	1	1	Static (OSCCLK)
0	x	0	1	0	1	x	Static (IRCCLK)
0	x	0	1	0	0	0	Static (IRCCLK)
0	x	0	0	1	1	1	Satic (OSCCLK)
0	x	0	0	0	1	1	Static (IRCCLK)
0	x	0	0	0	1	0	Static (IRCCLK)
0	x	0	0	0	0	0	Static (IRCCLK)

9.4 Signal Description

This section lists all inputs to the ADC12B_LBA block.

9.4.1 Detailed Signal Descriptions

9.4.1.1 AN*x* (*x* = *n*,..., 2, 1, 0)

This pin serves as the analog input Channel *x*. The maximum input channel number is *n*. Please refer to the device reference manual for the maximum number of input channels.

9.4.1.2 VRH_0, VRH_1, VRH_2, VRL_0, VRL_1

VRH_0/1/2 are the high reference voltages, VRL0/1 are the low reference voltages for a ADC conversion selectable on a conversion command basis. Please refer to the device overview information for availability and connectivity of these pins.

VRH_2 is only available on ADC12B_LBA V3.

VRL_1 is only available on ADC12B_LBA V1 and V2.

See also Table 9-2.

9.4.1.3 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B_LBA block.

Table 9-22. Conversion Interrupt Flag Select

CON_IF[15:1]	INTFLG_SEL[3]	INTFLG_SEL[2]	INTFLG_SEL[1]	INTFLG_SEL[0]	Comment
0x0000	0	0	0	0	No flag set
0x0001	0	0	0	1	Only one flag can be set (one hot coding)
0x0002	0	0	1	0	
0x0004	0	0	1	1	
0x0008	0	1	0	0	
0x0010	0	1	0	1	
....	...	...	...	...	
0x0800	1	1	0	0	
0x1000	1	1	0	1	
0x2000	1	1	1	0	
0x4000	1	1	1	1	

9.5.2.22 ADC Result Base Pointer Register (ADCRBP)

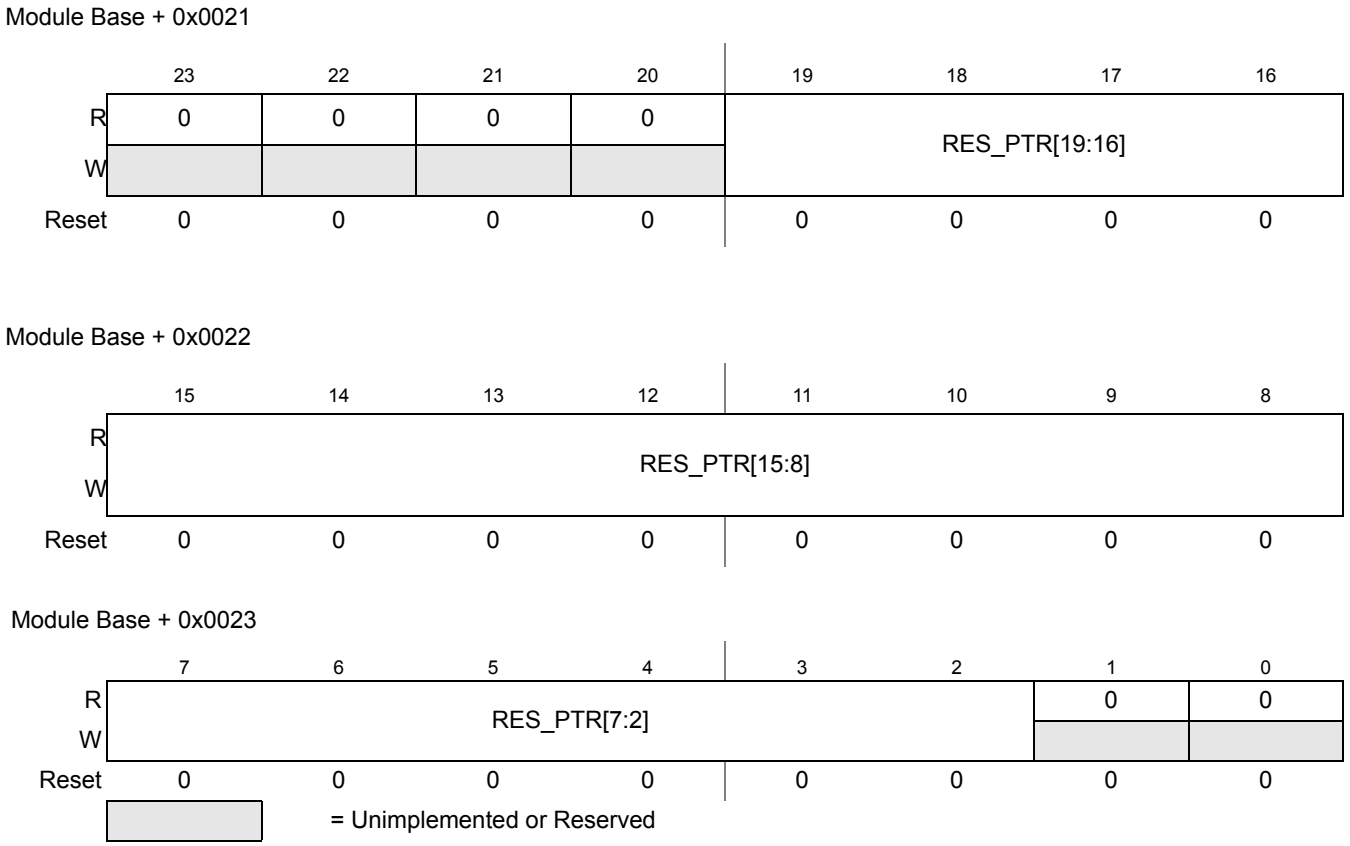


Figure 9-25. ADC Result Base Pointer Registers (ADCRBP_0, ADCRBP_1, ADCRBP_2))

Read: Anytime

Write: Bits RES_PTR[19:2] writeable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-30. ADCRBP Field Descriptions

Field	Description
19-2 RES_PTR[19:2]	**ADC Result Base Pointer Address** — These bits define the base address of the list areas inside the system RAM of the memory map to which conversion results will be stored to at the end of a conversion. These bits can only be written if bit ADC_EN is clear. See also Section 9.6.3.2.3, “Introduction of the two Result Value Lists (RVLs).

Table 11-12. Timer Clock Selection

PR2	PR1	PR0	Timer Clock
0	0	0	Bus Clock / 1
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

NOTE

The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

11.3.2.10 Main Timer Interrupt Flag 1 (TFLG1)

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	C3F	C2F	C1F	C0F
Reset	0	0	0	0	0	0	0	0

Figure 11-16. Main Timer Interrupt Flag 1 (TFLG1)

Read: Anytime

Write: Used in the clearing mechanism (set bits cause corresponding bits to be cleared). Writing a zero will not affect current status of the bit.

Table 11-13. TRLG1 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 C[3:0]F	**Input Capture/Output Compare Channel “x” Flag** — These flags are set when an input capture or output compare event occurs. Clearing requires writing a one to the corresponding flag bit while TEN is set to one. **Note:** When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel (0x0010–0x001F) will cause the corresponding channel flag CxF to be cleared.

12.3.2.13 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
1:0 OCPD[1:0]	Output Compare Pin Disconnect Bits 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

12.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 12-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

NOTE

The CANRIER register is held in the reset state when the initialization mode is active (INITRQ=1 and INITAK=1). This register is writable when not in initialization mode (INITRQ=0 and INITAK=0).

The RSTATE[1:0], TSTATE[1:0] bits are not affected by initialization mode.

Table 13-11. CANRIER Register Field Descriptions

Field	Description
7 WUPIE[1]	**Wake-Up Interrupt Enable** 0 No interrupt request is generated from this event. 1 A wake-up event causes a Wake-Up interrupt request.
6 CSCIE	**CAN Status Change Interrupt Enable** 0 No interrupt request is generated from this event. 1 A CAN Status Change event causes an error interrupt request.
5-4 RSTATE[1:0]	**Receiver Status Change Enable** — These RSTAT enable bits control the sensitivity level in which receiver state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level the RSTAT flags continue to indicate the actual receiver state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by receiver state changes. 01 Generate CSCIF interrupt only if the receiver enters or leaves “bus-off” state. Discard other receiver state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the receiver enters or leaves “RxErr” or “bus-off”[2] state. Discard other receiver state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
3-2 TSTATE[1:0]	**Transmitter Status Change Enable** — These TSTAT enable bits control the sensitivity level in which transmitter state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level, the TSTAT flags continue to indicate the actual transmitter state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by transmitter state changes. 01 Generate CSCIF interrupt only if the transmitter enters or leaves “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the transmitter enters or leaves “TxErr” or “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
1 OVRIE	**Overrun Interrupt Enable** 0 No interrupt request is generated from this event. 1 An overrun event causes an error interrupt request.
0 RXFIE	**Receiver Full Interrupt Enable** 0 No interrupt request is generated from this event. 1 A receive buffer full (successful message reception) event causes a receiver interrupt request.

1. WUPIE and WUPE (see Section 13.3.2.1, “MSCAN Control Register 0 (CANCTL0)”) must both be enabled if the recovery mechanism from stop or wait is required.

2. Bus-off state is only defined for transmitters by the CAN standard (see Bosch CAN 2.0A/B protocol specification). Because the only possible state change for the transmitter from bus-off to TxOK also forces the receiver to skip its current state to RxOK, the coding of the RXSTAT[1:0] flags define an additional bus-off state for the receiver (see Section 13.3.2.5, “MSCAN Receiver Flag Register (CANRFLG)”).

Table 18-18. Charge Pump Clock Divider Factors k = f_{BUS} / f_{CP}

GCPCD[3:0]	f_{CP}
0000	f_{BUS} / 16
0001	f_{BUS} / 24
0010	f_{BUS} / 32
0011	f_{BUS} / 48
0100	f_{BUS} / 64
0101	f_{BUS} / 96
0110	f_{BUS} / 100
0111	f_{BUS} / 128
1000	f_{BUS} / 192
1001	f_{BUS} / 200
1010	f_{BUS} / 256
1011	f_{BUS} / 384
1100	f_{BUS} / 400
1101	f_{BUS} / 512
1110	f_{BUS} / 768
1111	f_{BUS} / 800

20.4.8.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the SFDIF flag in combination with the SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 20.3.2.5, “Flash Configuration Register (FCNFG)”, Section 20.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 20.3.2.7, “Flash Status Register (FSTAT)”, and Section 20.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 20-31.

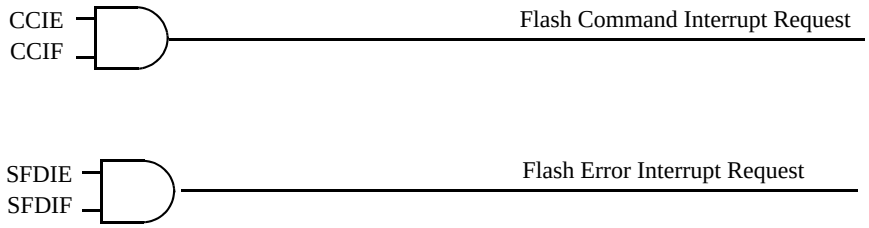


Figure 20-31. Flash Module Interrupts Implementation

20.4.9 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 20.4.8, “Interrupts”).

20.4.10 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

20.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 20-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0xFF_FE0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

Table 21-6. CPSR Register Field Descriptions

Field	Description
4 CPCLVL	CANL Voltage Failure Low Status Bit This bit reflects the CANL voltage failure low monitor status. 0 Condition $V_{CANL} > V_{L0}$ 1 Condition $V_{CANL} \leq V_{L0}$
3 CPDT	CPTXD-Dominant Timeout Status Bit This bit is set to 1, if CPTXD is dominant for longer than $t_{CPTXDDT}$. It signals a timeout event and remains set until CPTXD returns to recessive level for longer than 1 µs. 0 No CPTXD-timeout occurred or CPTXD has ceased to be dominant after timeout 1 CPTXD-dominant timeout occurred and CPTXD is still dominant

21.5.2.5 Standby Mode

Standby is a reduced current consumption mode and is entered during RPM following a stop mode request. The transceiver and bus error diagnostics are disabled. The CPTXD-dominant timeout counter is stopped. CANH and CANL lines are pulled to VSSC via high-ohmic input resistors of the receiver. The SPLIT pin is set to high-impedance. The internal mid-point reference is set to 0V. All voltage failure and over-current monitors are disabled.

Standby is left as soon as the device returns from RPM.

21.5.3 Configurable Wake-Up

If the wake-up function is enabled, the CAN Physical Layer provides an asynchronous path through CPRXD to the MSCAN to support wake-up from stop mode. The CPRXD signal is switched from precision receiver to the low-power wake-up receiver as long as the device resides in RPM.

In order to avoid false wake-up after entering stop mode, a pulse filter can be enabled and configured to mask the first or first two wake-up events from the MSCAN input. The CPRXD output is held at recessive level until the selected number of wake-up events have been detected as shown in Figure 21-11.

A valid wakeup-event is defined as a dominant level with a length of min. t_{CPWUP} followed by a recessive level of length t_{CPWUP}.

The wake-up filter specification t_{WUP} of the MSCAN applies to wake-up the MSCAN from sleep mode. Refer to MSCAN chapter.After wake-up the CAN Physical Layer automatically returns to the mode where stop mode was requested.

Refer to 21.6.2, “Wake-up Mechanism” for setup information.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

Wait: The prescaler keeps on running, unless PSWAI in PWMCTL is set to 1.

Freeze: The prescaler keeps on running, unless PFRZ in PWMCTL is set to 1.

22.1.3 Block Diagram

Figure 22-1 shows the block diagram for the 8-bit up to 8-channel scalable PWM block.

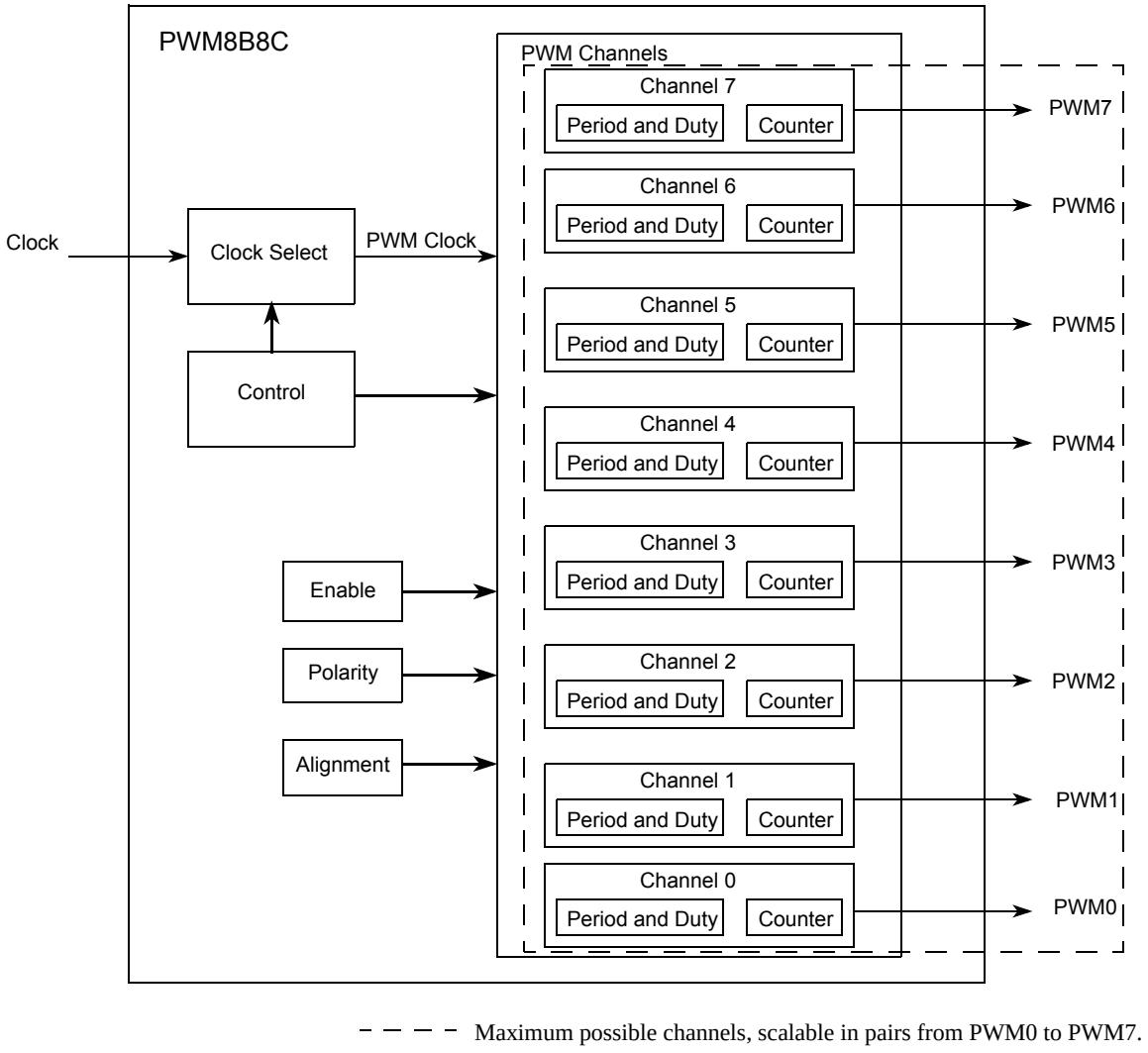


Figure 22-1. Scalable PWM Block Diagram

22.2 External Signal Description

The scalable PWM module has a selected number of external pins. Refer to device specification for exact number.

NOTE

Please refer to the temperature rating of the device with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to Section A.1.8, “Power Dissipation and Thermal Characteristics”.

Table A-6. Operating Conditions

Num	Rating	Symbol	Min	Typ	Max	Unit
1	Voltage regulator and LINPHY supply voltage(1)	V_{SUP}	3.5	12	40	V
2	Voltage difference V_{DDX} to V_{DDA}	ΔVDDX	–0.1	—	0.1	V
3	Voltage difference V_{SSX} to V_{SSA}	ΔVSSX	–0.1	—	0.1	V
	Digital logic supply voltage	V_{DD}	1.72	1.8	1.98	V
4	Oscillator	f_{osc}	4	—	20	MHz
5	Bus frequency(2) -40°C < T_j < 150°C 150°C < T_j < 175°C (Temp option W only)	f_{bus}	(4)	— —	50 40	MHz
6	Bus frequency without flash wait states -40°C < T_j < 150°C 150°C < T_j < 175°C (Temp option W only)	f_{WSTAT}	— —	— —	25 20	MHz
7a	Operating junction temperature range Operating ambient temperature range(3) (option V)	T_J T_A	–40 –40	— —	125 105	°C
7b	Operating junction temperature range Operating ambient temperature range(3) (option M)	T_J T_A	–40 –40	— —	150 125	°C
7c	Operating junction temperature range Operating ambient temperature range(3) (option W)	T_J T_A	–40 –40	— —	175 150	°C

1. Normal operating range is 5.5 V - 18 V. Continuous operation at 40 V is not allowed. Only Transient Conditions (Load Dump) single pulse t_{max}<400 ms. Operation down to 3.5V is guaranteed without reset, however some electrical parameters are specified only in the range above 4.5 V. Operation in the range 20V<VSUP<26.5V is limited to 1 hour over lifetime of the device. In this range the device continues to function but electrical parameters are degraded.

2. The flash program and erase operations must configure f_{NVMOP} as specified in the NVM electrical section.

3. Please refer to Section A.1.8, “Power Dissipation and Thermal Characteristics” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

4. Refer to f_{ATDCLK} for minimum ADC operating frequency. This is derived from the bus clock.

NOTE

Operation is guaranteed when powering down until low voltage reset assertion.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00237D
		PAGE: 2139
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

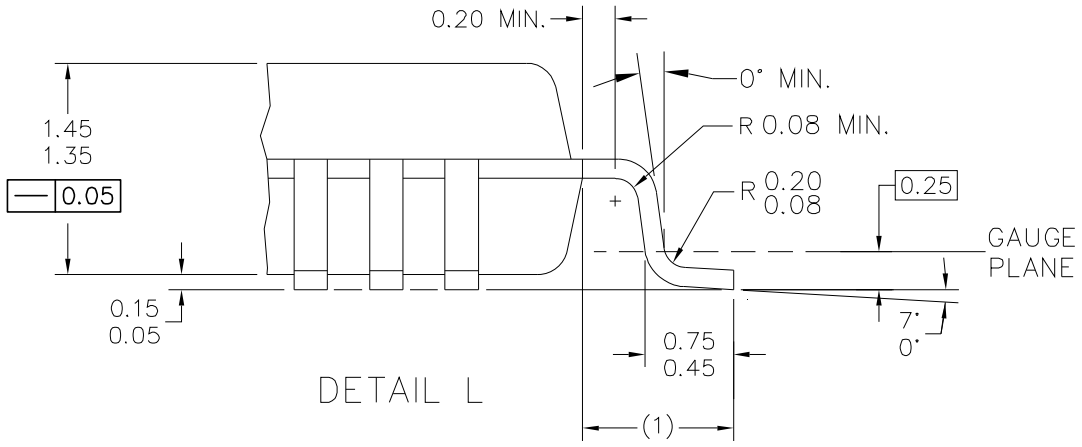
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 4.9 X 4.9 EXPOSED PAD	CASE NUMBER: 2139–01	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: IN AGILE	SHEET: 3 OF 4

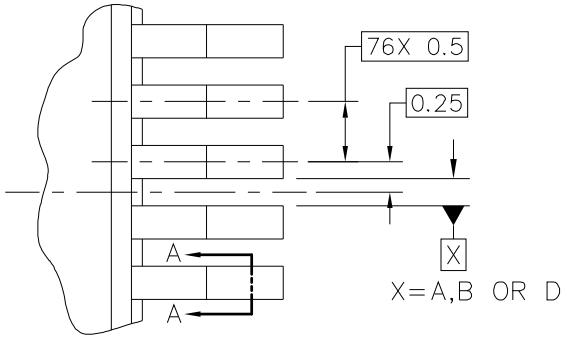
freescale

MECHANICAL OUTLINE

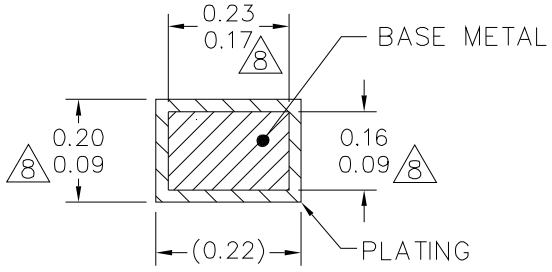
DO NOT SCALE THIS DRAWING



DETAIL L



DETAIL K



SECTION A–A
100 PLACES
ROTATED 90° CLOCKWISE

TITLE: LQFP, 12 X 12 X 1.4 PKG, 0.5 PITCH, 80LD, 5.6 X 5.6 EXPOSED PAD	DOCUMENT NO: 98ASA00505D	REV: X2
	STANDARD: NON–JEDEC	
	SHEET:	2

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02D6	PIES	R	0	0	PIES5[5]	PIES4[5]	PIES3	PIES2	PIES1	PIES0
		W								
0x02D7	PIFS	R	0	0	PIFS5[5]	PIFS4[5]	PIFS3	PIFS2	PIFS1	PIFS0
		W								
0x02D8–0x02DE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02DF	WOMS	R	0	0	WOMS5[5]	WOMS4[5]	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x02E0–0x02EF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F0	PTP	R	0	0	0	0	0	PTP2[5]	PTP1	PTP0
		W								
0x02F1	PTIP	R	0	0	0	0	0	PTIP2[5]	PTIP1	PTIP0
		W								
0x02F2	DDRP	R	0	0	0	0	0	DDRP2[5]	DDRP1	DDRP0
		W								
0x02F3	PERP	R	0	0	0	0	0	PERP2[5]	PERP1	PERP0
		W								
0x02F4	PPSP	R	0	0	0	0	0	PPSP2[5]	PPSP1	PPSP0
		W								
0x02F5	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F6	PIEP	R	OCIE1	0	0	0	0	PIEP2[5]	PIEP1	PIEP0
		W								
0x02F7	PIFP	R	OCIF1	0	0	0	0	PIFP2[5]	PIFP1	PIFP0
		W								

M.9 0x0480-0x04AF PWM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x049B	PWMPER7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049C	PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049D	PWMDTY1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049E	PWMDTY2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049F	PWMDTY32	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A0	PWMDTY42	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A1	PWMDTY52	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A2	PWMDTY62	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A3	PWMDTY72	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A4 - 0x04AF	RESERVED	R W	0	0	0	0	0	0	0	0

M.10 0x0500-x053F PMF15B6C

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0500	PMFCFG0	R W	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
0x0501	PMFCFG1	R W	0	ENCE	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
0x0502	PMFCFG2	R W	REV1	REV0	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
0x0503	PMFCFG3	R W	PMFWAI	PMFFRZ	0	VLMODE		PINVC	PINVB	PINVA
0x0504	PMFFEN	R W	0	FEN5	0	FEN4	FEN3	FEN2	FEN1	FEN0
0x0505	PMFFMOD	R W	0	FMOD5	0	FMOD4	FMOD3	FMOD2	FMOD1	FMOD0