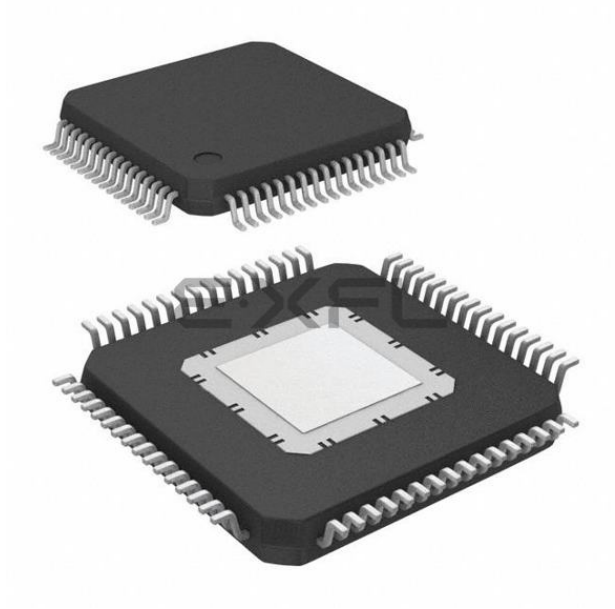

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml64f2vkh

1.8.1.2 ADC Internal Channels

The ADC0 and ADC1 internal channel mapping is shown in Table 1-10 and Table 1-11 respectively.

The GDU current sense amplifier outputs are mapped to pins with ADC input functionality. Thus configuring the ADC to convert these pin channels automatically converts the current sense outputs.

The ADC internal temperature sensors must be calibrated by the user. No electrical parameters are specified for these sensors. The VREG temperature sensor electrical parameters are given in the appendices.

Table 1-10. Usage of ADC0 Internal Channels

ADCCMD_1 CH_SEL[5:0]						ADC Channel	Usage
0	0	1	0	0	0	Internal_0	ADC0 temperature sensor
0	0	1	0	0	1	Internal_1	VREG temperature sensor or bandgap (V_{BG})[1]
0	0	1	0	1	0	Internal_2	GDU phase multiplexer voltage
0	0	1	0	1	1	Internal_3	GDU DC link voltage monitor
0	0	1	1	0	0	Internal_4	BATS VSUP sense voltage
0	0	1	1	0	1	Internal_5	HVI[0][2]
0	0	1	1	1	0	Internal_6	Reserved
0	0	1	1	1	1	Internal_7	Reserved

1. Selectable in CPMU

2. ZVMC256 only. On other devices this channel is reserved.

Table 1-11. Usage of ADC1 Internal Channels

ADCCMD_1 CH_SEL[5:0]						ADC Channel	Usage
0	0	1	0	0	0	Internal_0	ADC1 temperature sensor
0	0	1	0	0	1	Internal_1	VREG temperature sensor or bandgap (V_{BG})[1]
0	0	1	0	1	0	Internal_2	GDU phase multiplexer voltage
0	0	1	0	1	1	Internal_3	GDU DC link voltage monitor
0	0	1	1	0	0	Internal_4	Reserved
0	0	1	1	0	1	Internal_5	Reserved
0	0	1	1	1	0	Internal_6	Reserved
0	0	1	1	1	1	Internal_7	Reserved

1. Selectable in CPMU

1.8.2 Motor Control Loop Signals

The motor control loop signals are described in 1.13.3.1 Motor Control Loop Overview

Table 6-15. DBGCNT Field Descriptions

Field	Description
6–0 CNT[6:0]	**Count Value** — The CNT bits [6:0] indicate the number of valid data lines stored in the trace buffer. Table 6-16 shows the correlation between the CNT bits and the number of valid data lines in the trace buffer. When the CNT rolls over to zero, the TBF bit in DBGSR is set. Thereafter incrementing of CNT continues if configured for end-alignment or mid-alignment. The DBGCNT register is cleared when ARM in DBGC1 is written to a one. The DBGCNT register is cleared by power-on-reset initialization but is not cleared by other system resets. If a reset occurs during a debug session, the DBGCNT register still indicates after the reset, the number of valid trace buffer entries stored before the reset occurred. The DBGCNT register is not decremented when reading from the trace buffer.

Table 6-16. CNT Decoding Table

TBF (DBGSR)	CNT[6:0]	Description
0	0000000	No data valid
0	0000001	32 bits of one line valid
0	0000010 0000100 0000110 .. 1111100	1 line valid 2 lines valid 3 lines valid .. 62 lines valid
0	1111110	63 lines valid
1	0000000	64 lines valid; if using Begin trigger alignment, ARM bit is cleared and the tracing session ends.
1	0000010 .. 1111110	64 lines valid, oldest data has been overwritten by most recent data

6.3.2.7 Debug State Control Register 1 (DBGSCR1)

Address: 0x0107

	7	6	5	4	3	2	1	0
R W	C3SC1	C3SC0	C2SC1	C2SC0	C1SC1	C1SC0	C0SC1	C0SC0
Reset	0	0	0	0	0	0	0	0

Figure 6-9. Debug State Control Register 1 (DBGSCR1)

Read: Anytime.

Write: If DBG is not armed and PTACT is clear.

The state control register 1 selects the targeted next state whilst in State1. The matches refer to the outputs of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.12”. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

- When a reset occurs the debugger pulls BKGD low until the reset ends, forcing SSC mode entry.
- Then the debugger reads the reset flags to determine the cause of reset.
- If required, the debugger can read the trace buffer to see what happened just before reset. Since the trace buffer and DBGCNT register are not affected by resets other than POR.
- The debugger configures and arms the DBG to start tracing on returning to application code.
- The debugger then sets the PC according to the reset flags.
- Then the debugger returns to user code with GO or STEP1.

6.5.3 Breakpoints from other S12Z sources

The DBG is neither affected by CPU BGND instructions, nor by BDC BACKGROUND commands.

6.5.4 Code Profiling

The code profiling data output pin PDO is mapped to a device pin that can also be used as GPIO in an application. If profiling is required and all pins are required in the application, it is recommended to use the device pin for a simple output function in the application, without feedback to the chip. In this way the application can still be profiled, since the pin has no effect on code flow.

The PDO provides a simple bit stream that must be strobed at both edges of the profiling clock when profiling. The external development tool activates profiling by setting the DBG ARM bit, with PROFILE and PDOE already set. Thereafter the first bit of the profiling bit stream is valid at the first rising edge of the profiling clock. No start bit is provided. The external development tool must detect this first rising edge after arming the DBG. To detect the end of profiling, the DBG ARM bit can be monitored using the BDC.

8.3.2.19 Autonomous Clock Trimming Register (CPMUACLKTR)

The CPMUACLKTR register configures the trimming of the Autonomous Clock (ACLK - trimmable internal RC-Oscillator) which can be selected as clock source for some CPMU features.

Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
W								
Reset	F	F	F	F	F	F	0	0

After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 8-26. Autonomous Clock Trimming Register (CPMUACLKTR)

Read: Anytime

Write: Anytime

Table 8-20. CPMUACLKTR Field Descriptions

Field	Description
7–2 ACLKTR[5:0]	**Autonomous Clock Period Trimming Bits** — See Table 8-21 for trimming effects. The ACLKTR[5:0] value represents a signed number influencing the ACLK period time.

Table 8-21. Trimming Effect of ACLKTR[5:0]

ACLKTR[5:0]	Decimal	ACLK frequency
100000	-32	lowest
100001	-31	increasing
....		
111111	-1	
000000	0	mid
000001	+1	increasing
....		
011110	+30	
011111	+31	highest

8.3.2.22 High Temperature Trimming Register (CPMUHTTR)

The CPMUHTTR register configures the trimming of the S12CPMU_UHV_V10_V6 temperature sense.

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	F	F	F	F

After de-assert of System Reset a trim value is automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 8-30. High Temperature Trimming Register (CPMUHTTR)

Read: Anytime

Write: Anytime

Table 8-25. CPMUHTTR Field Descriptions

Field	Description
7 HTOE	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled. 0 The temperature sense offset is disabled. HTTR[3:0] bits don't care. 1 The temperature sense offset is enabled. HTTR[3:0] select the temperature offset.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 8-26 for trimming effects.

Table 8-26. Trimming Effect of HTTR

HTTR[3:0]	Temperature sensor voltage V_{HT}	Interrupt threshold temperatures T_{HTIA} and T_{HTID}
0000	lowest	highest
0001	increasing	decreasing
....		
1110		
1111	highest	lowest

8.4.2 Startup from Reset

An example for startup of the clock system from Reset is given in Figure 8-41.

Figure 8-41. Startup of clock system after Reset

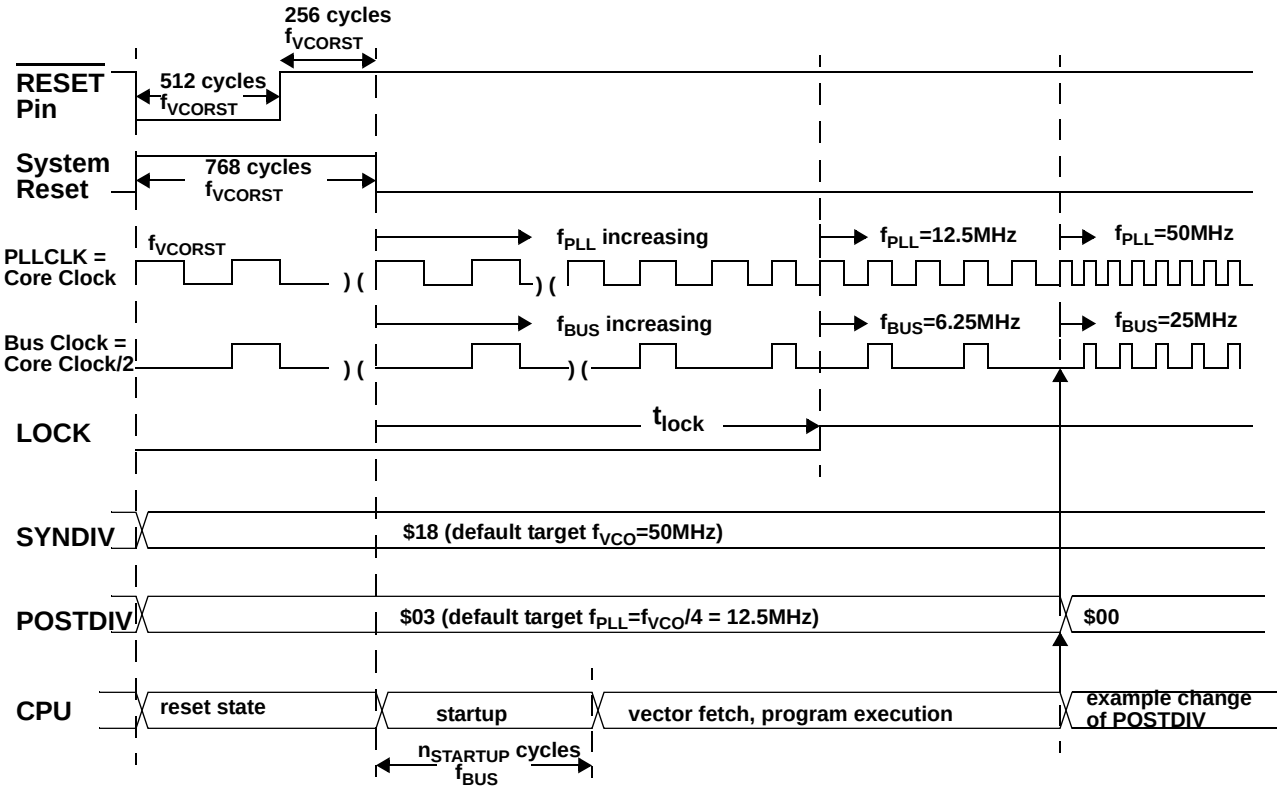

Table 9-10. ADCFLWCTL Field Descriptions (continued)

Field	Description
5 RSTA	**Restart Event (Restart from Top of Command Sequence List)** — This bit indicates that a Restart Event is executed. The ADC loads the conversion command from top of the active Sequence Command List when no conversion or conversion sequence is ongoing. This bit is cleared when the first conversion command of the sequence from top of active Sequence Command List has been loaded into the ADCCMD register. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. Data Bus Control: This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. Writing a one to this bit does not clear it but causes an overrun if the bit has already been set. See also Section 9.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. Internal Interface Control: This bit can be controlled via the internal interface Signal "Restart" if access control is configured accordingly via ACC_CFG[1:0]. After being set an additional request via internal interface Signal "Restart" causes an overrun. See conversion flow control in case of overrun situations for more details. General: In conversion flow control mode "Trigger Mode" when bit RSTA gets set bit TRIG is set simultaneously if one of the following has been executed: - "End Of List" command type has been executed or is about to be executed - Sequence Abort Event 0 Continue with commands from active Sequence Command List. 1 Restart from top of active Sequence Command List.
4 LDOK	**Load OK for alternative Command Sequence List** — This bit indicates if the preparation of the alternative Sequence Command List is done and Command Sequence List must be swapped with the Restart Event. This bit is cleared when bit RSTA is set (Restart Event executed) and the Command Sequence List got swapped. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. This bit is forced to zero if bit CSL_BMOD is clear. Data Bus Control: This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. To set bit LDOK the bits LDOK and RSTA must be written simultaneously. After being set this bit can not be cleared by writing a value of 1'b1. See also Section 9.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. Internal Interface Control: This bit can be controlled via the internal interface Signal "LoadOK" and "Restart" if access control is configured accordingly via ACC_CFG[1:0]. With the assertion of Interface Signal "Restart" the interface Signal "LoadOK" is evaluated and bit LDOK set accordingly (bit LDOK set if Interface Signal "LoadOK" asserted when Interface Signal "Restart" asserts). General: Only in "Restart Mode" if a Restart Event occurs without bit LDOK being set the error flag LDOK_EIF is set except when the respective Restart Request occurred after or simultaneously with a Sequence Abort Request. The LDOK_EIF error flag is also not set in "Restart Mode" if the first Restart Event occurs after: - ADC got enabled - Exit from Stop Mode - ADC Soft-Reset 0 Load of alternative list done. 1 Load alternative list.

13.3.3.1.2 IDR0–IDR3 for Standard Identifier Mapping

Module Base + 0x00X0

	7	6	5	4	3	2	1	0
R W	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
Reset:	x	x	x	x	x	x	x	x

Figure 13-30. Identifier Register 0 — Standard Mapping

Table 13-30. IDR0 Register Field Descriptions — Standard

Field	Description
7-0 ID[10:3]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 13-31.

Module Base + 0x00X1

	7	6	5	4	3	2	1	0
R W	ID2	ID1	ID0	RTR	IDE (=0)			
Reset:	x	x	x	x	x	x	x	x

= Unused; always read ‘x’

Figure 13-31. Identifier Register 1 — Standard Mapping

Table 13-31. IDR1 Register Field Descriptions

Field	Description
7-5 ID[2:0]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 13-30.
4 RTR	**Remote Transmission Request** — This flag reflects the status of the Remote Transmission Request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)

13.4.5.7 Disabled Mode

The MSCAN is in disabled mode out of reset (CANE=0). All module clocks are stopped for power saving, however the register map can still be accessed as specified.

13.4.5.8 Programmable Wake-Up Function

The MSCAN can be programmed to wake up from sleep or power down mode as soon as CAN bus activity is detected (see control bit WUPE in MSCAN Control Register 0 (CANCTL0). The sensitivity to existing CAN bus action can be modified by applying a low-pass filter function to the RXCAN input line (see control bit WUPM in Section 13.3.2.2, “MSCAN Control Register 1 (CANCTL1)”).

This feature can be used to protect the MSCAN from wake-up due to short glitches on the CAN bus lines. Such glitches can result from—for example—electromagnetic interference within noisy environments.

13.4.6 Reset Initialization

The reset state of each individual bit is listed in Section 13.3.2, “Register Descriptions,” which details all the registers and their bit-fields.

13.4.7 Interrupts

This section describes all interrupts originated by the MSCAN. It documents the enable bits and generated flags. Each interrupt is listed and described separately.

13.4.7.1 Description of Interrupt Operation

The MSCAN supports four interrupt vectors (see Table 13-38), any of which can be individually masked (for details see Section 13.3.2.6, “MSCAN Receiver Interrupt Enable Register (CANRIER)” to Section 13.3.2.8, “MSCAN Transmitter Interrupt Enable Register (CANTIER)”).

Refer to the device overview section to determine the dedicated interrupt vector addresses.

Table 13-38. Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Wake-Up Interrupt (WUPIF)	I bit	CANRIER (WUPIE)
Error Interrupts Interrupt (CSCIF, OVRIF)	I bit	CANRIER (CSCIE, OVRIE)
Receive Interrupt (RXF)	I bit	CANRIER (RXFIE)
Transmit Interrupts (TXE[2:0])	I bit	CANTIER (TXEIE[2:0])

13.4.7.2 Transmit Interrupt

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXEx flag of the empty message buffer is set.

Chapter 14
Programmable Trigger Unit (PTUV3)

Table 14-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
01.00	21 Oct. 2011	all	Initial Version
02.00	22. Mar. 2012	14.3.2.1, 14.3.2.7, 14.3.2.10, 14.3.2.14 - 14.3.2.17	- removed PTUWP bit (now: PTUPTR is write protected if both TGs are disabled, TGxLxIDX is write protected if the associated TG is disabled) - TGxLIST bits are writeable if associated TG is disabled - PTULDOK bit is writable if both TGs are disabled - TGxLIST swap at every reload with LDOK set
3.0	16. Jul. 2013		minor corrections

Table 14-2. Terminology

Term	Meaning
TG	Trigger Generator
EOL	End of trigger list

14.1 Introduction

In PWM driven systems it is important to schedule the acquisition of the state variables with respect to PWM cycle.

The Programmable Trigger Unit (PTU) is intended to completely avoid CPU involvement in the time acquisitions of state variables during the control cycle that can be half, full, multiple PWM cycles.

All acquisition time values are stored inside the global memory map, basically inside the system memory; see the MMC section for the supported memory area. In such cases the pre-setting of the acquisition times needs to be completed during the previous control cycle to where the actual acquisitions are to be made.

14.1.1 Features

The PTU module includes these distinctive features:

- One 16 bit counter as time base for all trigger events
- Two independent trigger generators (TG0 and TG1)
- Up to 32 trigger events per trigger generator

In independent PWM operation, setting or clearing the OUT*n* bit activates or deactivates the PWM*n* output.

In complementary channel operation, the even-numbered OUT*n* bits replace the PWM generator outputs as inputs to the deadtime generators. Complementary channel pairs still cannot drive active level simultaneously, and the deadtime generators continue to insert deadtime in both channels of that pair, whenever an even OUT*n* bit toggles. Even OUT*n* bits control the top PWM signals while the odd OUT bits control the bottom PWM signals with respect to the even OUT*n* bits. Setting the odd OUT*n* bit makes its corresponding PWM the complement of its even pair, while clearing the odd OUT*n* bit deactivates the odd PWM.

Setting the OUTCTL*n* bits does not disable the PWM generators and current status sensing circuitry. They continue to run, but no longer control the outputs. When the OUTCTL*n* bits are cleared, the outputs of the PWM generator become the inputs to the deadtime generators at the beginning of the next PWM cycle. Software can drive the PWM outputs even when PWM enable bit (PWMEN*x*) is set to zero.

NOTE

Avoid an unexpected deadtime insertion by clearing the OUT*n* bits before setting and after clearing the OUTCTL*n* bits.

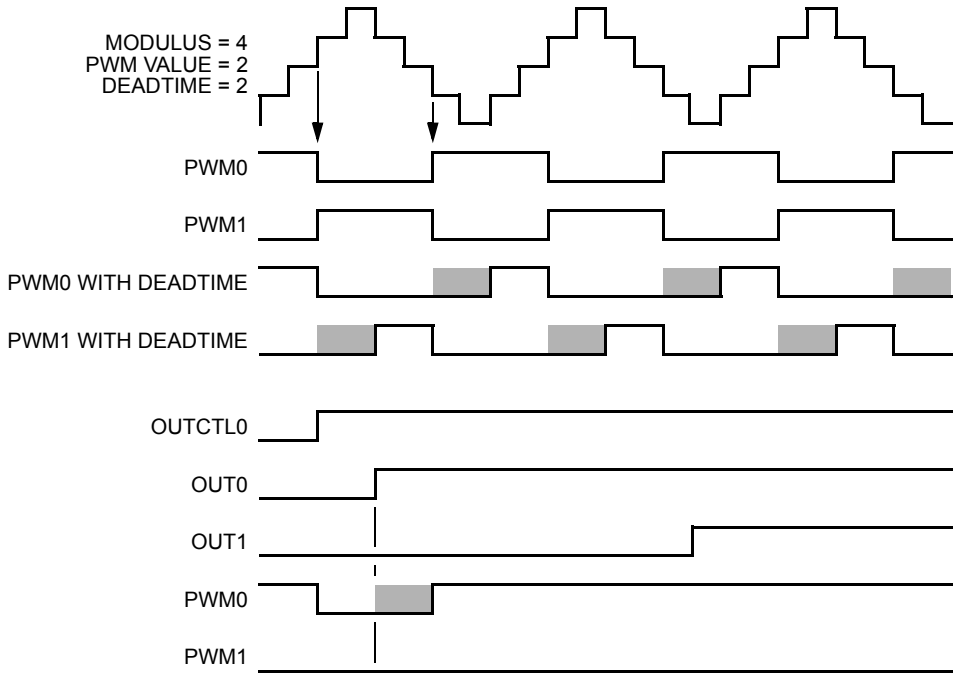

Figure 15-68. Setting OUT0 with OUTCTL Set in Complementary Mode

Table 17-4. SPICR2 Field Descriptions

Field	Description
6 XFRW	**Transfer Width —** This bit is used for selecting the data transfer width. If 8-bit transfer width is selected, SPIDRL becomes the dedicated data register and SPIDRH is unused. If 16-bit transfer width is selected, SPIDRH and SPIDRL form a 16-bit data register. Please refer to Section 17.3.2.4, “SPI Status Register (SPISR) for information about transmit/receive data handling and the interrupt flag clearing mechanism. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 8-bit Transfer Width (n = 8)(1) 1 16-bit Transfer Width (n = 16)[1]
4 MODFEN	**Mode Fault Enable Bit** — This bit allows the MODF failure to be detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration, refer to Table 17-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 $\overline{SS}$ port pin is not used by the SPI. 1 $\overline{SS}$ port pin with MODF feature.
3 BIDIROE	**Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode, this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state. 0 Output buffer disabled. 1 Output buffer enabled.
1 SPISWAI	**SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 SPI clock operates normally in wait mode. 1 Stop SPI clock generation when in wait mode.
0 SPC0	**Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 17-5. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

1. n is used later in this document as a placeholder for the selected transfer width.

Table 17-5. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

17.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 17-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 17-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 17-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 17-10).

18.3.2.9 GDU Boost Current Limit Register (GDUBCL)

Module Base + 0x0008 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	GBCL[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 18-11. GDU Boost Current Limit Register (GDUBCL)

1. Read: Anytime
   Write: Anytime if GWP=0

Table 18-12. GDU Boost Current Limit Register Field Descriptions

Field	Description
GBCL[3:0]	GDU Boost Current Limit Register— These bits are used to adjust the boost coil current limit $I_{COIL0,16}$ on the BST pin. These bits cannot be modified after GWP bit is set. See GDU electrical parameters.

18.3.2.10 GDU Phase Mux Register (GDUPHMUX)

Module Base + 0x0009 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	GPHMX[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-12. GDU Phase Mux Register (GDUPHMUX)

1. Read: Anytime
   Write: Anytime

Table 18-13. GDU Phase Mux Register Field Descriptions

Field	Description
[1:0] GPHMUX	GDU Phase Multiplexer — These buffered bits are used to select the voltage which is routed to internal ADC channel.The value written to the GDUPHMUX register does not take effect until the LDOK bit is set and the next PWM reload cycle begins. Reading GDUPHMUX register reads the value in the buffer. It is not necessary the value which is currently used. 00 Pin HD selected , V_{HD} / 12 connected to ADC channel 01 Pin HS0 selected , V_{HS0} / 6 connected to ADC channel 10 Pin HS1 selected , V_{HS1} / 6 connected to ADC channel 11 Pin HS2 selected, V_{HS2} / 6 connected to ADC channel

20.4.7.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 20-48. Erase Flash Block Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x09	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 20-49. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 20-29)
		Set if an invalid global address [23:0] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

20.4.7.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 20-50. Erase P-Flash Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0A	Global address [23:16] to identify P-Flash block to be erased
FCCOB1	Global address [15:0] anywhere within the sector to be erased. Refer to Section 20.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

21.4.2.3 Reserved Register

Module Base + 0x0002 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 21-4. Reserved Register

1. Read: Anytime
   Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only and is not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

21.4.2.4 CAN Physical Layer Status Register (CPSR)

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	CPCHVH	CPCHVL	CPCLVH	CPCLVL	CPDT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 21-5. CAN Physical Layer Status Register (CPSR)

1. Read: Anytime
   Write: Never

Table 21-6. CPSR Register Field Descriptions

Field	Description
7 CPCHVH	CANH Voltage Failure High Status Bit This bit reflects the CANH voltage failure high monitor status. 0 Condition $V_{CANH} < V_{H5}$ 1 Condition $V_{CANH} \geq V_{H5}$
6 CPCHVL	CANH Voltage Failure Low Status Bit This bit reflects the CANH voltage failure low monitor status. 0 Condition $V_{CANH} > V_{H0}$ 1 Condition $V_{CANH} \leq V_{H0}$
5 CPCLVH	CANL Voltage Failure High Status Bit This bit reflects the CANL voltage failure high monitor status. 0 Condition $V_{CANL} < V_{L5}$ 1 Condition $V_{CANL} \geq V_{L5}$

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0006 PWMCLKAB [1]	R	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
	W								
0x0007 RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x0008 PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0009 PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x000A RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x000B RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x000C PWMCNT0 [2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000D PWMCNT1[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000E PWMCNT2[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000F PWMCNT3[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0010 PWMCNT4[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0011 PWMCNT5[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0012 PWMCNT6[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0013 PWMCNT7[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 22-2. The scalable PWM Register Summary (Sheet 2 of 4)

Appendix E
GDU Electrical Specifications

NOTE

It is necessary to consider the power dissipation of the FET channel versus the power dissipation in the FET-Predriver.

FET-Predriver dissipation is Power VSUP x f(PWM) x C(FET-GATE)
FET channel power dissipation is a function of channel current and voltage.

Reducing the RDSON of the external FET to reduce the FET power dissipation increases the FET gate capacitance.

At a certain FET level, further reduction of FET RDSON actually increases overall power consumption because the increased charging and discharging power dissipation due to increased gate capacitance outweighs the FET power reduction due to RDSON reduction.

E.1 GDU specifications for devices featuring GDU V4 or V6

Table E-1. GDU Electrical Characteristics (Junction Temperature From –40°C To +175°C)

4.85V<=VDDX,VDDA<=5.15V						
Num	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	VSUP Supply range	V_{VSUP}	-0.3	—	40	V
2a	VSUP, HD Supply range FETs can be turned on(1) (normal range)	V_{VSUP}/V_{HD}	7	14	20	V
2b	VSUP, HD Supply range FETs can be turned on(2) (extended range)	V_{VSUP}/V_{HD}	7	14	26.6	V
3	External FET Vgs drive with boost(3) (7V < V_{RBATP} < 20V)	V_{VGS}	9	9.6	12	V
4	External FET Vgs drive without boost(4)	V_{VGS}	5	9.6	12	V
5	External FET total gate charge @ 10V(5)	QG	—	75	—	nC
6	Pull resistance between HGx and HSx	R_{HSpul}	60	80	120	KΩ
7	Pull resistance between LGx and LSx	R_{LSpul}	60	80	120	KΩ
8a	VLS output voltage for Vsup >=12.5V, Iout=30mA -40°C < T_j < 150°C	V_{VLS_OUT}	10.5	11	11.5	V
8b	VLS output voltage for Vsup >=12.5V, Iout=30mA 150°C < T_j < 175°C	V_{VLS_OUT}	10.0	10.6	11.5	V
9	VLS current limit threshold	I_{LIMVLS}	60	77	112	mA
10a	VLS low voltage monitor trippoint assert (GDUV6 with GVLSLVL=1 or GDUV4)	V_{LVLSHA}	6.2	6.5	7	V
10b	VLS low voltage monitor trippoint deassert (GDUV6 with GVLSLVL=1 or GDUV4)	V_{LVLSHD}	6.2	6.58	7	V
10c	VLS low voltage monitor trippoint assert (GDUV6 with GVLSLVL=0)	V_{LVLSLA}	5.2	5.5	6	V
10d	VLS low voltage monitor trippoint deassert (GDUV6 with GVLSLVL=0)	V_{LVLSLD}	5.2	5.55	6	V
11a	HD high voltage monitor assert trippoint low	V_{HVHDLA}	20	21	22	V

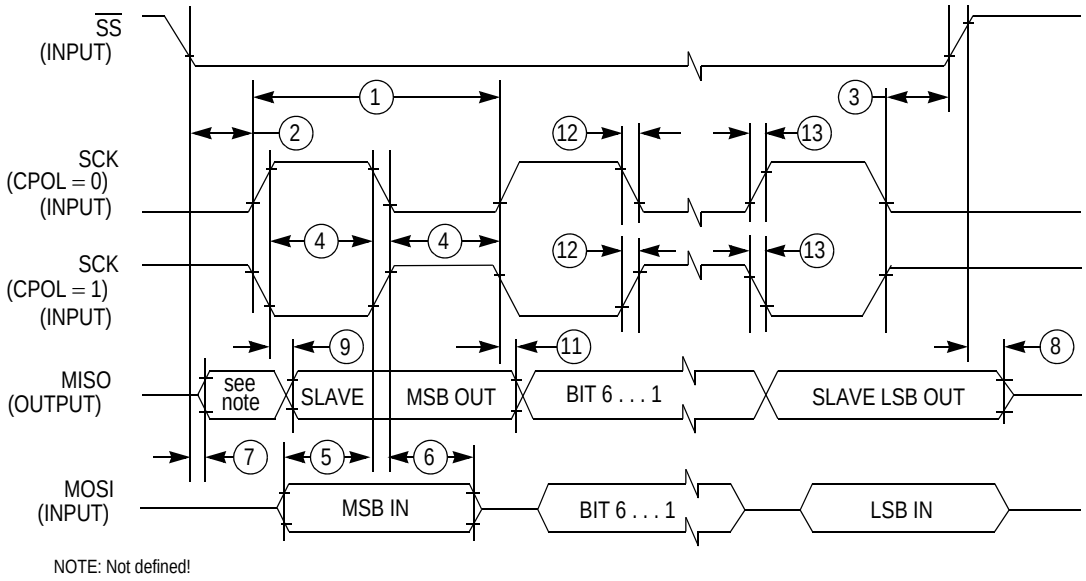

Figure I-6. SPI Slave Timing (CPHA=1)

Table I-2. SPI Slave Mode Timing Characteristics -40°C to 175°C

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1		SCK Frequency	f_{sck}	DC	—	1/4[1]	f_{bus}
1		SCK Period	t_{sck}	4	—	∞	t_{bus}
2		Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3		Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4		Clock (SCK) High or Low Time	t_{wsck}	$2t_{bus}$ - (t_{rfi} + t_{rfo})	—	—	ns
5		Data Setup Time (Inputs)	t_{su}	3	—	—	ns
6		Data Hold Time (Inputs)	t_{hi}	2	—	—	ns
7		Slave Access Time (time to data active)	t_a	—	—	28	ns
8		Slave MISO Disable Time	t_{dis}	—	—	26	ns
9a		Data Valid after SCK Edge (-40°C < T_j < 150°C)	t_{vsck}	—	—	$23 + 0.5 \cdot t_{bus}$ [2]	ns
9b		Data Valid after SCK Edge (150°C <T_j < 175°C)[1]	t_{vsck}	—	—	$25 + 0.5 \cdot t_{bus}$ [2]	ns
10a		Data Valid after $\overline{SS}$ fall (-40°C < T_j < 150°C)	t_{vss}	—	—	$23 + 0.5 \cdot t_{bus}$ [2]	ns
10b		Data Valid after $\overline{SS}$ fall (150°C < T_j < 175°C)[1]	t_{vss}	—	—	$25 + 0.5 \cdot t_{bus}$ [2]	ns
11		Data Hold Time (Outputs)	t_{ho}	22	—	—	ns
12		Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13		Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

1. f_{bus} max is 40MHz at temperatures above 150°C

2. $0.5t_{bus}$ added due to internal synchronization delay