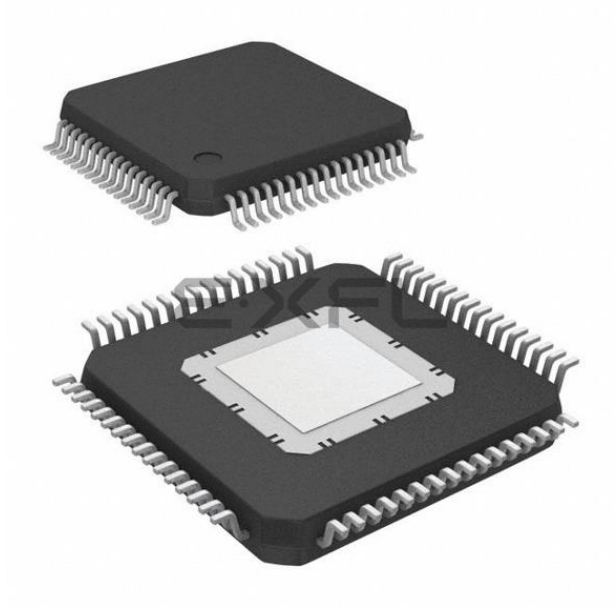

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S12Z
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml64f2wkh

Table 0-1. Revision History

Date	Revision	Description
22 MAY2014	1.4	Updated family derivative table for S12ZVML32, S12ZVM32 and S12ZVM16 devices Added 64KB, 32KB and 16KB derivative information to flash module chapter Added pin routing options for S12ZVM32 and S12ZVM16 devices Added HV Phy information for the S12ZVM32 and S12ZVM16 derivatives Updated Part ID assignment table and ordering information for S12ZVM32 and S12ZVM16 Corrected PLL VCO maximum frequency specification Changed V_{LVLSA} maximum from 7V to 6.9V Added electrical parameter for HD division ratio through the phase multiplexer Corrected preferred VRL reference from VRL_1 to VRL_0 Included NVM timing parameters for the S12ZVM32 and S12ZVM16 devices Added GDU S12ZVM32 and S12ZVM16 specific differences and electrical specifications Added references to f_{WSTAT} Added VDDX short circuit fall back current and temperature/input dependency specs.
22 SEP 2014	1.5	Removed incorrect references to PACLK in TIM chapter Improved clarity of routing options in PIM chapter. Updated S12ZVM- Family derivative table. Added 48LQFP thermal package parameters Extended LINPHY specification range minimum to 5V Updated BKGD pin I/O specification Specified ADC accuracy for a range of VDDA and VREF.
20 MAR 2015	2.0	Added ZVMC256 information Added mask set 2N95G information Added more detailed PTU minimum trigger spacing description Updated CPMU, PIM and GDU chapters for ZVMC256 Improved CPMU specification clarity (see CPMU revision history) Removed electrical parameter classification Added reset startup timing parameter Updated BATS parameters Extended BKGD V_{IL} condition from 3.15V to 3.13V Extended GDU operating range from 26V to 26.6V Temperature sensor output at 150C changed from 2.25V to 2.33V. Added GDU VBS current parameter Updated package thermal information for ZVM32 and ZVM16 parts Added VBG temperature and voltage dependency parameters Added device stop current at 105C.
22 APR 2015	2.1	Updated Stop and Wait current parameter values (I_{SUPS}, I_{SUPW}) Corrected 80LQFP-EP pin name from VSS2 to VSS1 Updated ZVMC256 VDDS regulator parameters. Changed PL0 ESD specification Minor corrections to PIM, PMF, SRAM and ADC chapters (see module revision histories)
27 APR 2015	2.2	Updated Stop current parameter values (I_{SUPS}) Updated LINPHY parameter range limit to 5.5V Added more information about VDDS1, VDDS2, SNPS1, SNPS2 to CPMU chapter. Reintroduced EPRES bit for GDU V4 Added 80LQFP-EP mechanical package information

Chapter 18
Gate Drive Unit (GDU)

Chapter 19
LIN/HV Physical Layer (S12LINPHYV3)

Table 1-21. Control Loop Events

Device Level Event	TIM0	PMF	PTU	ADC0	ADC1
commutation_event	OC0[1]	commutation_event	—	—	—
reload	—	reloada[2]	reload	Restart	Restart
async_reload	—	async_reload	async_reload	Seq_abort	Seq_abort
trigger_0	—	—	trigger_0	Trigger	—
trigger_1	—	—	trigger_1	—	Trigger
glb_ldok	—	glb_ldok	glb_ldok	LoadOK	LoadOK

1. TIM channel OC0 must be configured to toggle on both edges.

2. PMF events reloadb and reloadc are not connected at device level

Each control loop cycle is started by a PMF **reload** event. The PMF reload event restarts the PTU time base. If the PTU is enabled, the reload is immediately passed through to the ADC and GDU modules.

The PMF generates the **reload** event at the required PWM reload frequency. The PMF reload event causes the PTU time base to restart, to acquire the first trigger times from the list and the ADCs to start loading the ADC conversion command from the Command Sequence List (CSL).

NOTE

In the PTU there is time window after the **reload** event assertion before the first trigger is permitted. This time can be up to 10 bus cycles.

Subsequent triggers also require a load time of 6 bus clock cycles (one trigger generator enabled) or 10 bus clock cycles (both trigger generators enabled). This defines the minimal spacing between triggers without causing a PTU trigger generator timing error.

In the ADC there is 10 bus cycle maximum time window after the **reload** event assertion to access the first ADC command from the list. In this window the ADC conversion can not be started. If the measurement is control loop related these delays are negligible due to much larger delays in the PWM-GDU-feedback loop.

When the trigger time is encountered the corresponding PTU trigger generates the **trigger_x** event for the associated ADC. For simultaneous sampling the PTU generates simultaneous **trigger_x** events for both ADCs. At the **trigger_x** event the ADC starts the first conversion of the next conversion sequence in the CSL (the first ADC command is already downloaded).

A commutation event is used by the PMF to generate an async_reload event. The async_reload is used by the PTU to update lists and re-initialize the trigger lists. If the PTU is enabled the async_reload is immediately passed through to the ADC.

Table 6-35. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
1	1	1	Read match

6.3.2.19 Debug Comparator C Address Register (DBGCAH, DBGCAM, DBGCAL)

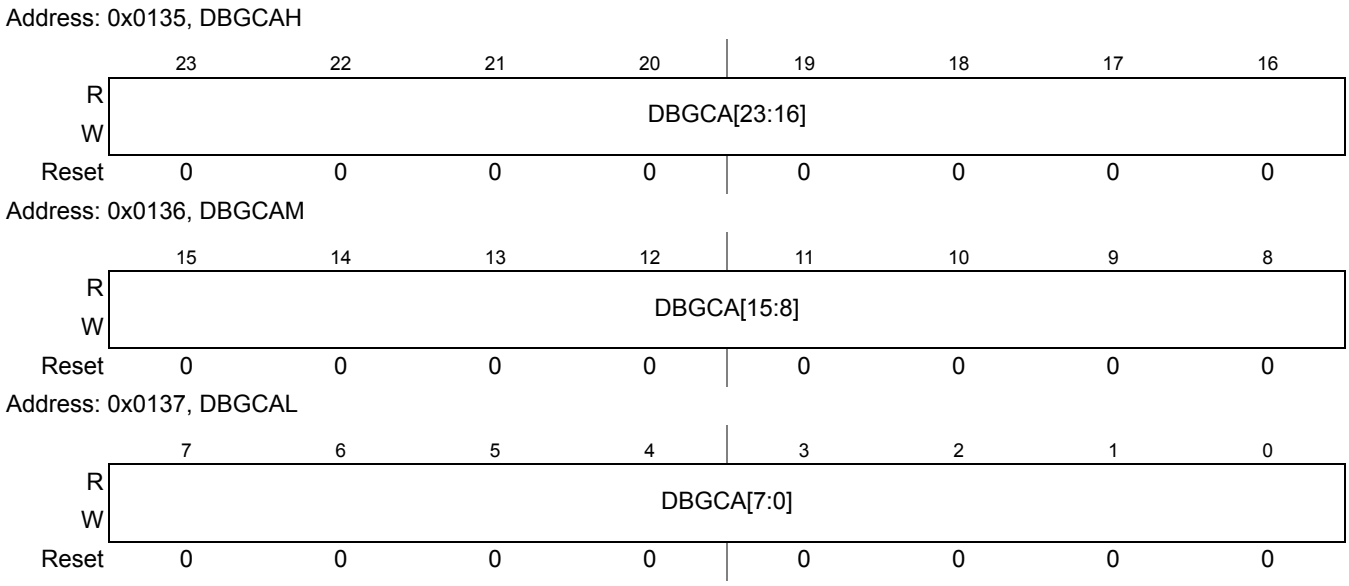

Figure 6-21. Debug Comparator C Address Register

Read: Anytime.

Write: If DBG not armed and PTACT is clear.

Table 6-36. DBGCAH, DBGCAM, DBGCAL Field Descriptions

Field	Description
23–16 DBGCA [23:16]	**Comparator Address Bits [23:16]**— These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one
15–0 DBGCA [15:0]	**Comparator Address Bits**[15:0]— These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

9.5.2 Register Descriptions

This section describes in address order all the ADC12B_LBA registers and their individual bits.

9.5.2.1 ADC Control Register 0 (ADCCTL_0)

Module Base + 0x0000

	15	14	13	12	11	10	9	8
R W	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-4. ADC Control Register 0 (ADCCTL_0)

Read: Anytime

Write:

- Bits ADC_EN, ADC_SR, FRZ_MOD and SWAI writable anytime
- Bits MOD_CFG, STR_SEQA and ACC_CFG[1:0] writable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-3. ADCCTL_0 Field Descriptions

Field	Description
15 ADC_EN	**ADC Enable Bit** — This bit enables the ADC (e.g. sample buffer amplifier etc.) and controls accessibility of ADC register bits. When this bit gets cleared any ongoing conversion sequence will be aborted and pending results or the result of current conversion gets discarded (not stored). The ADC cannot be re-enabled before any pending action or action in process is finished or aborted, which could take up to a maximum latency time of $t_{DISABLE}$ (see device reference manual for more details). Because internal components of the ADC are turned on/off with this bit, the ADC requires a recovery time period (t_{REC}) after ADC is enabled until the first conversion can be launched via a trigger. 0 ADC disabled. 1 ADC enabled.
14 ADC_SR	ADC Soft-Reset — This bit causes an ADC Soft-Reset if set after a severe error occurred (see list of severe errors in Section 9.5.2.9, “ADC Error Interrupt Flag Register (ADCEIF) that causes the ADC to cease operation). It clears all overrun flags and error flags and forces the ADC state machine to its idle state. It also clears the Command Index Register, the Result Index Register, and the CSL_SEL and RVL_SEL bits (to be ready for a new control sequence to load new command and start execution again from top of selected CSL). A severe error occurs if an error flag is set which cause the ADC to cease operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. Once this bit is set it can not be cleared by writing any value. It is cleared only by ADC hardware after the Soft-Reset has been executed. 0 No ADC Soft-Reset issued. 1 Issue ADC Soft-Reset.
13 FRZ_MOD	Freeze Mode Configuration — This bit influences conversion flow during Freeze Mode. 0 ADC continues conversion in Freeze Mode. 1 ADC freezes the conversion at next conversion boundary at Freeze Mode entry.
12 SWAI	Wait Mode Configuration — This bit influences conversion flow during Wait Mode. 0 ADC continues conversion in Wait Mode. 1 ADC halts the conversion at next conversion boundary at Wait Mode entry.

- Three complementary pairs and zero independent PWM outputs
- Zero complementary pairs and six independent PWM outputs

All PWM outputs can be generated from the same counter, or each pair can have its own counter for three independent PWM frequencies. Complementary operation permits programmable deadtime insertion, distortion correction through current sensing by software, and separate top and bottom output polarity control. Each counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width-control and full range modulation from 0 percent to 100 percent, are supported. The PMF is capable of controlling most motor types: AC induction motors (ACIM), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

15.1.1 Features

- Three complementary PWM signal pairs, or six independent PWM signals
- Edge-aligned or center-aligned mode
- Features of complementary channel operation:
  - — Deadtime insertion
  - — Separate top and bottom pulse width correction via current status inputs or software
  - — Three variants of PWM output:
    - – Asymmetric in center-aligned mode
    - – Variable edge placement in edge-aligned mode
    - – Double switching in center-aligned mode
- Three 15-bit counters based on core clock
- Separate top and bottom polarity control
- Half-cycle reload capability
- Integral reload rates from 1 to 16
- Programmable fault protection
- Link to timer output compare for 6-step BLDC commutation support with optional counter restart Reload overrun interrupt
- PWM compare output polarity control Software-controlled PWM outputs, complementary or independent

15.1.2 Modes of Operation

Care must be exercised when using this module in the modes listed in Table 15-4. Some applications require regular software updates for proper operation. Failure to do so could result in destroying the hardware setup. Because of this, PWM outputs are placed in their inactive states in STOP mode, and optionally under WAIT and FREEZE modes. PWM outputs will be reactivated (assuming they were active to begin with) when these modes are exited.

15.1.3 Block Diagram

Figure 15-1 provides an overview of the PMF module.

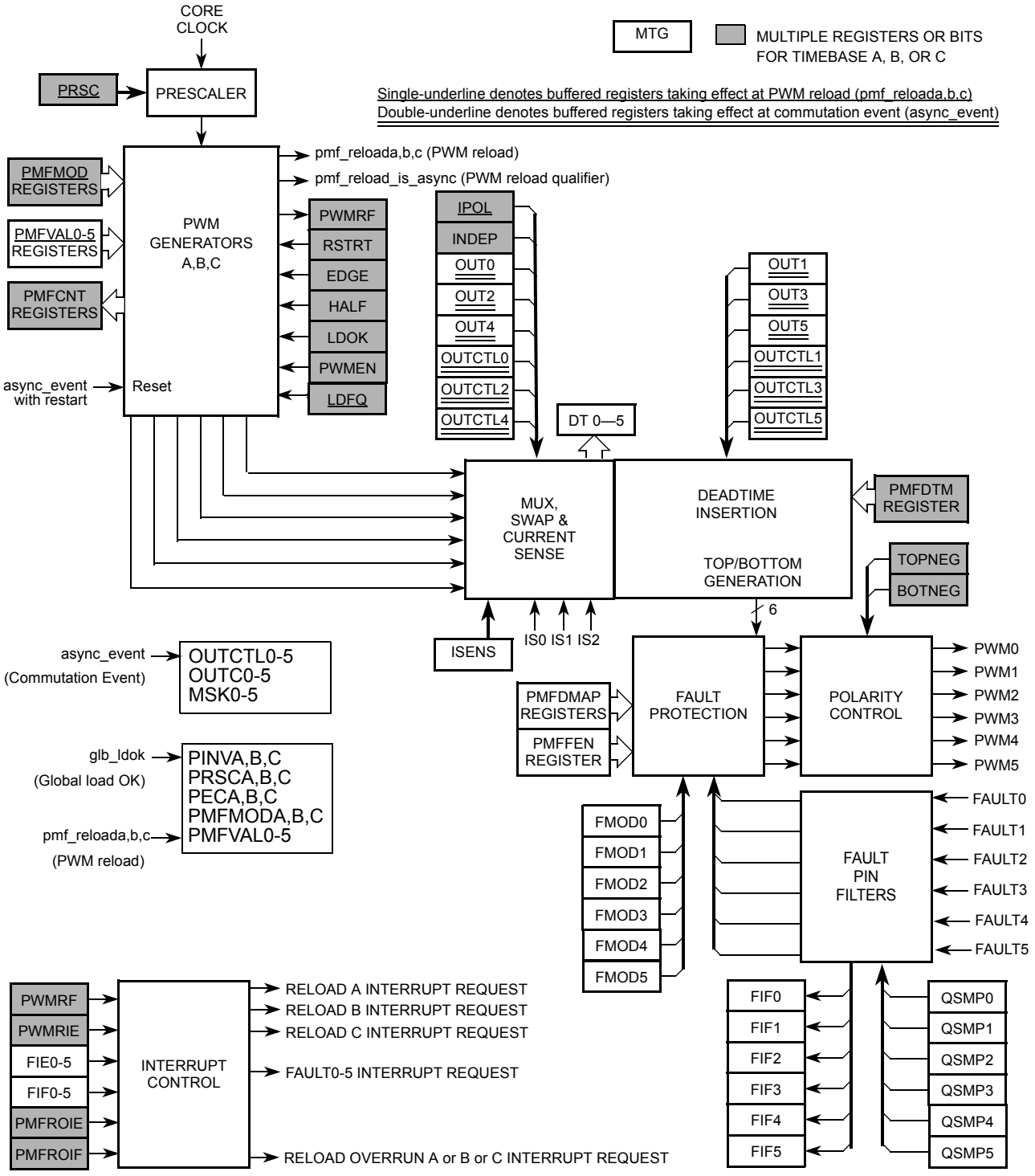

Figure 15-1. PMF Block Diagram

buffered mode. In addition, if restart is enabled (RSTRTx=1), the commutation event generates both “PWM reload event” and “PWM reload-is-asynchronous event” simultaneously.

15.2.6 Commutation Event Edge Select Signal — async_event_edge_sel[1:0]

These device-internal PMF input signals select the active edge for the async_event input. Refer to the device overview section to determine if the selection is user configurable or tied constant at integration level.

Table 15-5. Commutation Event Edge Selection

async_event_edge-sel[1:0]	async_event active edge
00	direct input
01	rising edge
10	falling edge
11	both edges

15.2.7 PWM Reload Event Signals — pmf_reloada,b,c

These device-internal PMF output signals assert once per control cycle and can serve as triggers for other implemented IP modules. Signal pmf_reloadb and pmf_reloadc are related to time base B and C, respectively, while signal pmf_reloada is off out of reset and can be programmed for time base A, B, or C. Refer to the device overview section to determine the signal connections.

15.2.8 PWM Reload-Is-Asynchronous Signal — pmf_reload_is_async

This device-internal PMF output signal serves as a qualifier to the PMF reload event signal pmf_reloada. Whenever the async_event signal causes pmf_reloada output to assert also the pmf_reload_is_async output asserts for the same duration, except if asynchronous event and generated PWM reload event occur in the same cycle.

16.3.2.9 SCI Data Registers (SCIDRH, SCIDRL)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	R8	T8	0	0	0	Reserved	Reserved	Reserved
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-12. SCI Data Registers (SCIDRH)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 16-13. SCI Data Registers (SCIDRL)

Read: Anytime; reading accesses SCI receive data register

Write: Anytime; writing accesses SCI transmit data register; writing to R8 has no effect

NOTE

The reserved bit SCIDRH[2:0] are designed for factory test purposes only, and are not intended for general user access. Writing to these bit is possible when in special mode and can alter the modules functionality.

Table 16-13. SCIDRH and SCIDRL Field Descriptions

Field	Description
SCIDRH 7 R8	**Received Bit 8** — R8 is the ninth data bit received when the SCI is configured for 9-bit data format (M = 1).
SCIDRH 6 T8	**Transmit Bit 8** — T8 is the ninth data bit transmitted when the SCI is configured for 9-bit data format (M = 1).
SCIDRL 7:0 R[7:0] T[7:0]	**R7:R0** — Received bits seven through zero for 9-bit or 8-bit data formats **T7:T0** — Transmit bits seven through zero for 9-bit or 8-bit formats

NOTE

If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten.The same value is transmitted until T8 is rewritten

In 8-bit data format, only SCI data register low (SCIDRL) needs to be accessed.

1. The address bit identifies the frame as an address character. See Section 16.4.6.6, “Receiver Wakeup”.

16.4.4 Baud Rate Generation

A 16-bit modulus counter in the two baud rate generator derives the baud rate for both the receiver and the transmitter. The value from 0 to 65535 written to the SBR15:SBR0 bits determines the baud rate. The value from 0 to 4095 written to the SBR15:SBR4 bits determines the baud rate clock with SBR3:SBR0 for fine adjust. The SBR bits are in the SCI baud rate registers (SCIBDH and SCIBDL) for both transmit and receive baud generator. The baud rate clock is synchronized with the bus clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver has an acquisition rate of 16 samples per bit time.

Baud rate generation is subject to one source of error:

- Integer division of the bus clock may not give the exact target frequency.

Table 16-16 lists some examples of achieving target baud rates with a bus clock frequency of 25 MHz.

When IREN = 0 then,

SCI baud rate = SCI bus clock / (SCIBR[15:0])

Table 16-16. Baud Rates (Example: Bus Clock = 25 MHz)

Bits SBR[15:0]	Receiver(1) Clock (Hz)	Transmitter(2) Clock (Hz)	Target Baud Rate	Error (%)
109	3669724.8	229,357.8	230,400	.452
217	1843318.0	115,207.4	115,200	.006
651	614439.3	38,402.5	38,400	.006
1302	307219.7	19,201.2	19,200	.006
2604	153,609.8	9600.6	9,600	.006
5208	76,804.9	4800.3	4,800	.006
10417	38,398.8	2399.9	2,400	.003
20833	19,200.3	1200.02	1,200	.00
41667	9599.9	600.0	600	.00
65535	6103.6	381.5		

1. 16x faster then baud rate

2. divide 1/16 form transmit baud generator

Table 18-2. GDUV4/V5/V6 Differences(1)

Feature	GDU V4	GDU V5	GDU V6
On chip bootstrap diode	not available, off chip bootstrap diode required	available	not available, off chip bootstrap diode required
Desaturation filter bits GDSFLS/GDSFHS	not available	available	available
Fault[3] output to PMF	driven by GLVLSIF	driven by GLVLSF	driven by GLVLSF
Fault[4] output to PMF	driven by GHHDIF	driven by GHHDF	driven by GHHDF
Low-side drivers on or off out of reset dependent on NVM option	available[1.]	available[1.]	available
additional drain connections LD[2:0] to external low-side power FETs	not available	not available	available
Control bits GSRMOD1/0 for SR motor drive	not available	not available	available

1. Refer to device overview for mask set / GDU version info.

The GDU module is a Field Effect Transistor (FET) pre-driver designed for three phase motor control applications.

18.1.1 Features

The GDU module includes these distinctive features:

- 11V voltage regulator for FET pre-drivers
- Boost converter option for low supply voltage condition
- 3-phase bridge FET pre-drivers
- Bootstrap circuit for high-side FET pre-drivers with external bootstrap capacitor
- Charge pump for static high-side driver operation
- Phase voltage measurement with internal ADC
- Two low-side current measurement amplifiers for DC phase current measurement
- Phase comparators for BEMF zero crossing detection in sensorless BLDC applications
- Voltage measurement on HD pin (DC-Link voltage) with internal ADC
- Desaturation comparator for high-side drivers and low-side drivers protection
- Undervoltage detection on FET pre-driver supply pin VLS
- Two overcurrent comparators with programmable voltage threshold
- Overvoltage detection on 3-phase bridge supply HD pin

Table 18-3. GDUE Register Field Description

Field	Description
1 GCPE	**GDU Charge Pump Enable** — This bit enables the charge pump. This bit cannot be modified after GWP bit is set. See Section 18.4.4, “Charge Pump 0 Charge pump is disabled 1 Charge pump is enabled
0 GFDE	**GDU FET Pre-Driver Enable** — This bit enables the low-side and high-side FET pre-drivers. It must also be set in order to use the boost converter and the current sense amplifiers. This bit cannot be modified after GWP bit is set.See Section 18.4.2, “Low-Side FET Pre-Drivers and Section 18.4.3, “High-Side FET Pre-Driver. 0 Low-side and high-side drivers are disabled 1 Low-side and high-side drivers are enabled **NOTE** It is not allowed to set and clear GFDE bit periodically in order to switch on and off the FET pre-drivers. In order to switch on and off the FET pre-drivers the PMF module has to be used to mask and un-mask the PWM channels.

Table 18-11. Boost Option Clock Divider Factors k = f_{BUS} / f_{BOOST}

GBOCD[4:0]	f_{BOOST}
00000	f_{BUS} / 4
00001	f_{BUS} / 4
00010	f_{BUS} / 4
00011	f_{BUS} / 4
00100	f_{BUS} / 4
00101	f_{BUS} / 4
00110	f_{BUS} / 6
00111	f_{BUS} / 6
01000	f_{BUS} / 8
01001	f_{BUS} / 8
01010	f_{BUS} / 10
01011	f_{BUS} / 10
01100	f_{BUS} / 12
01101	f_{BUS} / 12
01110	f_{BUS} / 14
01111	f_{BUS} / 14
10000	f_{BUS} / 16
10001	f_{BUS} / 24
10010	f_{BUS} / 32
10011	f_{BUS} / 48
10100	f_{BUS} / 64
10101	f_{BUS} / 96
10110	f_{BUS} / 100
10111	f_{BUS} / 128
11000	f_{BUS} / 192
11001	f_{BUS} / 200
11010	f_{BUS} / 256

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 20-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 20-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 20.4.5, “Flash Command Operations,” for more information.

Table 20-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN(1)	MAX(2)		MIN[1]	MAX[2]	
1.0	1.6	0x00	26.6	27.6	0x1A
1.6	2.6	0x01	27.6	28.6	0x1B
2.6	3.6	0x02	28.6	29.6	0x1C
3.6	4.6	0x03	29.6	30.6	0x1D
4.6	5.6	0x04	30.6	31.6	0x1E
5.6	6.6	0x05	31.6	32.6	0x1F
6.6	7.6	0x06	32.6	33.6	0x20
7.6	8.6	0x07	33.6	34.6	0x21
8.6	9.6	0x08	34.6	35.6	0x22
9.6	10.6	0x09	35.6	36.6	0x23
10.6	11.6	0x0A	36.6	37.6	0x24
11.6	12.6	0x0B	37.6	38.6	0x25
12.6	13.6	0x0C	38.6	39.6	0x26
13.6	14.6	0x0D	39.6	40.6	0x27
14.6	15.6	0x0E	40.6	41.6	0x28
15.6	16.6	0x0F	41.6	42.6	0x29
16.6	17.6	0x10	42.6	43.6	0x2A
17.6	18.6	0x11	43.6	44.6	0x2B

Table 20-32. Allowed P-Flash and EEPROM Simultaneous Operations on a single hardblock

	EEPROM				
Program Flash	**Read**	**Margin Read[2]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read	OK[(1)]	OK	OK	OK	
Margin Read[(2)]					
Program					
Sector Erase					
Mass Erase[(3)]					OK

1. Strictly speaking, only one read of either the P-Flash or EEPROM can occur at any given instant, but the memory controller will transparently arbitrate P-Flash and EEPROM accesses giving uninterrupted read access whenever possible.

2. A 'Margin Read' is any read after executing the margin setting commands 'Set User Margin Level' or 'Set Field Margin Level' with anything but the 'normal' level specified. See the Note on margin settings in Section 20.4.7.12 and Section 20.4.7.13.

3. The 'Mass Erase' operations are commands 'Erase All Blocks' and 'Erase Flash Block'

20.4.7 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation may return invalid data resulting in an illegal access (as described on Section 20.4.6).

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 20.3.2.7).

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

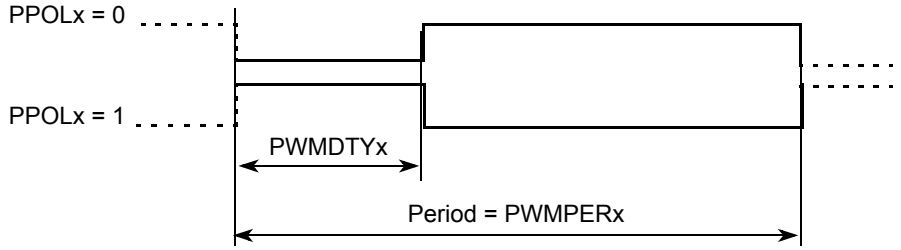

Figure 22-17. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a% of period):
  - — Polarity = 0 (PPOLx = 0)

    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - — Polarity = 1 (PPOLx = 1)

    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = bus clock, where bus clock = 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/4 = 2.5 MHz

PWMx Period = 400 ns

PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 22-18.

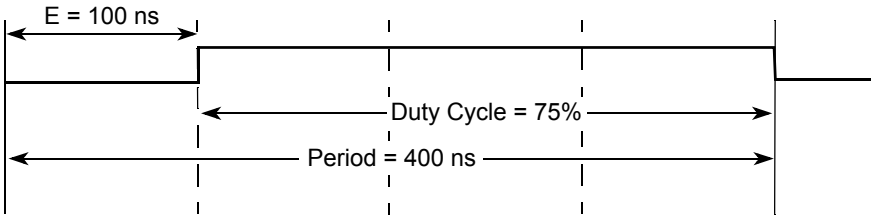

Figure 22-18. PWM Left Aligned Output Example Waveform

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise.

For better immunity to ESD events, the PCB test point for the BST pin should be located at a distance from the device to increase the track length to the BST pin, but the diode should be located close to the device. This may require a track branch on the PCB to ensure that the test point is further away from the device than the diode.

Table A-3. ESD and Latch-up Test Conditions

Model	Spec	Description	Symbol	Value	Unit
Human Body	JESD22-A114	Series Resistance	R	1500	Ω
		Storage Capacitance	C	100	pF
		Number of Pulses per pin positive negative	-	- 1 1	
Charged-Device	JESD22-C101	Series Resistance	R	0	Ω
		Storage Capacitance	C	4	pF
Latch-up for 5V GPIOs		Minimum Input Voltage Limit		-2.5	V
		Maximum Input Voltage Limit		+7.5	V
Latch-up for HD, VCP, BST, LIN, BCTL, BCTLC		Minimum Input Voltage Limit		-7	V
		Maximum Input Voltage Limit		+27	V
Latch-up for CANH,CANL, SPLIT		Minimum Input Voltage Limit		-7	V
		Maximum Input Voltage Limit		+21	V
Latch-up for HG,HS		Minimum Input Voltage Limit		-5	V
		Maximum Input Voltage Limit (VBS=10V)		15	V
Latch-up for LG,LS, LD		Minimum Input Voltage Limit		-5	V
		Maximum Input Voltage Limit (VLS=10V)		15	V

Table A-4. ESD Protection and Latch-up Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1		Human Body Model (HBM): - LIN versus LGND - CANH, CANL, SPLIT, PL0 - All other pins	 V_{HBM} V_{HBM} V_{HBM}	 +/-6 +/-4 +/-2	 - - -	KV
2		Charged-Device Model (CDM): Corner Pins	V_{CDM}	+/-750	-	V
3		Charged-Device Model (CDM): All other pins	V_{CDM}	+/-500	-	V
4		Direct Contact Discharge IEC61000-4-2 with and with out 220pF capacitor (R=330, C=150pF): LIN versus LGND, CANH, CANL	V_{ESDIEC}	+/-6	-	KV

M.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0103	DBGTCRL[2]	R	0	0	0	PREND[(1)]	DSTAMP	PDOE	PROFILE	STAMP
		W								
0x0104	DBGTBH[2]	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0105	DBGTBL[2]	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0106	DBGCNT[2]	R	0	CNT						
		W								
0x0107	DBGSCR1	R	C3SC1	C3SC0	C2SC1[2]	C2SC0[2]	C1SC1	C1SC0	C0SC1	C0SC0
		W								
0x0108	DBGSCR2	R	C3SC1	C3SC0	C2SC1[2]	C2SC0[2]	C1SC1	C1SC0	C0SC1	C0SC0
		W								
0x0109	DBGSCR3	R	C3SC1	C3SC0	C2SC1[2]	C2SC0[2]	C1SC1	C1SC0	C0SC1	C0SC0
		W								
0x010A	DBGEFR	R	PTBOVF[2]	TRIGF	0	EEVF	ME3	ME2[2]	ME1	ME0
		W								
0x010B	DBGSR	R	TBF[2]	0	0	PTACT[2]	0	SSF2	SSF1	SSF0
		W								
0x010C-0x010F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0110	DBGACTL	R	0	NDB	INST	0	RW	RWE	reserved	COMPE
		W								
0x0111-0x0114	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0115	DBGAAH	R	DBGAA[23:16]							
		W								
0x0116	DBGAAM	R	DBGAA[15:8]							
		W								
0x0117	DBGAAL	R	DBGAA[7:0]							
		W								
0x0118	DBGAD0	R	Bit 31	30	29	28	27	26	25	Bit 24
		W								
0x0119	DBGAD1	R	Bit 23	22	21	20	19	18	17	Bit 16
		W								
0x011A	DBGAD2	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x011B	DBGAD3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

M.18 0x0700-0x0707 SCI0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0706	SCI0DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0707	SCI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

M.19 0x0710-0x0717 SCI1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0710	SCI1BDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x0711	SCI1BDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x0712	SCI1CR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x0710	SCI1ASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		W								
0x0711	SCI1ACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		W								
0x0712	SCI1ACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
		W								
0x0713	SCI1CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x0714	SCI1SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x0715	SCI1SR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x0716	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0717	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.