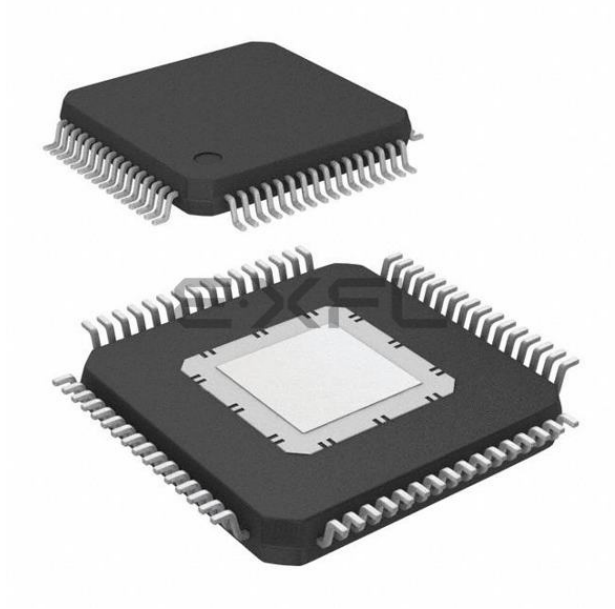

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | S12Z |
| Core Size | 16-Bit |
| Speed | 50MHz |
| Connectivity | CANbus, LINbus, SCI, SPI |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 31 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 40V |
| Data Converters | A/D 9x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 150°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP Exposed Pad |
| Supplier Device Package | 64-HLQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvml64f3wkh |

### 1.8.7 FTMRZ Connectivity

The soc_erase_all_req input to the flash module is driven directly by a BDC erase flash request resulting from the BDC ERASE_FLASH command.

The FTMRZ FCLKDIV register is forced to 0x05 by the BDC ERASE_FLASH command. This configures the clock frequency correctly for the initial bus frequency on leaving reset. The bus frequency must not be changed before launching the ERASE_FLASH command.

The device bus frequency, below which the flash wait states can be disabled, is specified in the device operating conditions table in Table A-6.

### 1.8.8 CPMU Connectivity

The API clock generated in the CPMU is not mapped to a device pin in the MC9S12ZVM-Family.

## 1.9 Modes of Operation

The MCU can operate in different modes. These are described in 1.9.1 Chip Configuration Modes.

The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in 1.9.3 Low Power Modes.

Some modules feature a software programmable option to freeze the module status whilst the background debug module is active to facilitate debugging. This is referred to as freeze mode at module level.

### 1.9.1 Chip Configuration Modes

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (Table 1-13). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of $\overline{\text{RESET}}$.

**Table 1-13. Chip Modes**

| Chip Modes | MODC |
|---|---|
| Normal single chip | 1 |
| Special single chip | 0 |

#### 1.9.1.1 Normal Single-Chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

4. Verify fault flags and service if necessary
5. Execute the STOP instruction

The return from stop is expected in reverse order:

1. On returning from Stop mode the clocks are automatically enabled coherently
2. Initialize and check device proper functionality (charge pump etc.)
3. Check functionality of the external system
4. Initializes control loop operation, however with PMF and GDU outputs still in safe state
5. Read the ADC values to check the system
6. Start driving energy into the system
   based on the measurements from the previous step, the PWM duty cycle values are calculated
7. PMF and GDU outputs are enabled (actively driven)

The device does not support putting the FETs in an active driving state during STOP as the GDU charge pump clock is not running. This means the device cannot be put in stop mode if the FETS need to be in an active driving state to protect the system from external energy supply (e.g. externally driven motor-generator).

**NOTE**

It is imperative, that whatever the modules perform on entering/exiting Stop mode, the pre-set complementary mode of operation and dead time insertion must be guaranteed all the times.

#### 1.13.3.11 Application Signal Visibility

In typical motor control applications, TIM OC0 is used internally to indicate commutation events. To switch off OC0 visibility at port pin PT0:

- Disable output compare signal on pin PT0 in TIM: OCPD[OCPD0]=0b1.

#### 1.13.3.12 Debug Signal Visibility

Depending on required visibility of internal signals on port pins enable the following registers:

- Set [PWMPRR]=0b1 in PIM if monitoring of internal PWM waveforms is needed. PWM0_[5:3] are driven out on pins PT[2:0] and PWM0_[2:0] on pins PP[2:0].
- Enable output compare channel OC0 to output commutation event on pin PT0 in TIM: OCPD[OCPD0]=0b0.
- Set PTUDEBUG[PTUREPE]=0b1 in PTU to output the reload event.
- Set PTUDEBUG[PTUTxPE]=0b1 with x=0,1 in PTU to output the trigger events.

### 1.13.4 BDCM Complementary Mode Operation

This section describes BDCM control using center aligned complementary mode with deadtime insertion.

**Table 2-6. Port S Pin Functions and Priorities**

| Port | Pin Name | ZVMC256 | ZVMC128\64 | ZVML128/64/32 | ZVML31 | ZVM32/16 | Pin Function & Priority[1] | I/O | Description | Routing Register Bit | Pin Function after Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | PS5 | | ✔ | ✔ | | | PDO | O | DBG profiling data output | — | GPIO |
| | | | ✔ | ✔ | ✔ | ✔ | $\overline{SS0}$ | I/O | SPI0 slave select | SPI0RR SPI0SSRR | |
| | | | ✔ | ✔ | ✔ | ✔ | PTS[5]/ KWS[5] | I/O | General-purpose; with interrupt and wakeup | — | |
| | PS4 | | ✔ | ✔ | | | PDOCLK | O | DBG profiling clock | — | |
| | | | ✔ | ✔ | ✔ | ✔ | SCK0 | I/O | SPI0 serial clock | SPI0RR | |
| | | | ✔ | ✔ | ✔ | ✔ | PTS[4]/ KWS[4] | I/O | General-purpose; with interrupt and wakeup | — | |
| | PS3 | ✔ | ✔ | ✔ | ✔ | ✔ | MOSI0 | I/O | SPI0 master out/slave in | SPI0RR | |
| | | ✔ | | | | | IOC1_1 | I/O | TIM1 channel 1 | — | |
| | | ✔ | | | | | (CPTXD0) | I | CANPHY0 transmit input | M0C0RR2-0 | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | (TXD1) | O | SCI1 transmit | SCI1RR | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | DBGEEV | I | DBG external event | — | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | PTS[3]/ KWS[3] | I/O | General-purpose; with interrupt and wakeup | — | |
| | PS2 | ✔ | ✔ | ✔ | ✔ | ✔ | MISO0 | I/O | SPI0 master in/slave out | SPI0RR | |
| | | ✔ | | | | | IOC1_0 | I/O | TIM1 channel 0 | — | |
| | | ✔ | | | | | (CPRXD0) | O | CANPHY0 receive output | M0C0RR2-0 | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | (RXD1) | I | SCI1 receive | SCI1RR | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | PTS[2]/ KWS[2] | I/O | General-purpose; with interrupt and wakeup | — | |
| | PS1 | ✔ | | | | | SCK0 | I/O | SPI0 serial clock | SPI0RR | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | PTUT1 | O | PTU trigger 1 | — | |
| | | ✔ | | | ✔ | ✔ | (IOC0_2) | I/O | TIM0 channel 2 | T0C2RR | |
| | | | | ✔ | ✔ | ✔ | (LPTXD0) | I | LINPHY0/HVPHY0 transmit input | S0L0RR2-0 | |
| | | ✔ | | | | | (CPDR1) | O | CANPHY0 direct control output CP0DR[CPDR1] | M0C0RR2-0 | |
| | | ✔ | ✔ | ✔ | | | TXCAN0[2] | O | MSCAN0 transmit | M0C0RR2-0 | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | TXD1 | O | SCI1 transmit | SCI1RR | |
| | | ✔ | ✔ | ✔ | ✔ | ✔ | PTS[1]/ KWS[1] | I/O | General-purpose; with interrupt and wakeup | — | |

| Global Address | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0338–0x0339 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x033A | PTABYPL[2] | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTABYPL0 |
| | | W | | | | | | | | |
| 0x033B | PTADIRL[2] | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTADIRL0 |
| | | W | | | | | | | | |
| 0x033C | DIENL[2] | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIENL0 |
| | | W | | | | | | | | |
| 0x033D | PTAENL[2] | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTAENL0 |
| | | W | | | | | | | | |
| 0x033E | PIRL[2] | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PIRL0 |
| | | W | | | | | | | | |
| 0x033F | PTTEL[2] | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTTEL0 |
| | | W | | | | | | | | |

1. Only available for ZVML128, ZVML64, ZVML32, and ZVML31
2. Only available for ZVMC256
3. PWMPRR[1] only writable for ZVMC256
4. Only available for ZVMC256, ZVML31, ZVM32, ZVM16
5. Not available for ZVMC256

## 2.3.2 PIM Registers 0x0200-0x020F

This section details the specific purposes of register implemented in address range 0x0200-0x020F. These registers serve for specific PIM related functions not part of the generic port registers.

- If not stated differently, writing to reserved bits has no effect and read returns zero.
- All register read accesses are synchronous to internal clocks.
- Register bits can be written at any time if not stated differently.

**Table 2-11. MODRR1 Routing Register Field Descriptions**

| Field | Description |
|---|---|
| 7-5<br>M0C0RR2-0 | **Module Routing Register** — MSCAN0-CANPHY0 routing<br>Selection of MSCAN0-CANPHY0 interface routing options to support probing and conformance testing. Refer to Figure 2-4 for an illustration and Table 2-12 for preferred settings. MSCAN0 must be enabled for TXCAN0 routing to take effect on pin. CANPHY0 must be enabled for CPRXD0 and CP0DR[CPDR1] routings to take effect on pins. |
| 4-3<br>PWMPRR1-0 | **Module Routing Register** — PMF probe<br><br>Internal PMF outputs can be probed on related external pins. Probing can be enabled independent of the PWM54RR, PWM32RR, and PWM10RR settings.<br><br>11 PMF channels 1, 3, 5 connected to related PWM1_x pins (only available for ZVMC256)<br>10 PMF channels 0, 2, 4 connected to related PWM1_x pins (only available for ZVMC256)<br>01 All PMF channels connected to related PWM1_x pins<br>00 No PMF channels connected to related PWM1_x pins |
| 2<br>PWM54RR | **Module Routing Register** — PWM1_4 and PWM1_5 routing<br><br>The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low.<br><br>1 PWM1_4 to PT1; PWM1_5 to PT2 (PP0 for S12ZVMC256)<br>0 PWM1_4 to GDU; PWM1_5 to GDU |
| 1<br>PWM32RR | **Module Routing Register** — PWM1_2 and PWM1_3 routing<br><br>The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low.<br><br>1 PWM1_2 to PP2 (PT3 for S12ZVMC256); PWM1_3 to PT0<br>0 PWM1_2 to GDU; PWM1_3 to GDU |
| 0<br>PWM10RR | **Module Routing Register** — PWM1_0 and PWM1_1 routing<br><br>The PWM channel pair can be configured for internal use with the GDU or with its related external pins only. If set the signal routing to the pins is established and the related GDU inputs are forced low.<br><br>1 PWM1_0 to PP0 (PT2 for S12ZVMC256); PWM1_1 to PP1<br>0 PWM1_0 to GDU; PWM1_1 to GDU |

### 2.3.4.8 Port L ADC Direct Register (PTADIRL)

Address 0x033B Access: User read/write[1]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PTADIRL0[2] |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-30. Port L ADC Direct Register (PTADIRL)**

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

**Table 2-34. PTADIRL Register Field Descriptions**

| Field | Description |
|---|---|
| 1-0<br>PTADIRL0 | **Port L ADC Direct Connection** —<br>This bit connects the analog input signal directly to the ADC channel bypassing the voltage divider. This bit takes effect only in analog mode (PTAENL=1).<br>1 Input pin directly connected to ADC channel<br>0 Input voltage divider active on analog input to ADC channel |

### 2.3.4.9 Port L Digital Input Enable Register (DIENL)

Address 0x33C Access: User read/write[1]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIENL0[2] |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-31. Port L Digital Input Enable Register (DIENL)**

1. Read: Anytime
   Write: Anytime
2. Only available for S12ZVMC256

**Table 2-35. DIENL Register Field Descriptions**

| Field | Description |
|---|---|
| 0<br>DIENL0 | **Digital Input Enable Port L** — Input buffer control<br>This bit controls the HVI digital input function. If set to 1 the input buffers are enabled and the pin can be used with the digital function. If the analog input function is enabled (PTAENL[PTAENL0]=1) the input buffer of the selected HVI pin is forced off[1] in run mode and is released to be active in stop mode only if DIENL=1.<br>1 Associated pin digital input is enabled if not used as analog input in run mode[1]<br>0 Associated pin digital input is disabled[1] |

1. Refer to PTTEL bit description in Section 2.3.4.11, “Port L Input Divider Ratio Selection Register (PIRL) for an override condition.

pointer is initialized by each aligned write to DBGTB to point to the oldest data again. This enables an interrupted trace buffer read sequence to be easily restarted from the oldest data entry. After reading all trace buffer lines, the next read wraps around and returns the contents of line0.

The least significant word of each 64-bit wide array line is read out first. All bytes, including those containing invalid information are read out.

#### 6.4.5.5 Trace Buffer Reset State

The trace buffer contents are not initialized by a system reset. Thus should a system reset occur, the trace session information from immediately before the reset occurred can be read out. The DBGCNT bits are not cleared by a system reset. Thus should a reset occur, the number of valid lines in the trace buffer is indicated by DBGCNT. The internal pointer is cleared by a system reset. It can be initialized by an aligned word write to DBGTB following a reset during debugging, so that it points to the oldest valid data again. Debugging occurrences of system resets is best handled using mid or end trigger alignment since the reset may occur before the trace trigger, which in the begin trigger alignment case means no information would be stored in the trace buffer.

### 6.4.6 Code Profiling

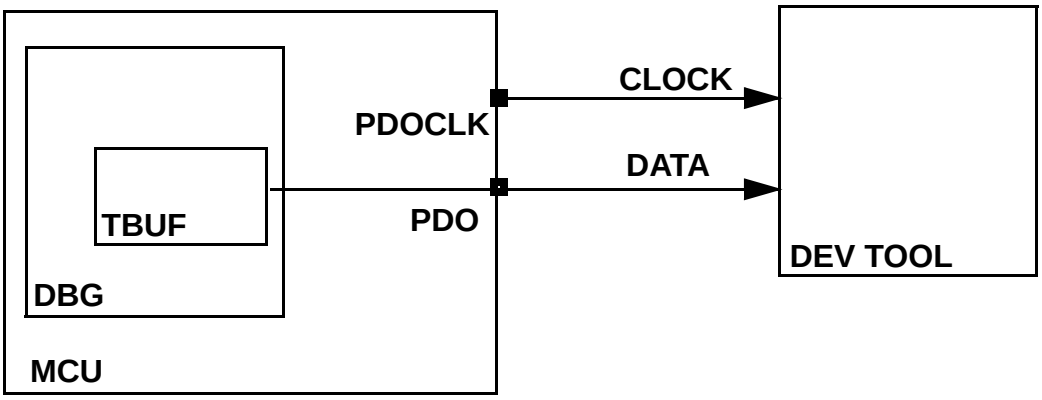
#### 6.4.6.1 Code Profiling Overview

Code profiling supplies encoded COF information on the PDO pin and the reference clock on the PDOCLK pin. If the TSOURCE bit is set then code profiling is enabled by setting the PROFILE bit. The associated device pin is configured for code profiling by setting the PDOE bit. Once enabled, code profiling is activated by arming the DBG. During profiling, if PDOE is set, the PDO operates as an output pin at a half the internal bus frequency, driving both high and low.

Independent of PDOE status, profiling data is stored to the trace buffer and can be read out in the usual manner when the debug session ends and the PTACT bit has been cleared.

The external debugger uses both edges of the clock output to strobe the data on PDO. The first PDOCLK edge is used to sample the first data bit on PDO.

**Figure 6-30. Profiling Output Interface**



### 8.3.2.17 Low Voltage Control Register (CPMULVCTL)

The CPMULVCTL register allows the configuration of the low-voltage detect features.

Module Base + 0x0011

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | VDDSIE(1) | LVDS | LVIE | LVIF |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | U | 0 | U |

The Reset state of LVDS and LVIF depends on the external supplied VDDA level

= Unimplemented or Reserved

**Figure 8-23. Low Voltage Control Register (CPMULVCTL)**

1. Only available in V10

Read: Anytime

Write: LVIE and LVIF are write anytime, LVDS is read only

**Table 8-18. CPMULVCTL Field Descriptions**

| Field | Description |
|---|---|
| 3<br>VDDSIE | VDDS Integrity Interrupt Enable Bit<br>0 Interrupt request is disabled.<br>1 Interrupt will be requested on VDDS integrity fails, that means whenever one of the following flags in CPMUVDDS register is set: SCS2IF, SCS1IF, LVS2IF, LVS1IF. |
| 2<br>LVDS | **Low-Voltage Detect Status Bit** — This read-only status bit reflects the voltage level on VDDA. Writes have no effect.<br>0 Input voltage VDDA is above level $V_{LVID}$ or RPM.<br>1 Input voltage VDDA is below level $V_{LVIA}$ and FPM. |
| 1<br>LVIE | Low-Voltage Interrupt Enable Bit<br>0 Interrupt request is disabled.<br>1 Interrupt will be requested whenever LVIF is set. |
| 0<br>LVIF | **Low-Voltage Interrupt Flag** — LVIF is set to 1 when LVDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (LVIE = 1), LVIF causes an interrupt request.<br>0 No change in LVDS bit.<br>1 LVDS bit has changed. |

### 8.5.4 PLL Clock Monitor Reset

In case of loss of PLL clock oscillation or the PLL clock frequency is below the failure assert frequency $f_{PMFA}$ (see device electrical characteristics for values), the S12CPMU_UHV_V10_V6 generates a PLL Clock Monitor Reset. In Full Stop Mode the PLL and the PLL clock monitor are disabled.

### 8.5.5 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus COP reset is generated.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit.

Depending on the COP configuration there might be a significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

Table 8-36 gives an overview of the COP condition (run, static) in Stop Mode depending on legal configuration and status bit settings:

**Table 8-36. COP condition (run, static) in Stop Mode**

| COPOSCSEL1 | CSAD | PSTP | PCE | COPOSCSEL0 | OSCE | UPOSC | COP counter behavior in Stop Mode (clock source) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | x | x | x | x | x | Run (ACLK) |
| 1 | 1 | x | x | x | x | x | Static (ACLK) |
| 0 | x | 1 | 1 | 1 | 1 | 1 | Run (OSCCLK) |
| 0 | x | 1 | 1 | 0 | 0 | x | Static (IRCCLK) |
| 0 | x | 1 | 1 | 0 | 1 | x | Static (IRCCLK) |
| 0 | x | 1 | 0 | 0 | x | x | Static (IRCCLK) |
| 0 | x | 1 | 0 | 1 | 1 | 1 | Static (OSCCLK) |
| 0 | x | 0 | 1 | 1 | 1 | 1 | Static (OSCCLK) |
| 0 | x | 0 | 1 | 0 | 1 | x | Static (IRCCLK) |
| 0 | x | 0 | 1 | 0 | 0 | 0 | Static (IRCCLK) |
| 0 | x | 0 | 0 | 1 | 1 | 1 | Satic (OSCCLK) |
| 0 | x | 0 | 0 | 0 | 1 | 1 | Static (IRCCLK) |
| 0 | x | 0 | 0 | 0 | 1 | 0 | Static (IRCCLK) |
| 0 | x | 0 | 0 | 0 | 0 | 0 | Static (IRCCLK) |

### 9.5.2.5 ADC Format Register (ADCFMT)

Module Base + 0x0004

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | DJM | 0 | 0 | 0 | 0 | SRES[2:0] | | |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 9-8. ADC Format Register (ADCFMT)**

Read: Anytime

Write: Bits DJM and SRES[2:0] are writable if bit ADC_EN clear or bit SMOD_ACC set

**Table 9-8. ADCFMT Field Descriptions**

| Field | Description |
|---|---|
| 7<br>DJM | **Result Register Data Justification** — Conversion result data format is always unsigned. This bit controls justification of conversion result data in the conversion result list.<br>0 Left justified data in the conversion result list.<br>1 Right justified data in the conversion result list. |
| 2-0<br>SRES[2:0] | **ADC Resolution Select** — These bits select the resolution of conversion results. See Table 9-9 for coding. |

**Table 9-9. Selectable Conversion Resolution**

| SRES[2] | SRES[1] | SRES[0] | ADC Resolution |
|---|---|---|---|
| 0 | 0 | 0 | 8-bit data |
| 0 | 0 | 1 | Reserved[1.] |
| 0 | 1 | 0 | 10-bit data |
| 0 | 1 | 1 | Reserved[1.] |
| 1 | 0 | 0 | 12-bit data |
| 1 | x | x | Reserved[(1)] |

1. Reserved settings cause a severe error at ADC conversion start whereby the CMD_EIF flag is set and ADC ceases operation

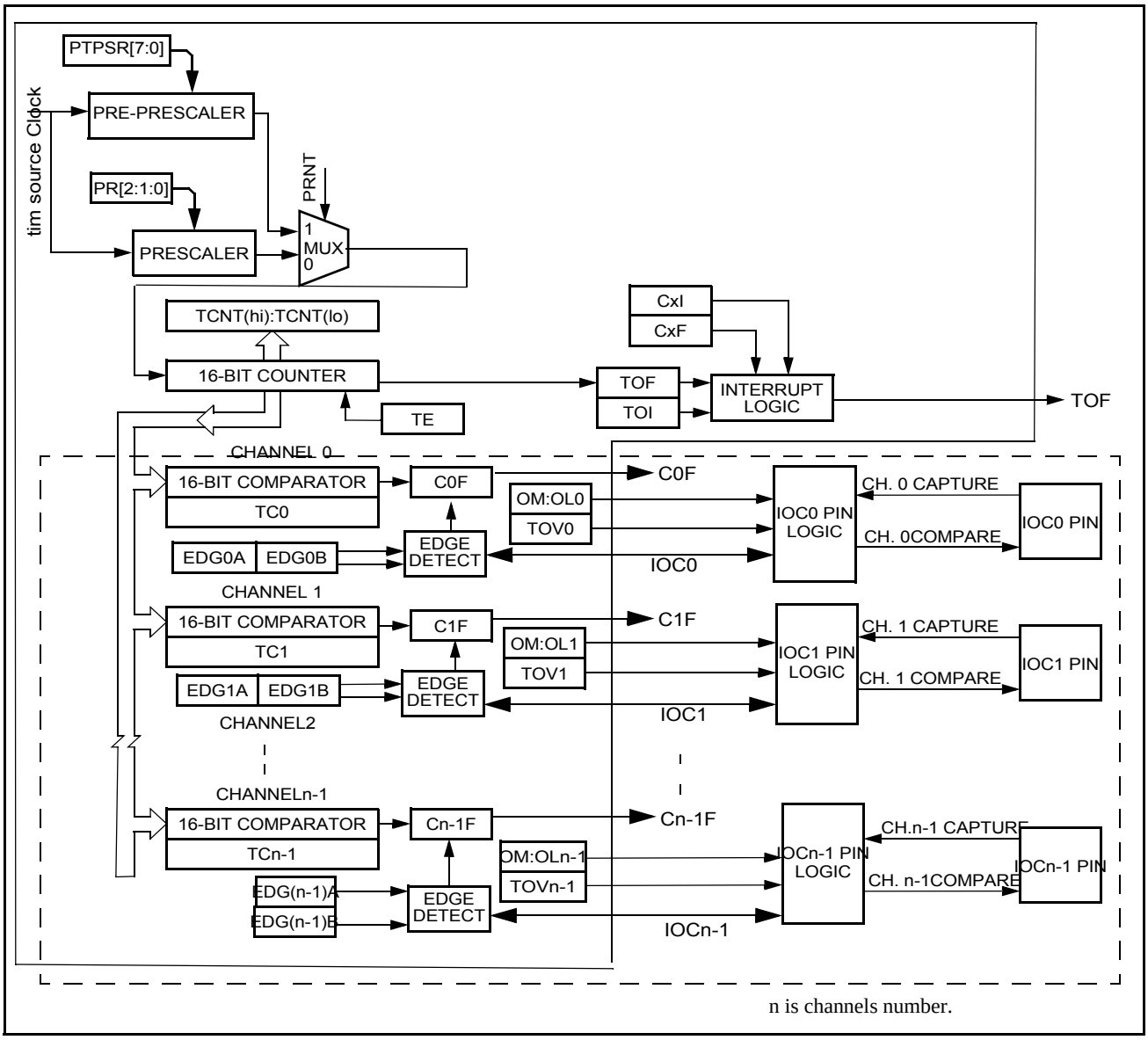



**Figure 12-22. Detailed Timer Block Diagram**

## 12.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

### 14.3.2.14 PTU Pointer Register (PTUPTRH, PTUPTRM, PTUPTRL)

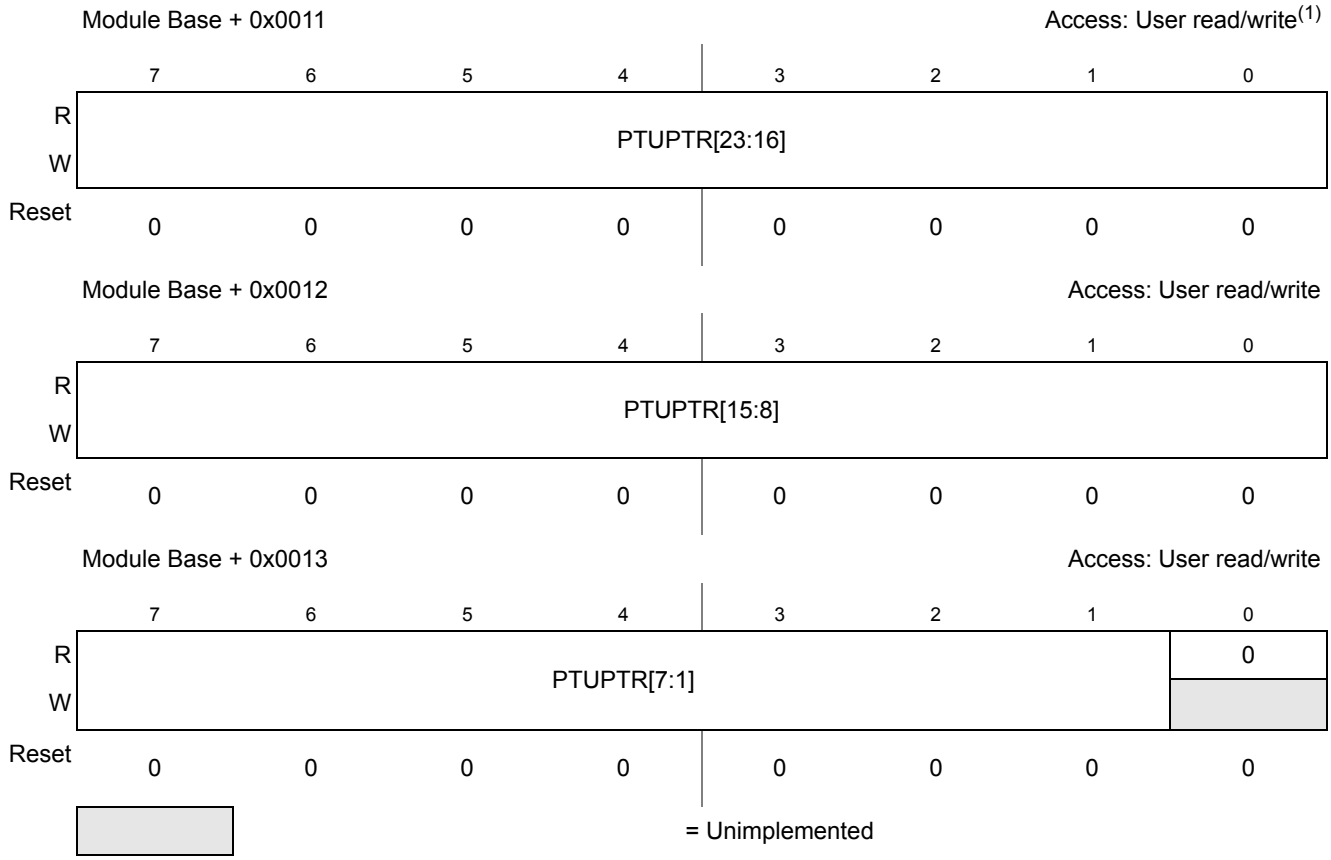



**Figure 14-16. PTU List Add Register (PTUPTRH, PTUPTRM, PTUPTRL)**

1. Read: Anytime
   Write: Anytime, if TG0En and TG1EN bit are cleared

**Table 14-16. PTUPTR Register Field Descriptions**

| Field | Description |
|---|---|
| PTUPTR [23:0] | PTU Pointer — This register cannot be modified if TG0EN or TG1EN bit is set. This register defines the start address of the used list area inside the global memory map. For more information see Section 14.4.2, “Memory based trigger event list”. |

mechanism” above. The only difference is, that during an async reload event the error interrupt flags PTUROIF and TGxREIF are not generated.

## 14.4.5 Interrupts and error handling

This section describes the interrupts generated by the PTU module and their individual sources, Vector addresses and interrupt priority are defined by MCU level.

**Table 14-22. PTU Interrupt Sources**

| Module Interrupt Sources | Local Enable |
|---|---|
| PTU Reload Overrun Error | PTUIEH[PTUROIE] |
| TG0 Error | PTUIEL[TG0AEIE,TG0REIE,TG0TEIE] |
| TG1 Error | PTUIEL[TG1AEIE,TG1REIE,TG1TEIE] |
| TG0 Done | PTUIEL[TG0DIE] |
| TG1 Done | PTUIEL[TG1DIE] |

### 14.4.5.1 PTU Double Bit ECC Error

If one trigger generator reads trigger values from the memory which contains double bit ECC errors then the PTUDEEF is set. These read data are ignored and the execution of both trigger generators is stopped until the PTUDEEF flag was cleared. To make sure the trigger generator starts in a define state it is required to execute follow sequence:

1. disable both trigger generators
2. configure the PTU if required
3. clear the PTUDEEF
4. enable the desired trigger generators

### 14.4.5.2 PTU Reload Overrun Error

If the PTULDOK bit is not set during the reload event then the PTUROIF bit is set. If enabled (PTUROIE is set) an interrupt is generated. For more information see Section 14.4.3, “Reload mechanism”. During an async reload event the PTUROIF interrupt flag is not set.

### 14.4.5.3 Trigger Generator Memory Access Error

The trigger generator memory access error flag (TGxAEIF) is set if the used read address is outside the accessible memory address area; see the MMC section for the supported memory area. The loaded trigger values are ignored and the execution of this trigger list is stopped until the next reload event. If enabled (TGxAEIE is set) an interrupt will be generated.

### 14.4.5.4 Trigger Generator Reload Error

The trigger generator reload error flag (TGxREIF) is set if a new reload event occurs before the trigger generator reaches the EOL symbol or the maximum number of generated triggers. Independent of this

**Table 15-4. Modes When PWM Operation is Restricted**

| Mode | Description |
|---|---|
| STOP | PWM outputs are disabled |
| WAIT | PWM outputs are disabled as a function of the PMFWAI bit |
| FREEZE | PWM outputs are disabled as a function of the PMFFRZ bit |

### 16.3.2.4 SCI Alternative Control Register 1 (SCIACR1)

Module Base + 0x0001

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | RXEDGIE | 0 | 0 | 0 | 0 | 0 | BERRIE | BKDIE |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 16-7. SCI Alternative Control Register 1 (SCIACR1)**

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

**Table 16-6. SCIACR1 Field Descriptions**

| Field | Description |
|---|---|
| 7<br>RXEDGIE | **Receive Input Active Edge Interrupt Enable** — RXEDGIE enables the receive input active edge interrupt flag, RXEDGIF, to generate interrupt requests.<br>0 RXEDGIF interrupt requests disabled<br>1 RXEDGIF interrupt requests enabled |
| 1<br>BERRIE | **Bit Error Interrupt Enable** — BERRIE enables the bit error interrupt flag, BERRIF, to generate interrupt requests.<br>0 BERRIF interrupt requests disabled<br>1 BERRIF interrupt requests enabled |
| 0<br>BKDIE | **Break Detect Interrupt Enable** — BKDIE enables the break detect interrupt flag, BKDIF, to generate interrupt requests.<br>0 BKDIF interrupt requests disabled<br>1 BKDIF interrupt requests enabled |

**Table 16-11. SCISR1 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 3<br>OR | **Overrun Flag** — OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL).<br>0 No overrun<br>1 Overrun<br>**Note:** OR flag may read back as set when RDRF flag is clear. This may happen if the following sequence of events occurs:<br>1. After the first frame is received, read status register SCISR1 (returns RDRF set and OR flag clear);<br>2. Receive second frame without reading the first frame in the data register (the second frame is not received and OR flag is set);<br>3. Read data register SCIDRL (returns first frame and clears RDRF flag in the status register);<br>4. Read status register SCISR1 (returns RDRF clear and OR set).<br>Event 3 may be at exactly the same time as event 2 or any time after. When this happens, a dummy SCIDRL read following event 4 will be required to clear the OR flag if further frames are to be received. |
| 2<br>NF | **Noise Flag** — NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL).<br>0 No noise<br>1 Noise |
| 1<br>FE | **Framing Error Flag** — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL).<br>0 No framing error<br>1 Framing error |
| 0<br>PF | **Parity Error Flag** — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL).<br>0 No parity error<br>1 Parity error |

### 18.3.2.17 GDU Control Register 1 (GDUCTR1)

Module Base + 0x0010 Access: User read/write(1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | GSRMOD1 | GSRMOD0 | 0 | 0 | 0 | 0 | 0 | TDEL |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented

**Figure 18-19. GDU Control Register 1 (GDUCTR1)**

1. Read: Anytime
   Write: Only if GWP=0

**Table 18-21. GDUCTR1 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>GSRMOD1 | GDU Switched Reluctance Motor Mode 1 — This bit cannot be modified after GWP bit is set. This bit controls the routing of the LDx pins to the low-side desaturation comparators for switched reluctance motor. See Figure 18-23<br>0 HSx routed to low-side desaturation comparator<br>1 LDx routed to low-side desaturation comparator |
| 6<br>GSRMOD0 | GDU Switched Reluctance Motor Mode 0 — This bit cannot be modified after GWP bit is set.<br>0 BLDC mode. Don't allow HGx and LGx high at the same time.<br>1 SR mode. Allow HGx and LGx high at the same time. |
| 0<br>TDEL | **$t_{delon}$ / $t_{deloff}$ Control** — This bit controls the parameters $t_{delon}$ and $t_{deloff}$. It cannot be modified after GWP bit is set. This bit must be set to meet the min and max values for $t_{delon}$ and $t_{deloff}$ specified in the electrical specification. If this bit is cleared the values for $t_{delon}$ and $t_{deloff}$ are out of spec. |

**NOTE**

GDU Control Register 1 GDUCTR1 availability is defined at device level.

### 20.4.5.3 Valid Flash Module Commands

Table 20-29 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

**Table 20-29. Flash Commands by Mode and Security State**

| FCMD | Command | Unsecured | | Secured | |
|---|---|---|---|---|---|
| | | NS (1) | SS(2) | NS (3) | SS(4) |
| 0x01 | Erase Verify All Blocks | * | * | * | * |
| 0x02 | Erase Verify Block | * | * | * | * |
| 0x03 | Erase Verify P-Flash Section | * | * | * | |
| 0x04 | Read Once | * | * | * | |
| 0x06 | Program P-Flash | * | * | * | |
| 0x07 | Program Once | * | * | * | |
| 0x08 | Erase All Blocks | | * | | * |
| 0x09 | Erase Flash Block | * | * | * | |
| 0x0A | Erase P-Flash Sector | * | * | * | |
| 0x0B | Unsecure Flash | | * | | * |
| 0x0C | Verify Backdoor Access Key | * | | * | |
| 0x0D | Set User Margin Level | * | * | * | |
| 0x0E | Set Field Margin Level | | * | | |
| 0x10 | Erase Verify EEPROM Section | * | * | * | |
| 0x11 | Program EEPROM | * | * | * | |
| 0x12 | Erase EEPROM Sector | * | * | * | |
| 0x13 | Protection Override | * | * | * | * |

1. Unsecured Normal Single Chip mode

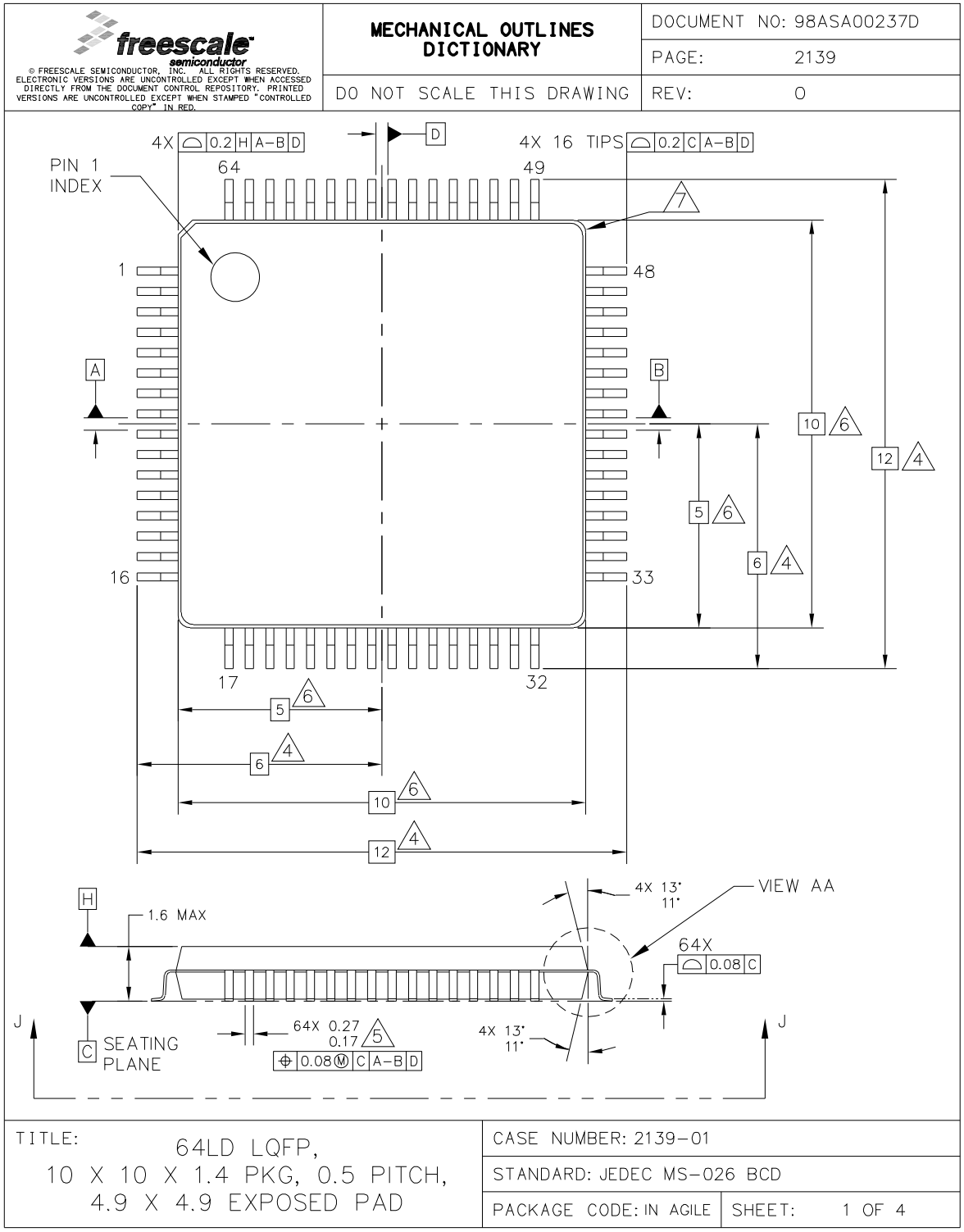
2. Unsecured Special Single Chip mode.

3. Secured Normal Single Chip mode.

4. Secured Special Single Chip mode.

# K.3 64LQFP-EP Mechanical Information (mask sets 1N95G, 2N95G)

**Figure K-3. 64LQFP-EP Mechanical Information (mask sets 1N95G, 2N95G)**



# M.12 0x05C0-0x05FF TIM0

| Address | Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x05D2 | TIM0TC1H | R<br>W | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
| 0x05D3 | TIM0TC1L | R<br>W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x05D4 | TIM0TC2H | R<br>W | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
| 0x05D5 | TIM0TC2L | R<br>W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x05D6 | TIM0TC3H | R<br>W | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
| 0x05D7 | TIM0TC3L | R<br>W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x05D8–<br>0x05DF | Reserved | R<br>W | | | | | | | | |
| 0x05E0 | Reserved | R<br>W | | | | | | | | |
| 0x05E1 | Reserved | R<br>W | | | | | | | | |
| 0x05E2 | Reserved | R<br>W | | | | | | | | |
| 0x05E3 | Reserved | R<br>W | | | | | | | | |
| 0x05E4–<br>0x05EB | Reserved | R<br>W | | | | | | | | |
| 0x05EC | TIM0OCPD | R<br>W | | | | | OCPD3 | OCPD2 | OCPD1 | OCPD0 |
| 0x05ED | Reserved | R<br>W | | | | | | | | |
| 0x05EE | TIM0PTPSR | R<br>W | PTPS7 | PTPS6 | PTPS5 | PTPS4 | PTPS3 | PTPS2 | PTPS1 | PTPS0 |
| 0x05EF | Reserved | R<br>W | | | | | | | | |