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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	71
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke06z64vlk4

Field	Description	Values
		• QH = 64 QFP (14 mm x 14 mm) • LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MKE06Z128VLK4

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 (64-pin and 80-pin packages only), and PTH1 (64-pin and 80-pin packages only) support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold—high range (LVDV = 1)[2]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVW1L}	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

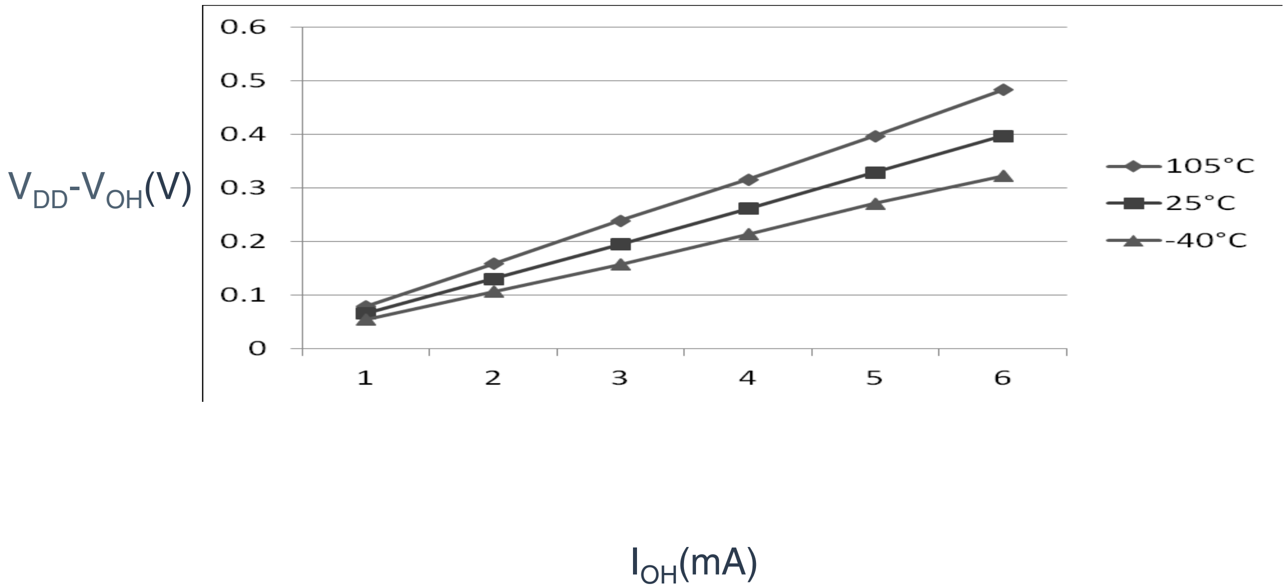


Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

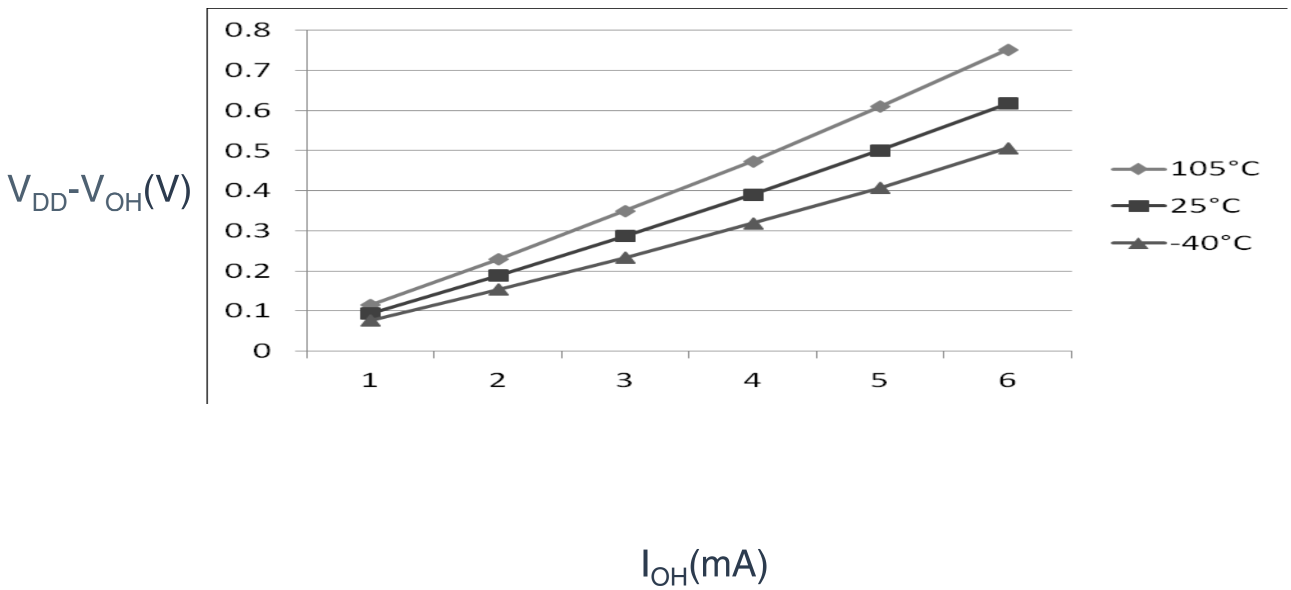


Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

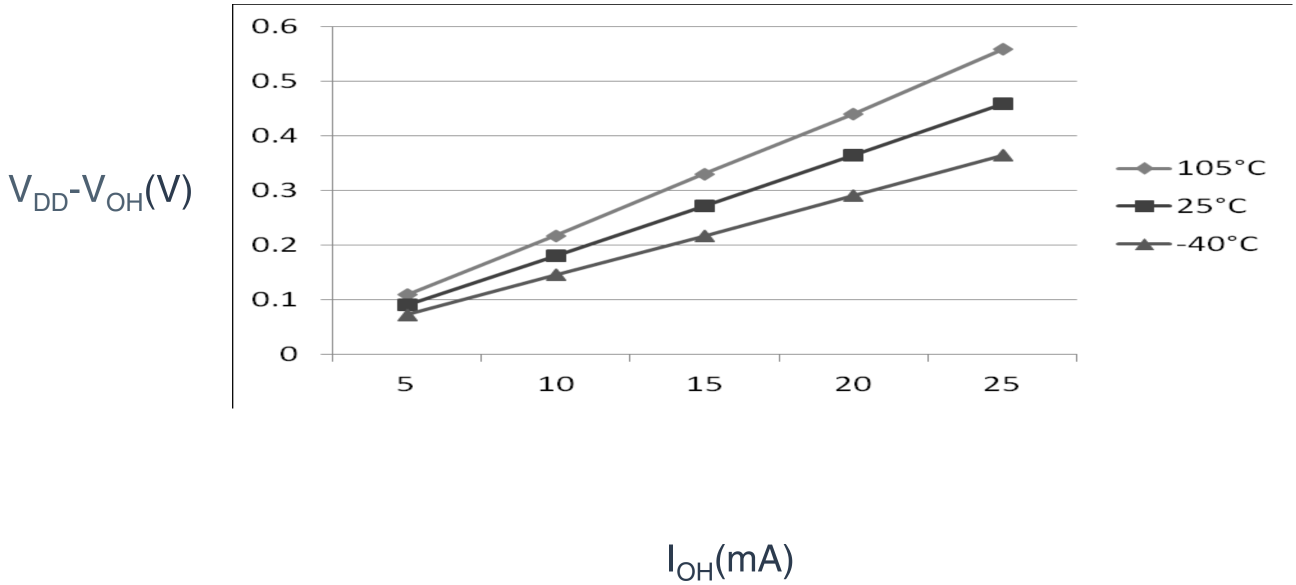


Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

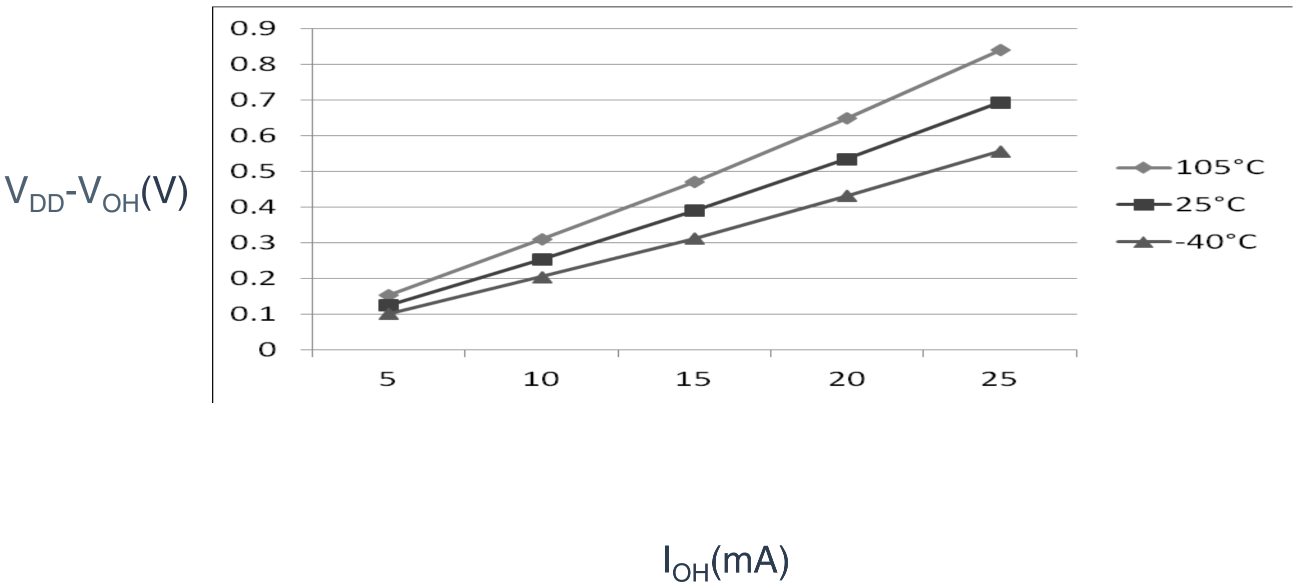


Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

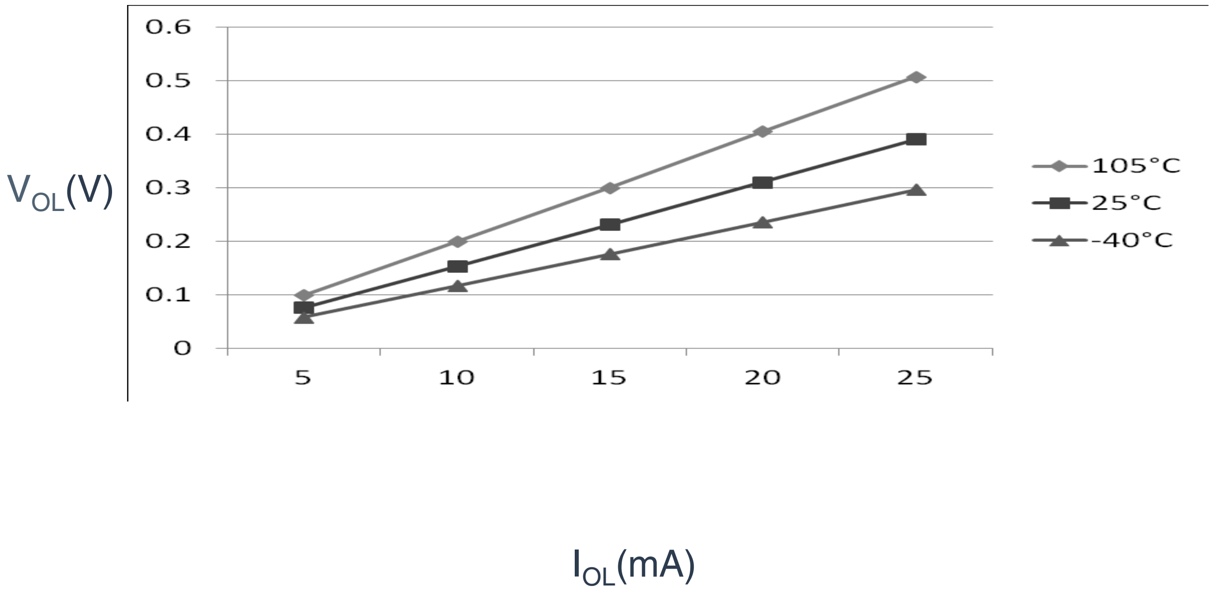


Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 5 V)

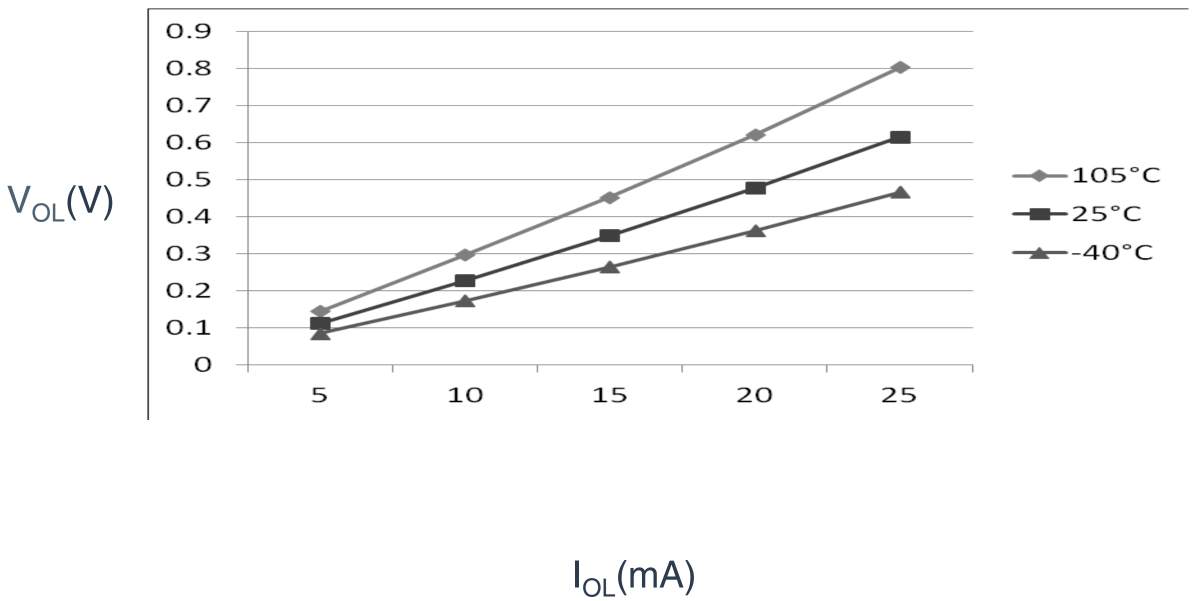


Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

Table 5. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	48/24 MHz	5	8.4	—	mA	-40 to 105 °C
P			24/24 MHz		6.5	7.2		
C			12/12 MHz		4.3	—		
C			1/1 MHz		2.4	—		
C			48/24 MHz	3	8.3	—		
P			24/24 MHz		6.4	7		
C			12/12 MHz		4.2	—		
C			1/1 MHz		2.3	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	105	μA	-40 to 105 °C
P			—	3	1.9	95		-40 to 105 °C
C	ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	86	—	μA	-40 to 105 °C
C				3	82	—		
C	ACMP adder to Stop	—	—	5	12	—	μA	-40 to 105 °C
C				3	12	—		
C	LVD adder to Stop[4]	—	—	5	130	—	μA	-40 to 105 °C
C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The Max current is observed at high temperature of 105 °C.
3. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following applications notes, available on **nxp.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

Table 8. FTM input timing (continued)

C	Function	Symbol	Min	Max	Unit
D	External clock period	t_{TCLK}	4	—	t_{Timer}, [1]
D	External clock high time	t_{clkh}	1.5	—	t_{Timer}[1]
D	External clock low time	t_{clkl}	1.5	—	t_{Timer}[1]
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{Timer}[1]

1. $t_{Timer} = 1/f_{Timer}$

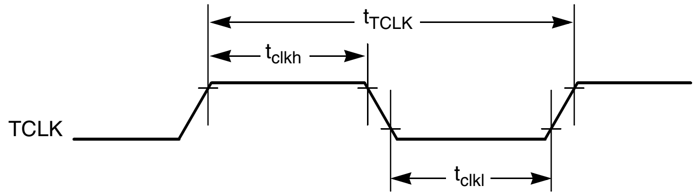


Figure 11. Timer external clock

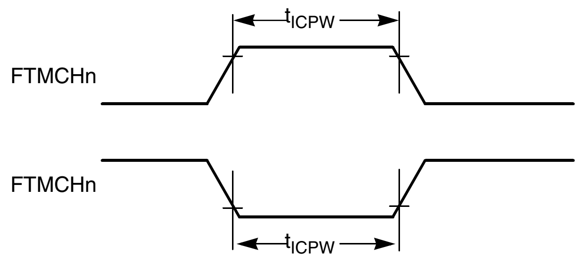


Figure 12. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA}$ x chip power dissipation

5.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal attributes

Board type	Symbol	Description	64 LQFP	64 QFP	44 LQFP	80 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	61	75	57	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	47	53	44	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	50	62	47	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	41	47	38	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	28	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	20	15	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	5	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns

Table continues on the next page...

Table 11. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

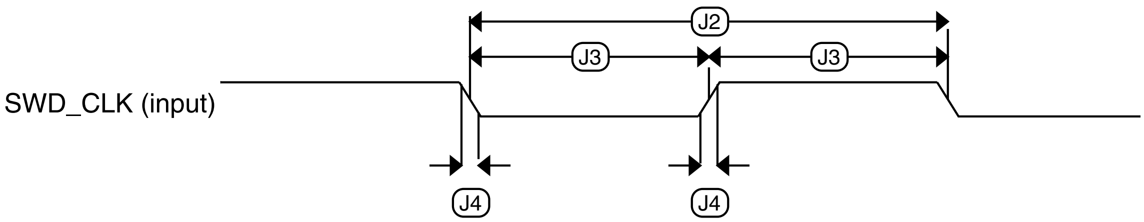


Figure 13. Serial wire clock input timing

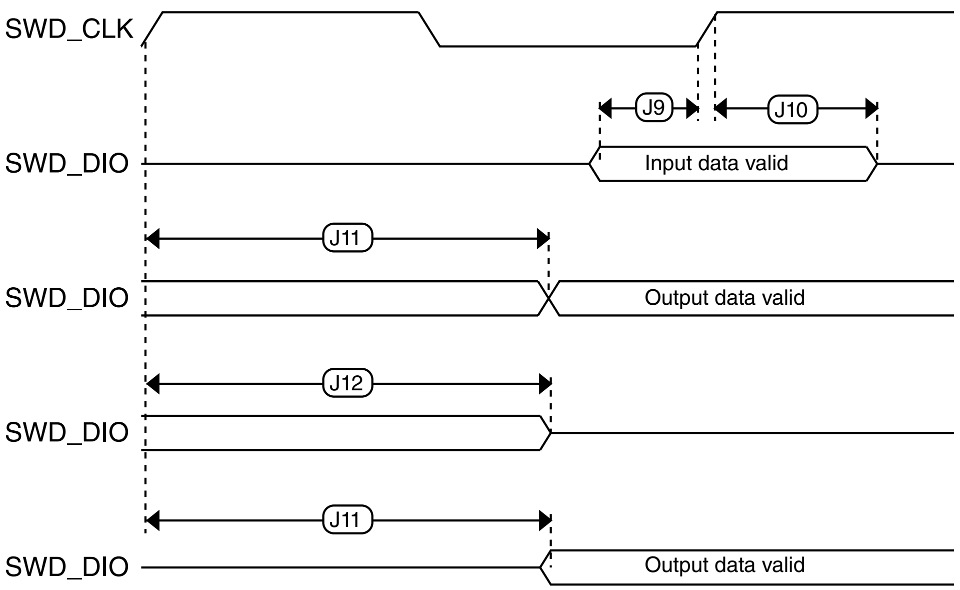


Figure 14. Serial wire data timing

6.2 External oscillator (OSC) and ICS characteristics

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1)	f_{hi}	4	—	24	MHz

Table continues on the next page...

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
2	D	Load capacitors		C1, C2	See Note[2]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	P	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	37.5	—	kHz
10	P	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	40	—	50	MHz
11	P	Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 105°C	Δf_{int_t}	-1	—	0.5	%
			Over temperature range from 0 °C to 105°C	Δf_{int_t}	-0.5	—	0.5	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105°C	Δf_{dco_ft}	-1.5	—	1	%
			Over temperature range from 0 °C to 105°C	Δf_{dco_ft}	-1	—	1	

Table continues on the next page...

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
14	C	FLL acquisition time[4,6]	$t_{Acquire}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

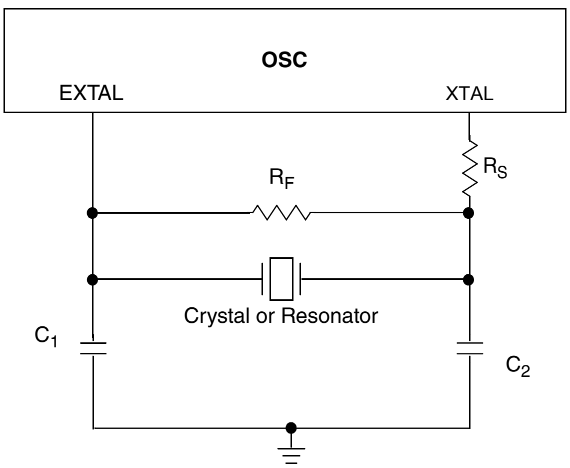


Figure 15. Typical crystal or resonator circuit

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 13. Flash characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase –40 °C to 105 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V

Table continues on the next page...

Table 13. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	24	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	2605	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	2579	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	485	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	464	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.13	0.31	ms
D	Program Flash (4 word)	t_{PGM4}	0.21	0.21	0.49	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Erase All Blocks	t_{ERSALL}	95.42	100.18	100.30	ms
D	Erase Flash Block	t_{ERSBLK}	95.42	100.18	100.30	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.09	ms
D	Unsecure Flash	t_{UNSECU}	95.42	100.19	100.31	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	415	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

6.4 Analog

6.4.1 ADC characteristics

Table 14. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Reference potential	• Low • High	V_{REFL} V_{REFH}	V_{SSA} $V_{DDA}/2$	— —	$V_{DDA}/2$ V_{DDA}	V	—

Table continues on the next page...

Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	12-bit mode	C	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode	C		—	±1.5	—	
	8-bit mode	C		—	±0.8	—	
Differential Non-Liniarity	12-bit mode	C	DNL	—	±1.5	—	LSB[3]
	10-bit mode	C		—	±0.4	—	
	8-bit mode	C		—	±0.15	—	
Integral Non-Linearity	12-bit mode	C	INL	—	±1.5	—	LSB[3]
	10-bit mode	C		—	±0.4	—	
	8-bit mode	C		—	±0.15	—	
Zero-scale error[4]	12-bit mode	C	E_{ZS}	—	±1.0	—	LSB[3]
	10-bit mode	C		—	±0.2	—	

Table continues on the next page...

Table 15. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
	8-bit mode	C		—	±0.35	—	
Full-scale error[5]	12-bit mode	C	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode	C		—	±0.3	—	
	8-bit mode	C		—	±0.25	—	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[6]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. V_{ADIN} = V_{SSA}
5. V_{ADIN} = V_{DDA}
6. I_{In} = leakage current (refer to DC characteristics)

6.4.2 Analog comparator (ACMP) electricals

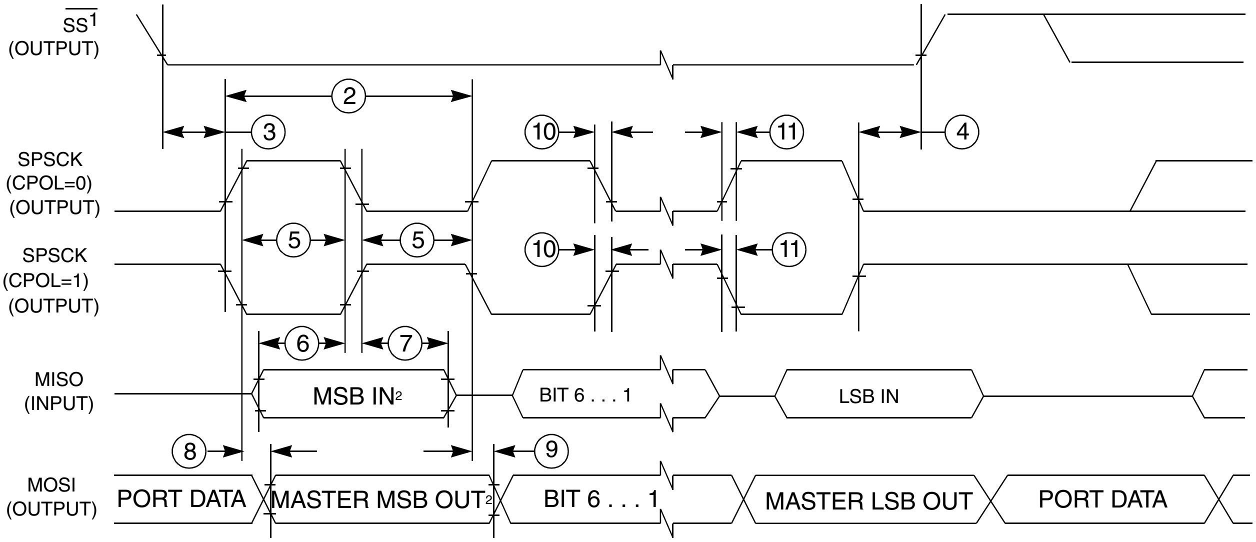
Table 16. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

6.5 Communication interfaces

6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 18. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in Control timing.
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

80 LQFP	64 LQFP /QFP	44 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	1	PTD1	DISABLED	PTD1	KBI0_P25	FTM2_CH3	SPI1_MOSI				
2	2	2	PTD0	DISABLED	PTD0	KBI0_P24	FTM2_CH2	SPI1_SCK				
3	3	—	PTH7	DISABLED	PTH7	KBI1_P31	PWT_IN1					
4	4	—	PTH6	DISABLED	PTH6	KBI1_P30						
5	—	—	PTH5	DISABLED	PTH5	KBI1_P29						
6	5	3	PTE7	DISABLED	PTE7	KBI1_P7	TCLK2		FTM1_CH1	CAN0_TX		
7	6	4	PTH2	DISABLED	PTH2	KBI1_P26	BUSOUT		FTM1_CH0	CAN0_RX		
8	7	5	VDD	VDD							VDD	
9	8	6	VDDA	VDDA						VREFH	VDDA	
10	—	—	VREFH	VREFH							VREFH	
11	9	7	VREFL	VREFL							VREFL	
12	10	8	VSS/ VSSA	VSS/ VSSA						VSSA	VSS	
13	11	9	PTB7	EXTAL	PTB7	KBI0_P15	I2C0_SCL				EXTAL	
14	12	10	PTB6	XTAL	PTB6	KBI0_P14	I2C0_SDA				XTAL	
15	13	11	PTI4	DISABLED	PTI4		IRQ					
16	—	—	PTI1	DISABLED	PTI1		IRQ	UART2_TX				
17	—	—	PTI0	DISABLED	PTI0		IRQ	UART2_RX				
18	14	—	PTH1	DISABLED	PTH1	KBI1_P25	FTM2_CH1					
19	15	—	PTH0	DISABLED	PTH0	KBI1_P24	FTM2_CH0					
20	16	—	PTE6	DISABLED	PTE6	KBI1_P6						
21	17	—	PTE5	DISABLED	PTE5	KBI1_P5						
22	18	12	PTB5	DISABLED	PTB5	KBI0_P13	FTM2_CH5	SPI0_PCS	ACMP1_OUT			
23	19	13	PTB4	NMI_b	PTB4	KBI0_P12	FTM2_CH4	SPI0_MISO	ACMP1_IN2	NMI_b		
24	20	14	PTC3	ADC0_SE11	PTC3	KBI0_P19	FTM2_CH3		ADC0_SE11			
25	21	15	PTC2	ADC0_SE10	PTC2	KBI0_P18	FTM2_CH2		ADC0_SE10			
26	22	16	PTD7	DISABLED	PTD7	KBI0_P31	UART2_TX					
27	23	17	PTD6	DISABLED	PTD6	KBI0_P30	UART2_RX					
28	24	18	PTD5	DISABLED	PTD5	KBI0_P29	PWT_IN0					
29	—	—	PTI6	DISABLED	PTI6	IRQ						
30	—	—	PTI5	DISABLED	PTI5	IRQ						
31	25	19	PTC1	ADC0_SE9	PTC1	KBI0_P17	FTM2_CH1		ADC0_SE9			
32	26	20	PTC0	ADC0_SE8	PTC0	KBI0_P16	FTM2_CH0		ADC0_SE8			
33	—	—	PTH4	DISABLED	PTH4	KBI1_P28	I2C1_SCL					
34	—	—	PTH3	DISABLED	PTH3	KBI1_P27	I2C1_SDA					
35	27	—	PTF7	ADC0_SE15	PTF7	KBI1_P15			ADC0_SE15			
36	28	—	PTF6	ADC0_SE14	PTF6	KBI1_P14			ADC0_SE14			
37	29	—	PTF5	ADC0_SE13	PTF5	KBI1_P13			ADC0_SE13			
38	30	—	PTF4	ADC0_SE12	PTF4	KBI1_P12			ADC0_SE12			
39	31	21	PTB3	ADC0_SE7	PTB3	KBI0_P11	SPI0_MOSI	FTM0_CH1	ADC0_SE7			
40	32	22	PTB2	ADC0_SE6	PTB2	KBI0_P10	SPI0_SCK	FTM0_CH0	ADC0_SE6			

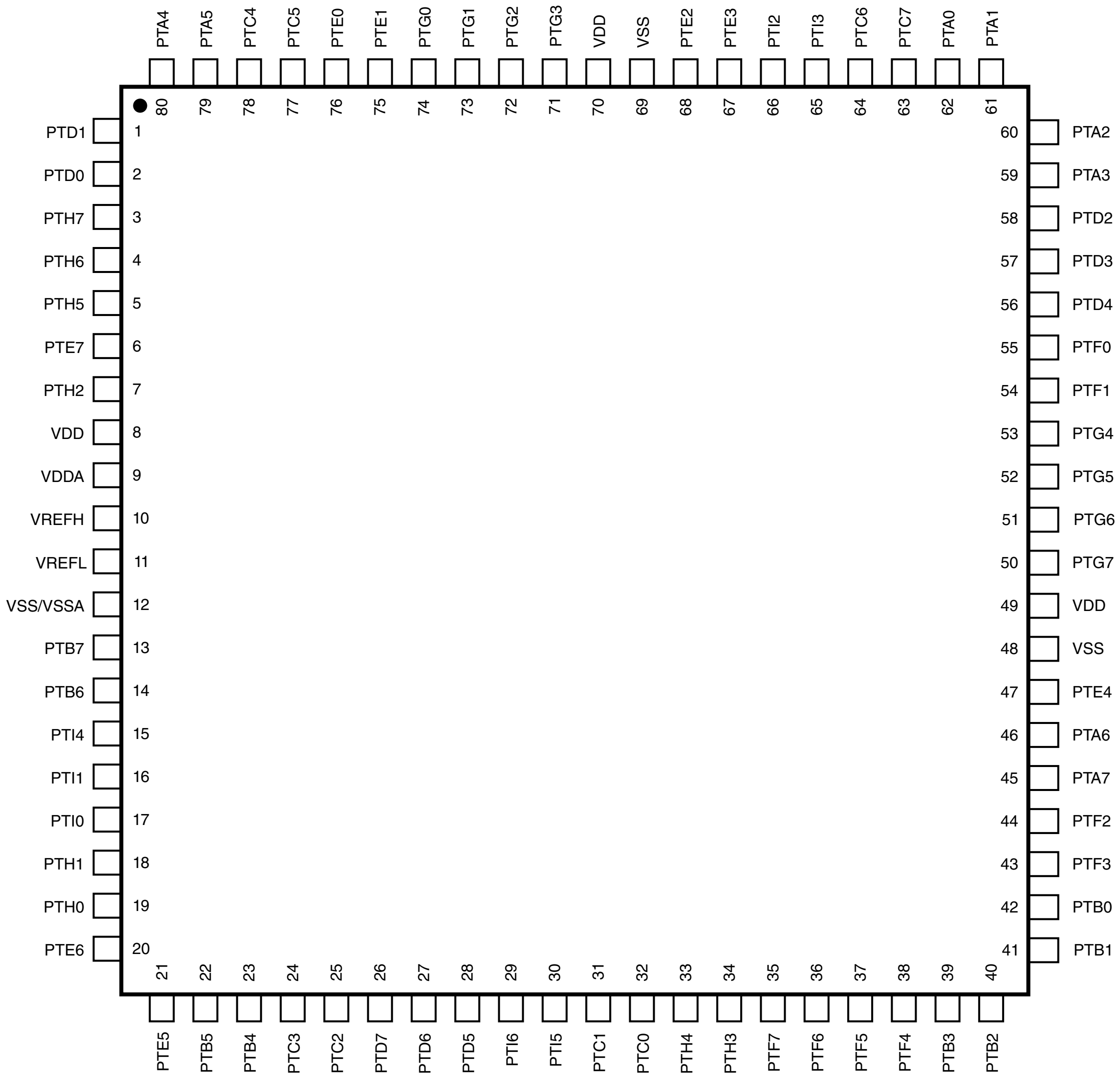


Figure 21. 80-pin LQFP package

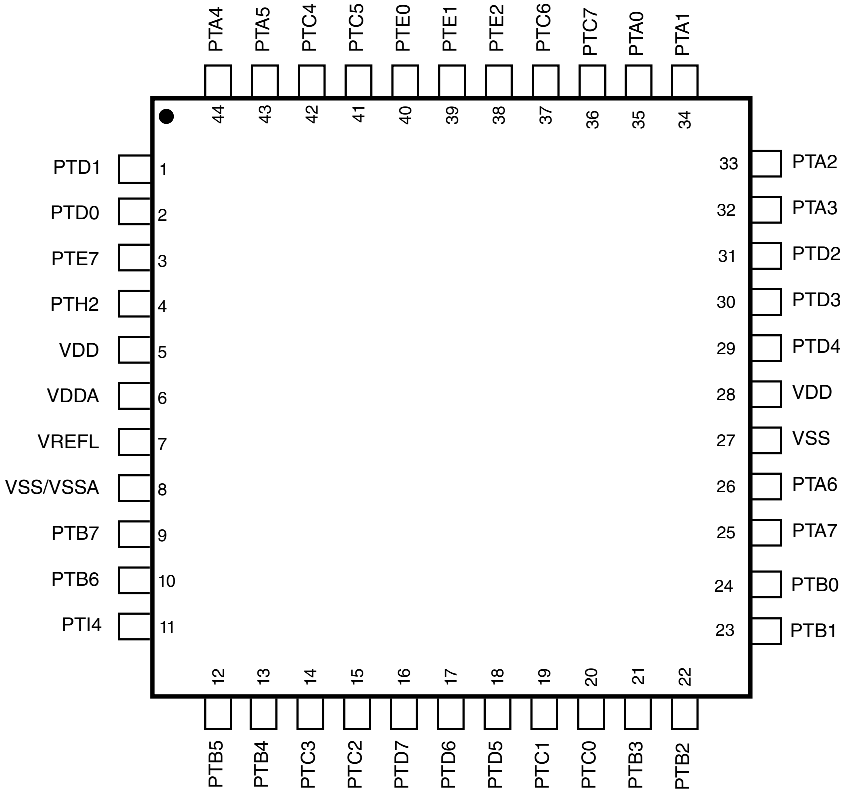


Figure 23. 44-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
1	12/2013	Initial NDA release.
2	3/2014	Initial public release.
3	5/2014	• Updated the Max. of SI_{DD}. • Updated footnote to the V_{OH}. • Corrected Unit in the FTM input timing table.
4	07/2016	• Added a new section of Thermal operating requirements. • Corrected pinout diagram for 44-pin LQFP in the Device pin assignment.