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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g222f128-qfp48

2. Ordering Information

The following table shows the available EFM32G devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32G200F16G-E-QFN32	16	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F32G-E-QFN32	32	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F64G-E-QFN32	64	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G210F128G-E-QFN32	128	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G222F32G-E-QFP48	32	8	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F64G-E-QFP48	64	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F128G-E-QFP48	128	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G230F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G232F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G280F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G290F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G840F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G842F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G880F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G890F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112

3.2.7 EFM32G290

The features of the EFM32G290 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.7. EFM32G290 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 57)

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	$0.30 \times V_{DD}$[1]	V
Input high voltage	V_{IOIH}		$0.70 \times V_{DD}$[1]	—	—	V
Output high voltage (Production test condition = 3.0 V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.80 \times V_{DD}$	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.90 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.85 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.90 \times V_{DD}$	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75 \times V_{DD}$	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80 \times V_{DD}$	—	—	V

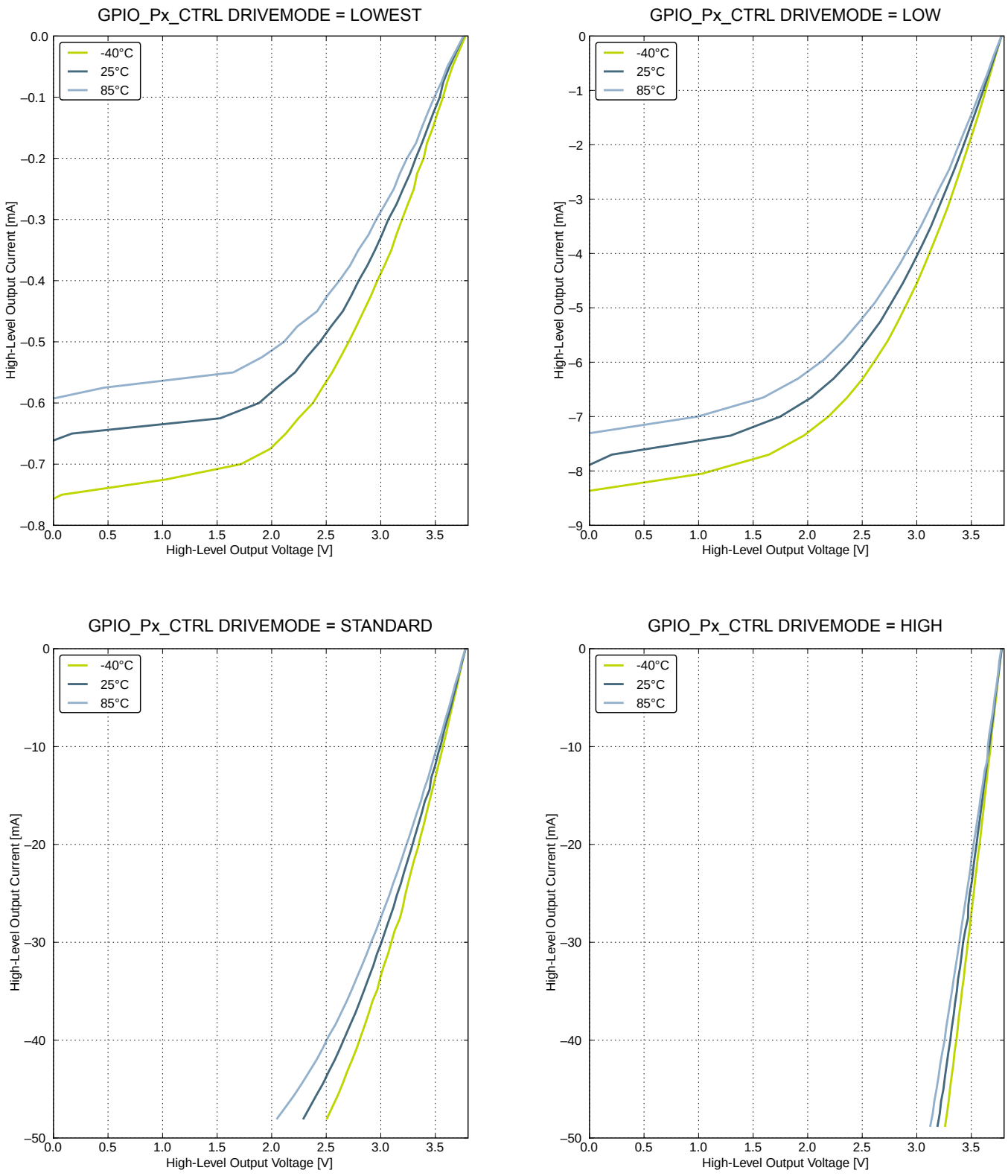

Figure 4.19. Typical High-Level Output Current, 3.8V Supply Voltage

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single-ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
Input range of external reference voltage, single-ended and differential	$V_{ADCREFIN}$		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{ADCREFIN\_CH7}$	See $V_{ADCREFIN}$	0	—	V_{DD} - 1.1	V
Input range of external positive reference voltage on channel 6	$V_{ADCREFIN\_CH6}$	See $V_{ADCREFIN}$	0.625	—	V_{DD}	V
Common mode input range	$V_{ADCCMIN}$		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	$CMRR_{ADC}$		—	65	—	dB
Average active current	I_{ADC}	1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	735[1]	—	µA
		1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	760[1]	—	µA
		500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	346[1]	—	µA
		500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	354[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	52[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	50[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	54[1]	—	µA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		1	—	—	MΩ
Input RC filter resistance	$R_{ADCFILT}$		—	10	—	kΩ
Input RC filter/decoupling capacitance	$C_{ADCFILT}$		—	250	—	fF
Input bias current	$I_{ADCBIASIN}$	VSS < VIN < VDD	-40	—	40	nA

4.13 Voltage Comparator (VCMP)

Table 4.17. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{VCMPIN}		—	V_{DD}	—	V
VCMP Common Mode voltage range	V_{VCMPCM}		—	V_{DD}	—	V
Active current	I_{VCMP}	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register	—	0.3	1	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.	—	22	30	µA
Startup time reference generator	$t_{VCMPREF}$	NORMAL	—	10	—	µs
Offset voltage	$V_{VCMPOFFSET}$	Single-ended	—	10	—	mV
		Differential	—	10	—	mV
VCMP hysteresis	$V_{VCMPHYST}$		—	40	—	mV
Startup time	$t_{VCMPSTART}$		—	—	10	µs

The $V_{DD\ Trigger\ Level}$ can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD\ Trigger\ Level} = 1.667V + 0.034 \times TRIGLEVEL$$

Table 5.1. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_1	Digital IO power supply 1.			
5	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
6	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
7	PB7	LFXTAL_P		US1_CLK #0	
8	PB8	LFXTAL_N		US1_CS #0	
9	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
11	AVDD_2	Analog power supply 2.			
12	PB13	HFXTAL_P		LEU0_TX #1	
13	PB14	HFXTAL_N		LEU0_RX #1	
14	IOVDD_3	Digital IO power supply 3.			
15	AVDD_0	Analog power supply 0.			
16	PD4	ADC0_CH4		LEU0_TX #0	
17	PD5	ADC0_CH5		LEU0_RX #0	
18	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
19	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
20	VDD_DREG	Power supply for on-chip voltage regulator.			
21	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
22	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
23	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
24	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
25	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
26	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
27	PF2				ACMP1_O #0 DBG_SWO #0
28	IOVDD_5	Digital IO power supply 5.			
29	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
30	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
6	PA5		EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
7	PA6		EBI_AD15 #0		LEU1_RX #1	
8	IOVDD_0	Digital IO power supply 0.				
9	PB0			TIM1_CC0 #2		
10	PB1			TIM1_CC1 #2		
11	PB2			TIM1_CC2 #2		
12	PB3			PCNT1_S0IN #1	US2_TX #1	
13	PB4			PCNT1_S1IN #1	US2_RX #1	
14	PB5				US2_CLK #1	
15	PB6				US2_CS #1	
16	VSS	Ground.				
17	IOVDD_1	Digital IO power supply 1.				
18	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
19	PC1	ACMP0_CH1		PCNT0_S1IN #2	US1_RX #0	
20	PC2	ACMP0_CH2			US2_TX #0	
21	PC3	ACMP0_CH3			US2_RX #0	
22	PC4	ACMP0_CH4		LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
23	PC5	ACMP0_CH5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
24	PB7	LFXTAL_P			US1_CLK #0	
25	PB8	LFXTAL_N			US1_CS #0	
26	PA7					
27	PA8			TIM2_CC0 #0		
28	PA9			TIM2_CC1 #0		
29	PA10			TIM2_CC2 #0		
30	PA11					
31	IOVDD_2	Digital IO power supply 2.				
32	VSS	Ground.				
33	PA12			TIM2_CC0 #1		
34	PA13			TIM2_CC1 #1		
35	PA14			TIM2_CC2 #1		
36	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
37	PB9					
38	PB10					
39	PB11	DAC0_OUT0		LETIM0_OUT0 #1		
40	PB12	DAC0_OUT1		LETIM0_OUT1 #1		
41	AVDD_1	Analog power supply 1.				
42	PB13	HFXTAL_P			LEU0_TX #1	
43	PB14	HFXTAL_N			LEU0_RX #1	
44	IOVDD_3	Digital IO power supply 3.				
45	AVDD_0	Analog power supply 0.				
46	PD0	ADC0_CH0		PCNT2_S0IN #0	US1_TX #1	
47	PD1	ADC0_CH1		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
48	PD2	ADC0_CH2		TIM0_CC1 #3	US1_CLK #1	
49	PD3	ADC0_CH3		TIM0_CC2 #3	US1_CS #1	
50	PD4	ADC0_CH4			LEU0_TX #0	
51	PD5	ADC0_CH5			LEU0_RX #0	
52	PD6	ADC0_CH6		LETIM0_OUT0 #0	I2C0_SDA #1	
53	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
54	PD8					CMU_CLK1 #1
55	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
56	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
60	PE0			PCNT0_S0IN #1	U0_TX #1	
61	PE1			PCNT0_S1IN #1	U0_RX #1	
62	PE2					ACMP0_O #1

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.15. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
K5	PA11					
K6	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
K7	AVSS_1	Analog ground 1.				
K8	AVDD_2	Analog power supply 2.				
K9	AVDD_1	Analog power supply 1.				
K10	AVSS_0	Analog ground 0.				
K11	PD1	ADC0_CH 1		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
L1	PB8	LFXTAL_N			US1_CS #0	
L2	PC5	ACMP0_C H5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
L3	PA14			TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OU T0		LETIM0_OUT0 #1		
L6	PB12	DAC0_OU T1		LETIM0_OUT1 #1		
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFXTAL_ P			LEU0_TX #1	
L9	PB14	HFXTAL_ N			LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH 0		PCNT2_S0IN #0	US1_TX #1	

5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.23. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

5.9.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G880 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.27. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L2	PC5	ACMP0_CH5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
L3	PA14	LCD_BEXT		TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0		LETIM0_OUT0 #1		
L6	PB12	DAC0_OUT1		LETIM0_OUT1 #1		
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFXTAL_P			LEU0_TX #1	
L9	PB14	HFXTAL_N			LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0		PCNT2_S0IN #0	US1_TX #1	

Alternate	LOCATION				
Functionality	0	1	2	3	Description
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

11.2 QFN32 PCB Layout

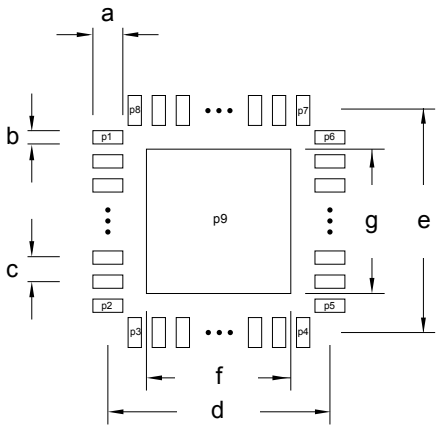

Figure 11.2. QFN32 PCB Land Pattern

Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	9	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17		
f	4.40				
g	4.40				

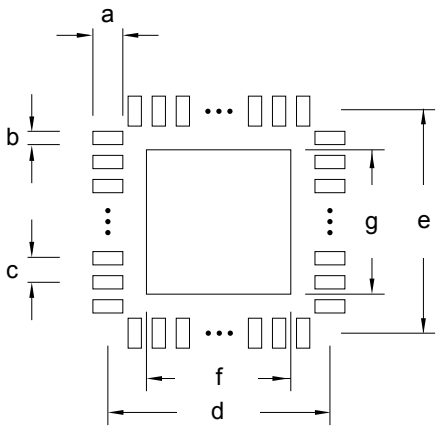

Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65

Symbol	Dim. (mm)
d	6.00
e	6.00
f	4.52
g	4.52

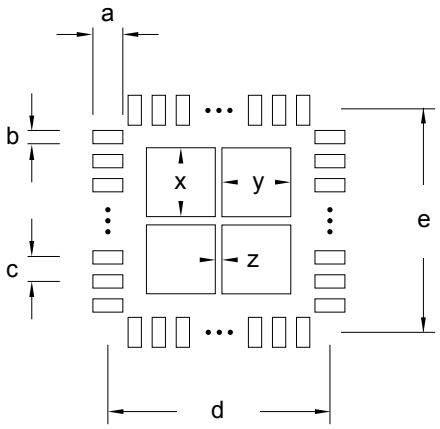

Figure 11.4. QFN32 PCB Stencil Design

Table 11.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.70
b	0.25
c	0.65
d	6.00
e	6.00
x	1.30
y	1.30
z	0.50

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see 5. Pin Definitions.

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

13.2 Revision 2.00

May 10th, 2017

Consolidated all EFM32G data sheets:

- EFM32G200
- EFM32G210
- EFM32G222
- EFM32G230
- EFM32G232
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G842
- EFM32G880
- EFM32G890

New formatting throughout.

Added 1. Feature List.

Updated ordering codes in 2. Ordering Information for Revision E and tape and reel.

Added Figure 2.1 Ordering Code Decoder on page 5.

Separated Memory Map figure into Figure 3.2 System Address Space with Core and Code Space Listing on page 27 and Figure 3.3 System Address Space with Peripheral Listing on page 28 for readability.

Removed footnote for storage temperature range in 4.2 Absolute Maximum Ratings.

In 4.6 Power Management:

- Updated EM0 condition for $V_{BODextthr-}$ specification.
- Added $V_{BODextthr-}$ in EM1 and EM2 specifications.
- Updated EM0 condition for $V_{BODextthr+}$ specification.

Updated Flash page erase time and device erase time in 4.7 Flash and added footnotes.

Updated figures in 4.9.3 LFRCO.

Updated figures and HFRCO current consumption typical values in 4.9.4 HFRCO.

In 4.10 Analog Digital Converter (ADC):

- Updated test conditions, updated specifications, and added footnote for average active current.
- Added input bias current.
- Added input offset current.
- Updated ADC clock frequency.
- Updated SNR, SINAD and SFDR.
- Updated offset voltage.
- Updated missing codes.
- Added gain error drift and offset error drift.
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

In 4.11 Digital Analog Converter (DAC):

- Updated I_{DAC} parameter, test conditions, and footnote.
- Added DAC load current specification to 4.11 Digital Analog Converter (DAC).
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

Updated ACMP active current (BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register) typical value in 4.12 Analog Comparator (ACMP).

Updated VCMP hysteresis typical value in 4.13 Voltage Comparator (VCMP).