**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32g222f128-qfp48t |

### 3.2.6 EFM32G280

The features of the EFM32G280 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

**Table 3.6. EFM32G280 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0] |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 86 pins | Available pins are shown in Table 4.3 (p. 57) |

### 3.2.8 EFM32G840

The features of the EFM32G840 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

**Table 3.8. EFM32G840 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 8-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0] |
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in Table 4.3 (p. 57) |
| LCD | Full configuration | LCD_SEG[23:0], LCD_COM[3:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

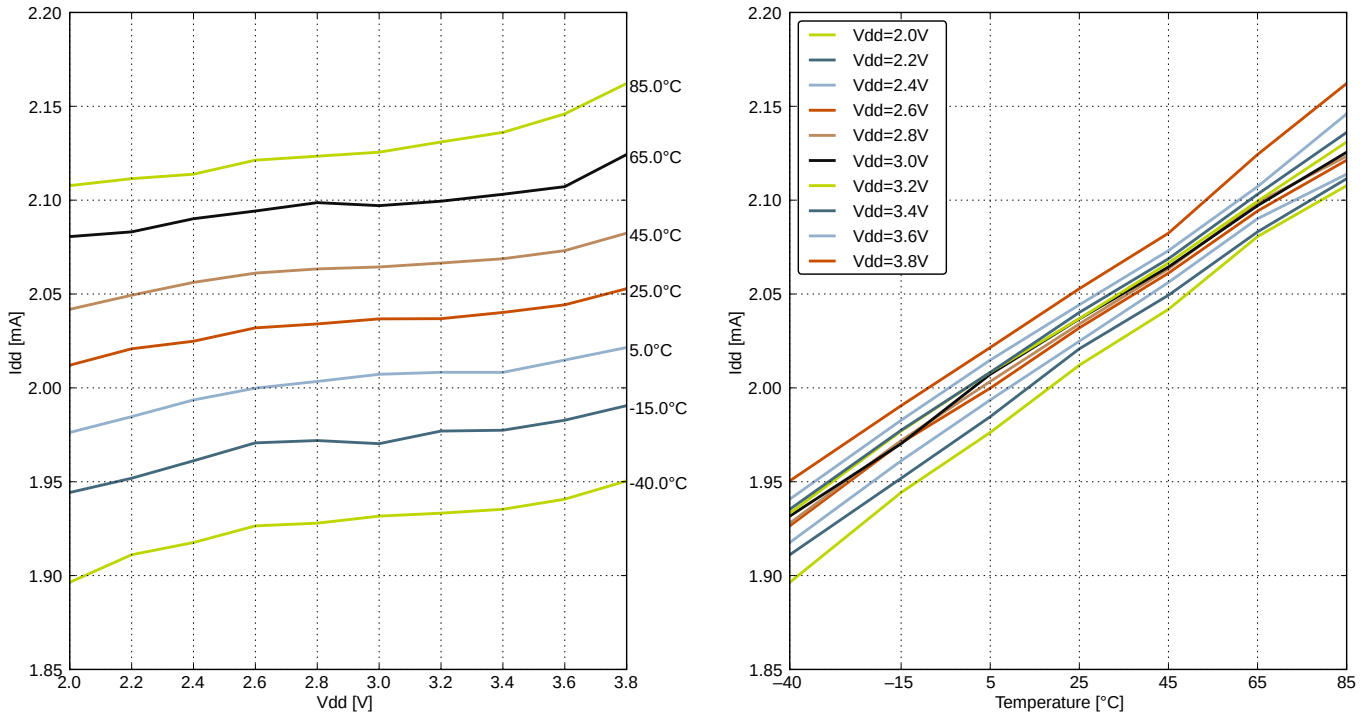


**Figure 4.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz**

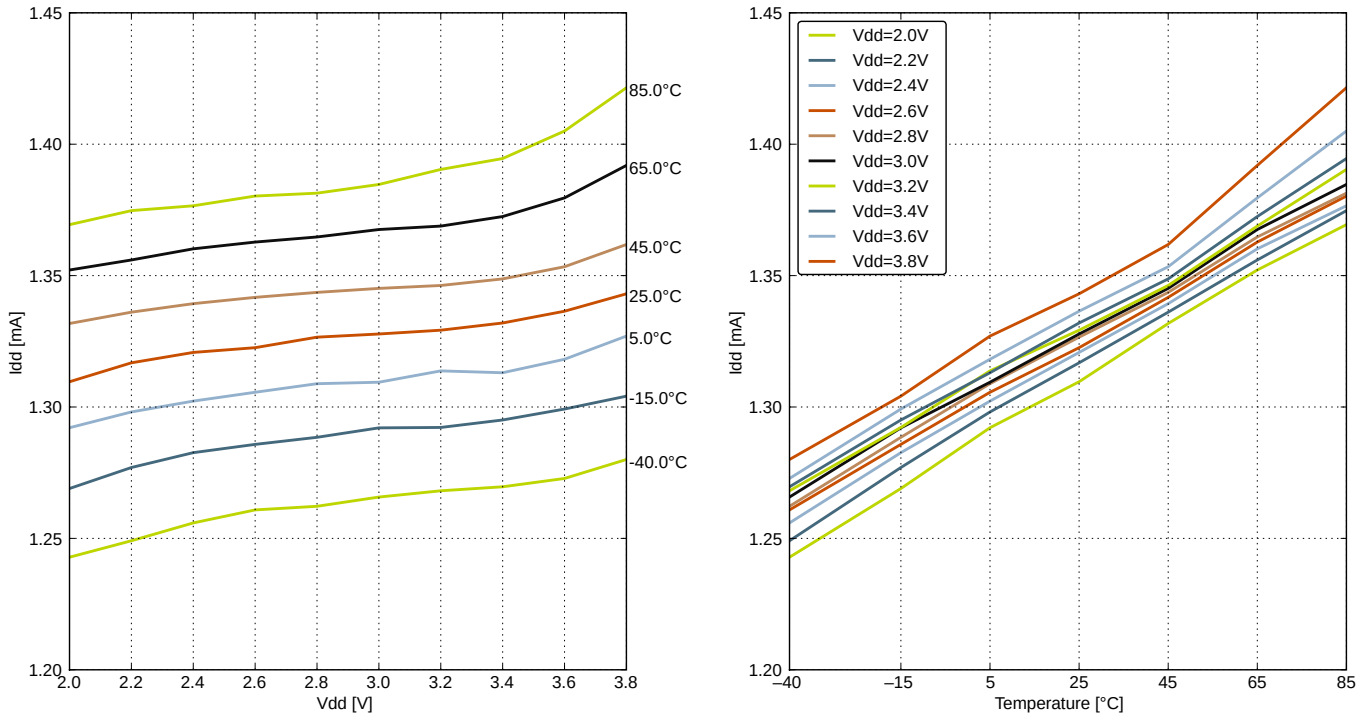


**Figure 4.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7 MHz**

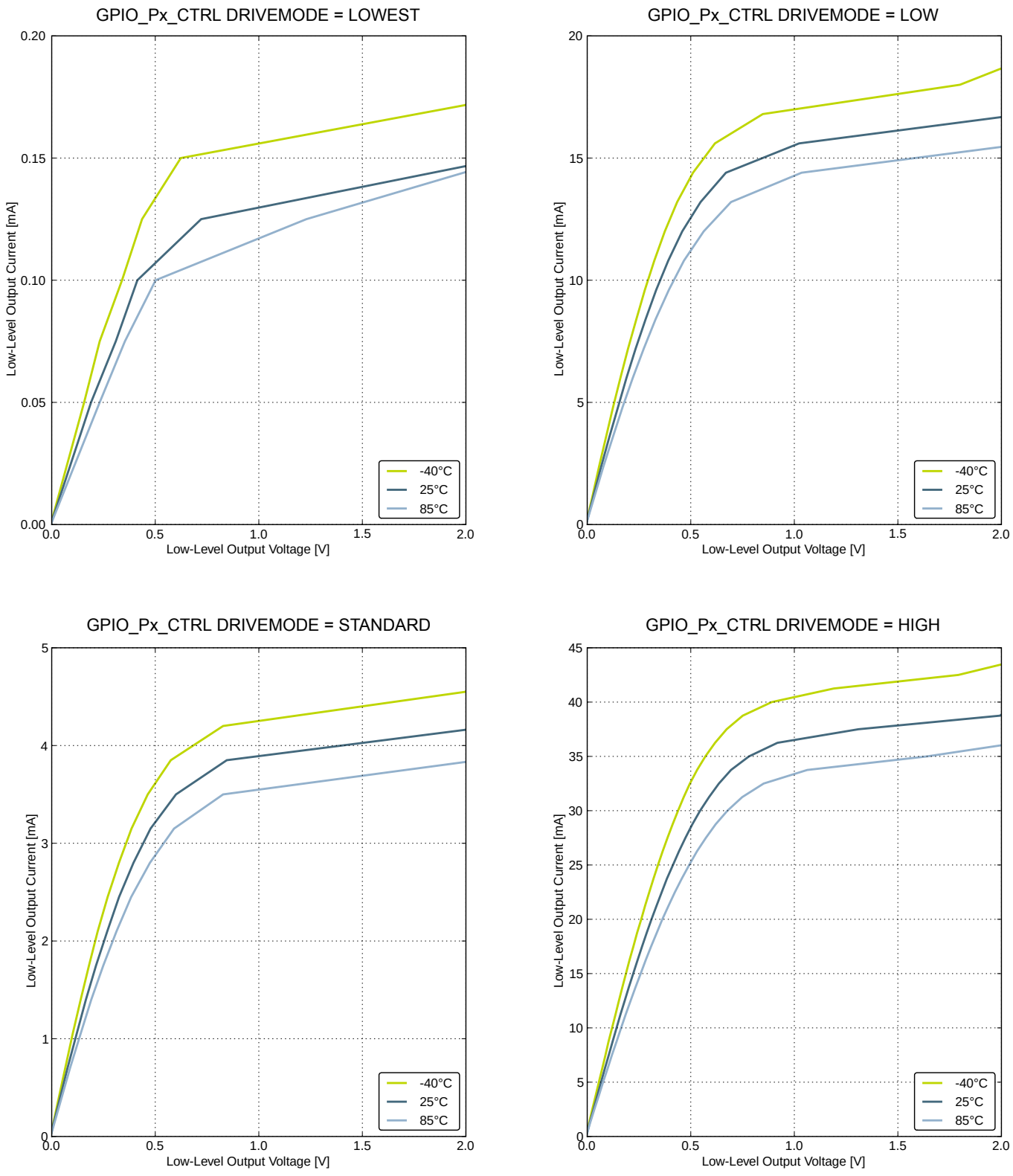


**Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage**

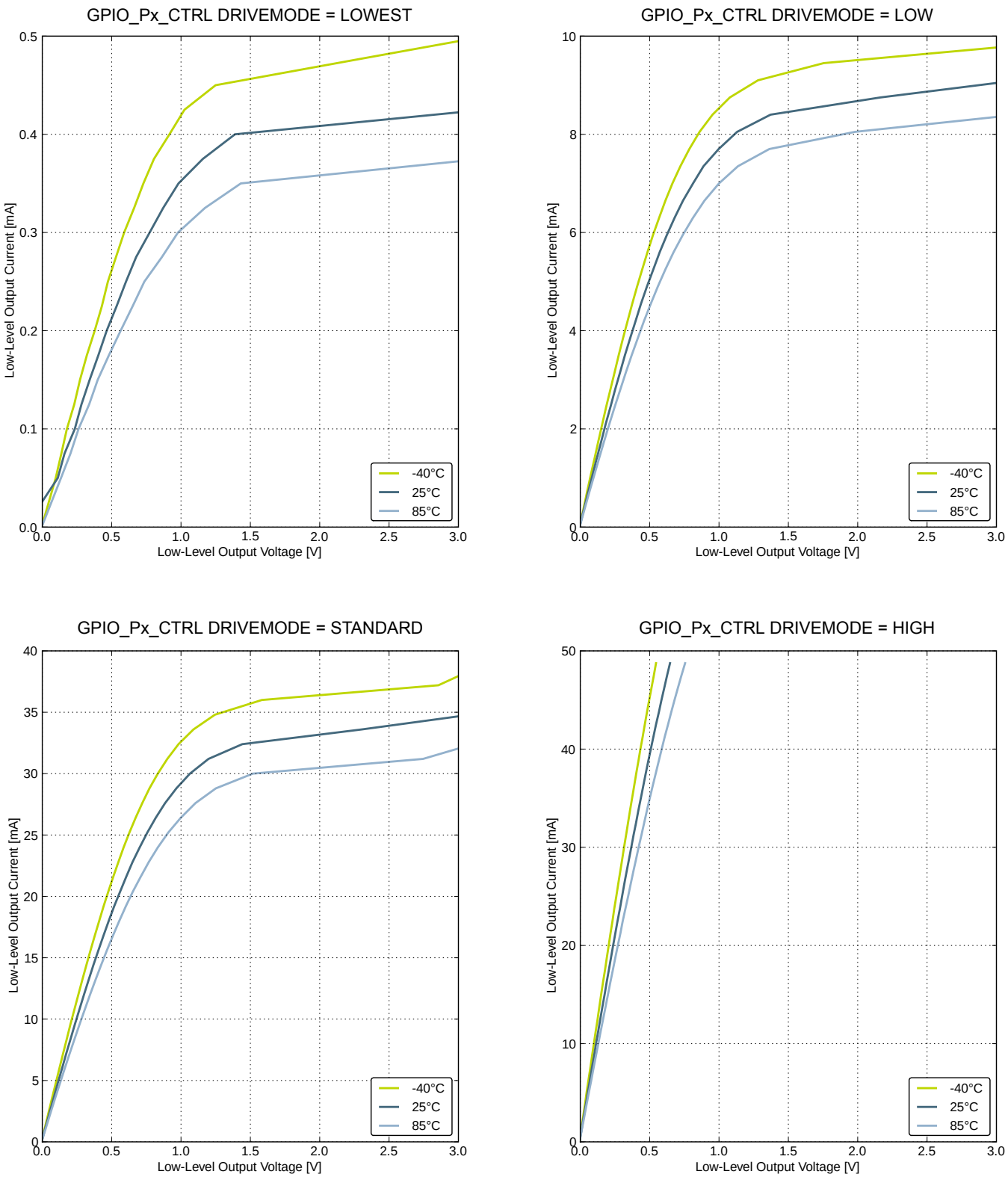


**Figure 4.16. Typical Low-Level Output Current, 3V Supply Voltage**

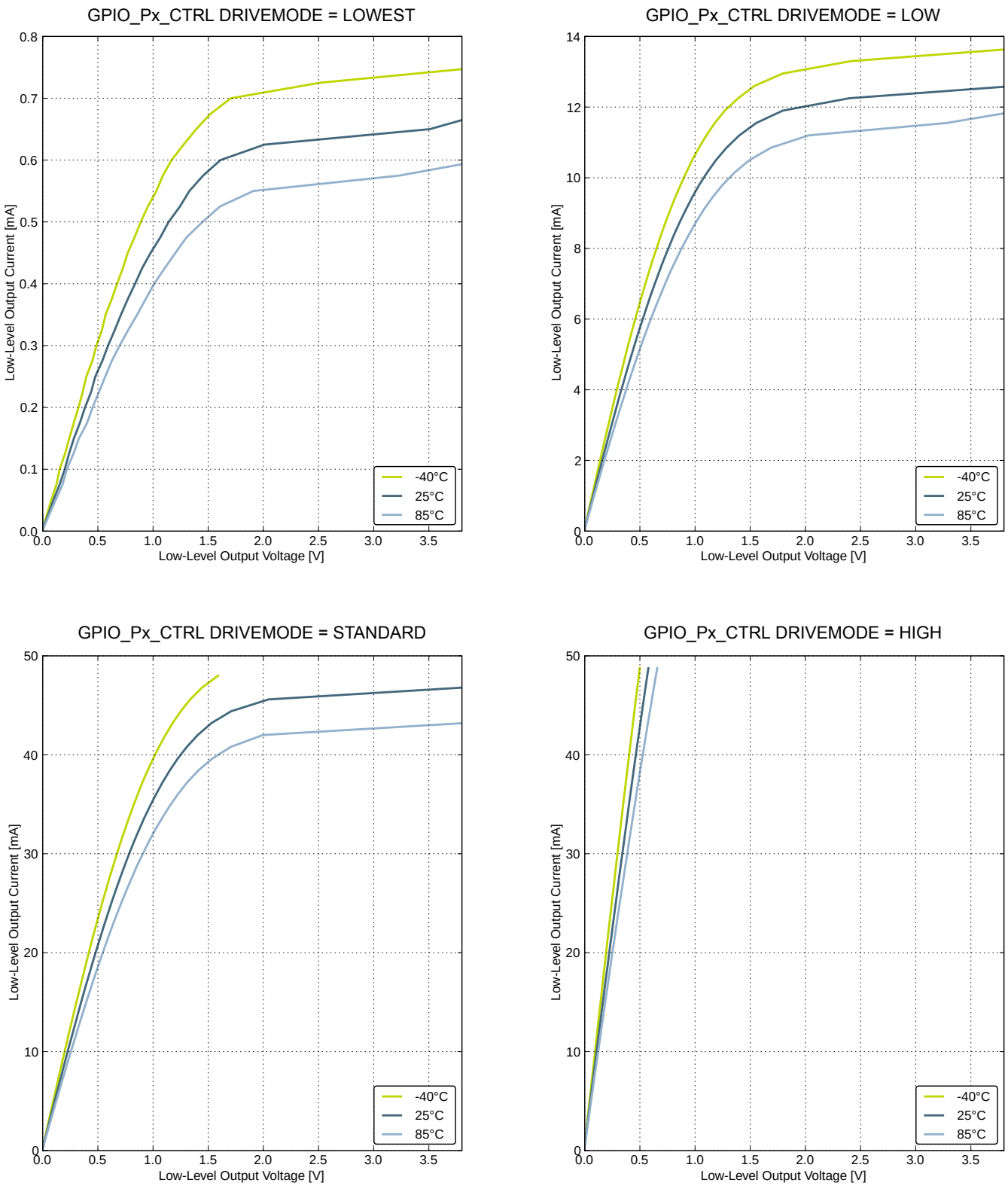


**Figure 4.18. Typical Low-Level Output Current, 3.8V Supply Voltage**

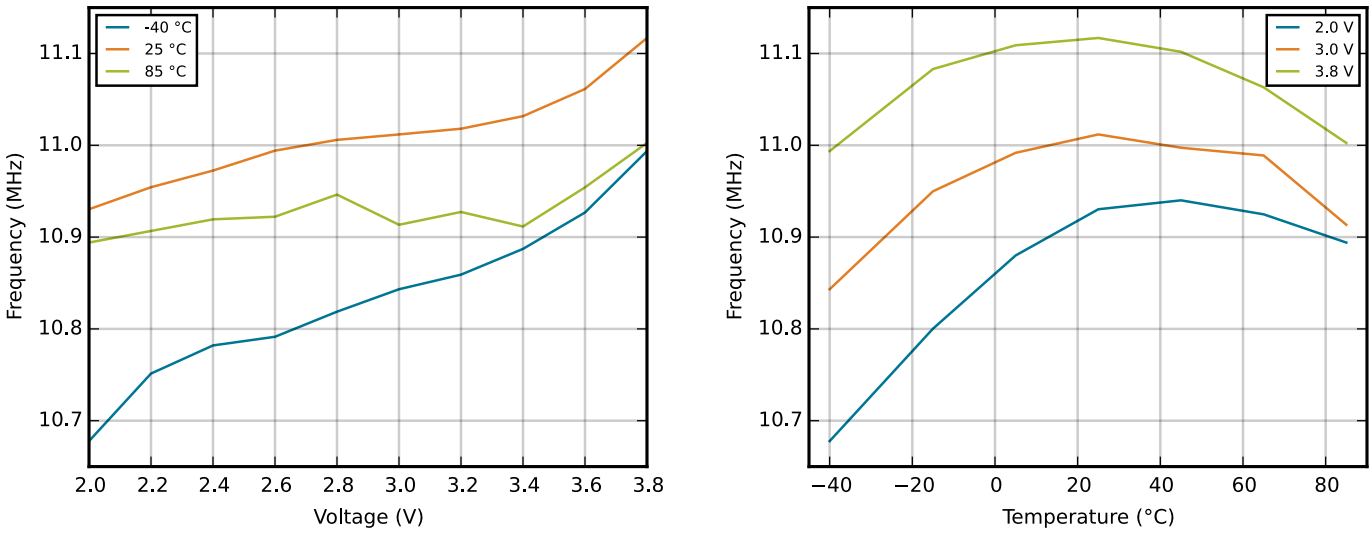


**Figure 4.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**

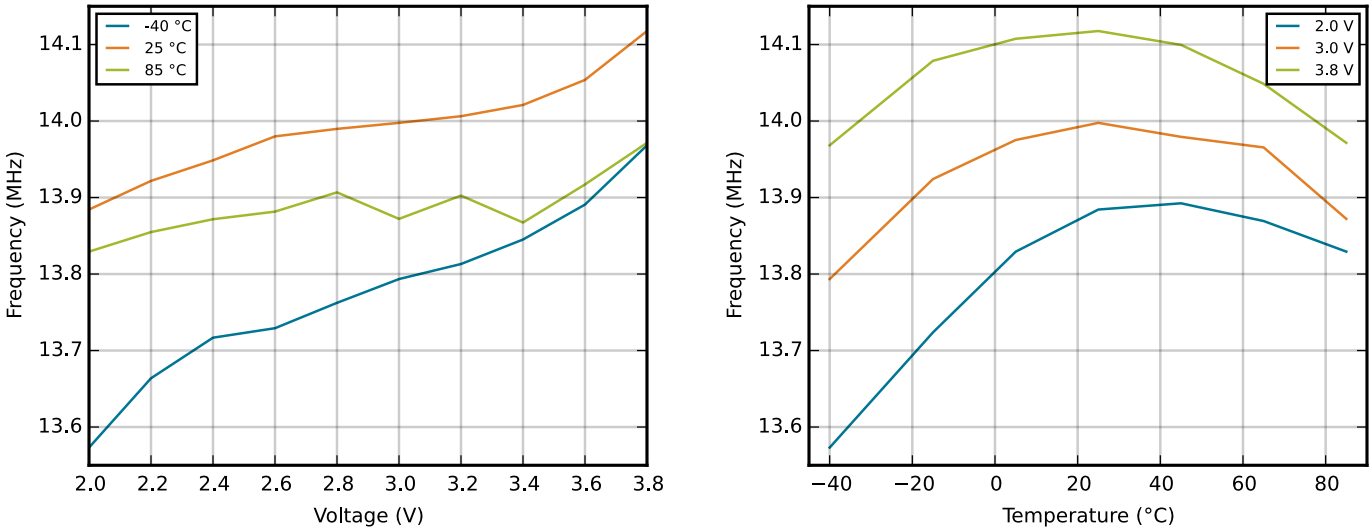


**Figure 4.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**

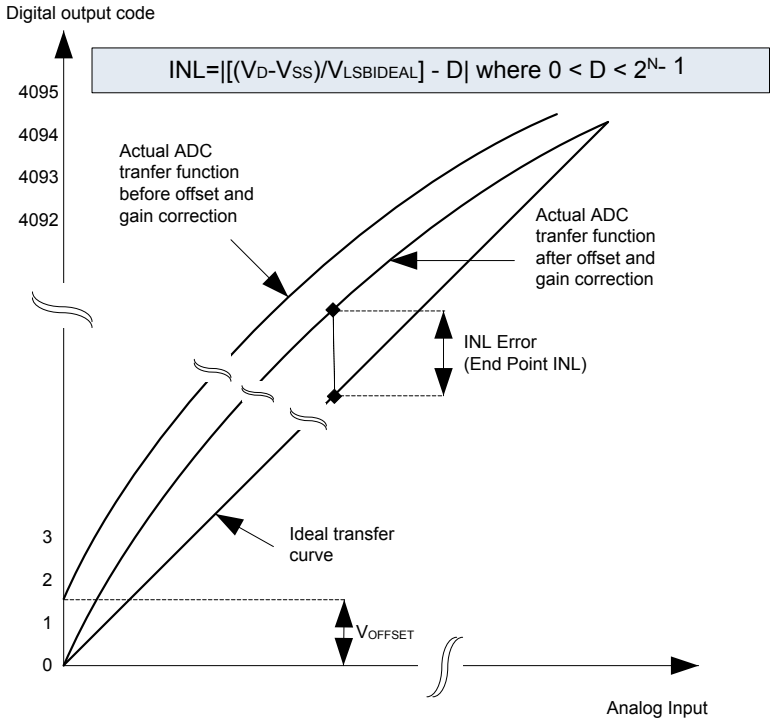


**Figure 4.27. Integral Non-Linearity (INL)**

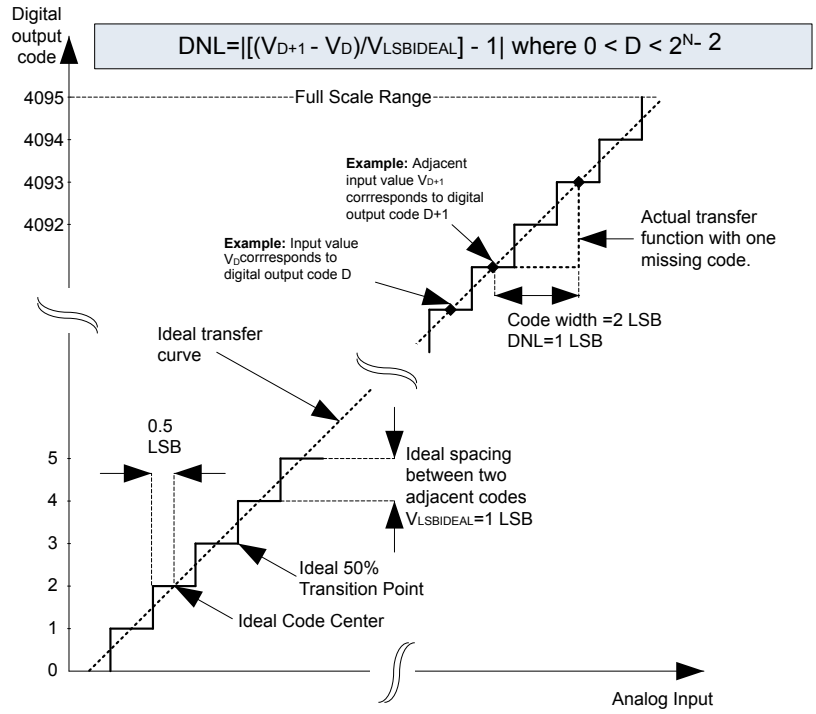


**Figure 4.28. Differential Non-Linearity (DNL)**

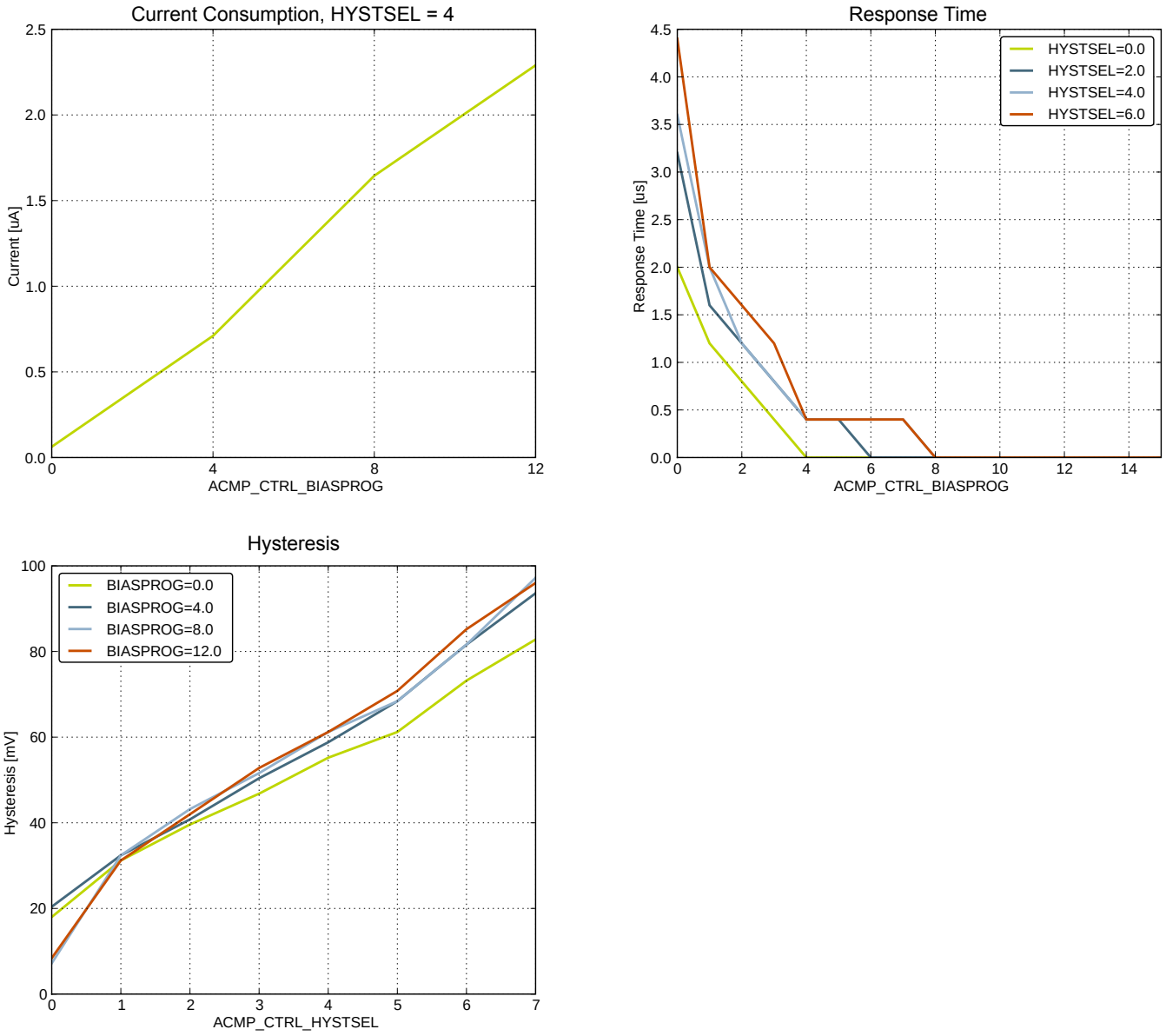


**Figure 4.34. ACMP Characteristics, VDD = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1**

# 5. Pin Definitions

**Note:** Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32G.

## 5.1 EFM32G200 & EFM32G210 (QFN32)

### 5.1.1 Pinout

The EFM32G200 and EFM32G210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

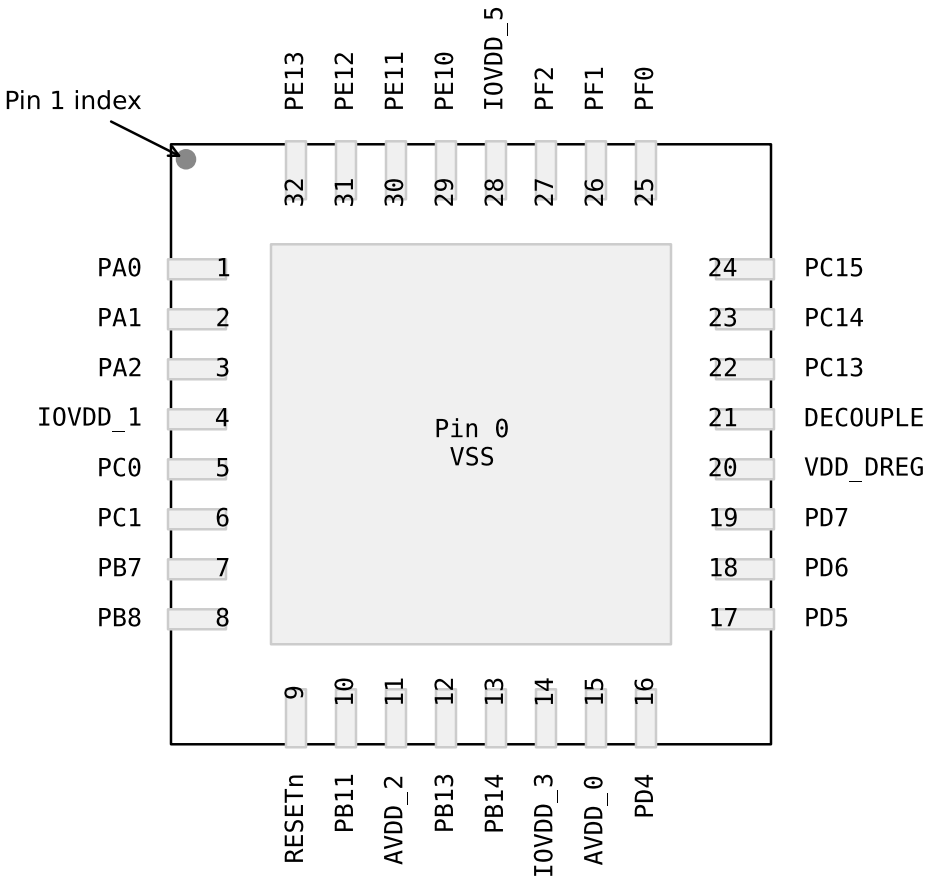


**Figure 5.1. EFM32G200 & EFM32G210 Pinout (top view, not to scale)**

| TQFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 6 | PC0 | ACMP0_CH0 | PCNT0_S0IN #2 | US1_TX #0 | |
| 7 | PC1 | ACMP0_CH1 | PCNT0_S1IN #2 | US1_RX #0 | |
| 8 | PC2 | ACMP0_CH2 | | | |
| 9 | PC3 | ACMP0_CH3 | | | |
| 10 | PC4 | ACMP0_CH4 | LETIM0_OUT0 #3 PCNT1_S0IN #0 | | |
| 11 | PB7 | LFXTAL_P | | US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | | US1_CS #0 | |
| 13 | PA8 | | TIM2_CC0 #0 | | |
| 14 | PA9 | | TIM2_CC1 #0 | | |
| 15 | PA10 | | TIM2_CC2 #0 | | |
| 16 | RESETn | Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | DAC0_OUT0 | LETIM0_OUT0 #1 | | |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |
| 24 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 25 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 26 | PD6 | ADC0_CH6 | LETIM0_OUT0 #0 | I2C0_SDA #1 | |
| 27 | PD7 | ADC0_CH7 | LETIM0_OUT1 #0 | I2C0_SCL #1 | |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 30 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | |
| 31 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | |
| 32 | PC10 | ACMP1_CH2 | TIM2_CC2 #2 | US0_RX #2 | |
| 33 | PC11 | ACMP1_CH3 | | US0_TX #2 | |
| 34 | PC13 | ACMP1_CH5 | TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0 | | |
| 35 | PC14 | ACMP1_CH6 | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | | |
| 36 | PC15 | ACMP1_CH7 | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | | DBG_SWO #1 |
| 37 | PF0 | | LETIM0_OUT0 #2 | | DBG_SWCLK #0/1 |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| TIM1_CC0 | PC13 | PE10 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | | | | USART2 clock input / output. |
| US2_CS | PC5 | | | | USART2 chip select input / output. |
| US2_RX | PC3 | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

## 5.5 EFM32G280 (LQFP100)

### 5.5.1 Pinout

The EFM32G280 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

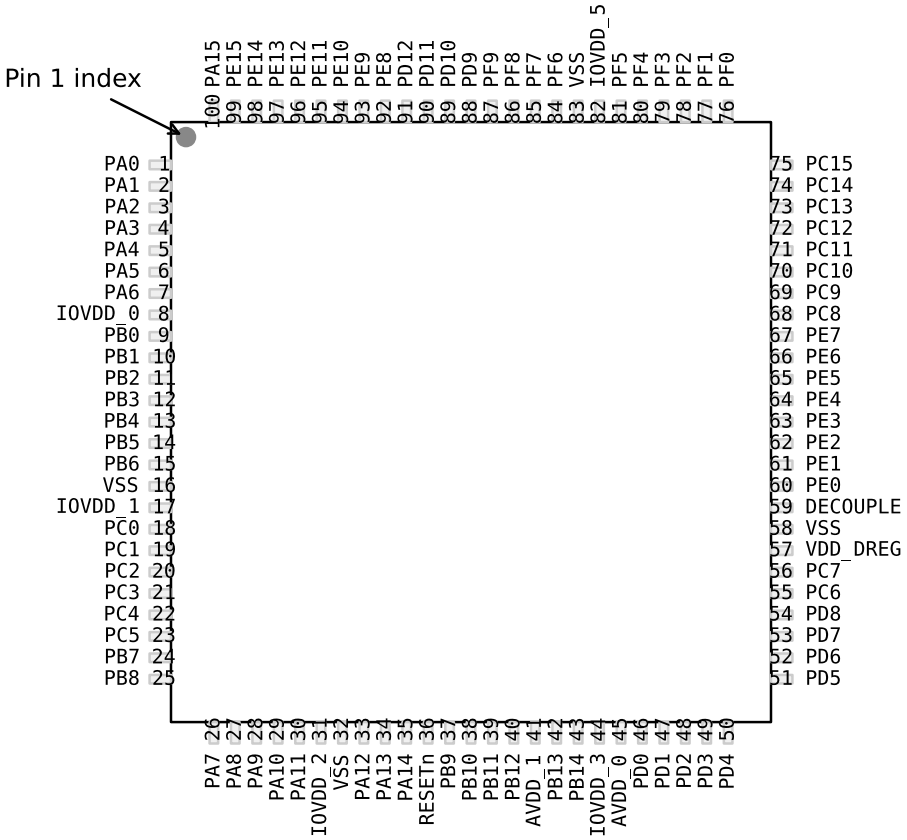


**Figure 5.5. EFM32G280 Pinout (top view, not to scale)**

**Table 5.13. Device Pinout**

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0 | |
| 2 | PA1 | | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 |
| 3 | PA2 | | EBI_AD11 #0 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | EBI_AD12 #0 | TIM0_CDTI0 #0 | U0_TX #2 | |
| 5 | PA4 | | EBI_AD13 #0 | TIM0_CDTI1 #0 | U0_RX #2 | |

| Alternate | LOCATION | | | | |
|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | Description |
| DBG_SWO | PF2 | PC15 | | | Debug-interface Serial Wire viewer Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| HFXTAL_N | PB14 | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 4 | PA3 | LCD_SEG 16 | EBI_AD12 #0 | TIM0_CDTI0 #0 | U0_TX #2 | |
| 5 | PA4 | LCD_SEG 17 | EBI_AD13 #0 | TIM0_CDTI1 #0 | U0_RX #2 | |
| 6 | PA5 | LCD_SEG 18 | EBI_AD14 #0 | TIM0_CDTI2 #0 | LEU1_TX #1 | |
| 7 | PA6 | LCD_SEG 19 | EBI_AD15 #0 | | LEU1_RX #1 | |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | LCD_SEG 32 | | TIM1_CC0 #2 | | |
| 10 | PB1 | LCD_SEG 33 | | TIM1_CC1 #2 | | |
| 11 | PB2 | LCD_SEG 34 | | TIM1_CC2 #2 | | |
| 12 | PB3 | LCD_SEG 20 | | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | LCD_SEG 21 | | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | LCD_SEG 22 | | | US2_CLK #1 | |
| 15 | PB6 | LCD_SEG 23 | | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0 | | PCNT0_S0IN #2 | US1_TX #0 | |
| 19 | PC1 | ACMP0_CH1 | | PCNT0_S1IN #2 | US1_RX #0 | |
| 20 | PC2 | ACMP0_CH2 | | | US2_TX #0 | |
| 21 | PC3 | ACMP0_CH3 | | | US2_RX #0 | |
| 22 | PC4 | ACMP0_CH4 | | LETIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 | |
| 23 | PC5 | ACMP0_CH5 | | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 | |
| 24 | PB7 | LFXTAL_P | | | US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | | US1_CS #0 | |
| 26 | PA7 | LCD_SEG 35 | | | | |
| 27 | PA8 | LCD_SEG 36 | | TIM2_CC0 #0 | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 77 | PF1 | | | LETIM0_OUT1 #2 | | DBG_SWDIO #0/1 |
| 78 | PF2 | LCD_SEG 0 | EBI_ARDY #0 | | | ACMP1_O #0<br>DBG_SWO #0 |
| 79 | PF3 | LCD_SEG 1 | EBI_ALE #0 | TIM0_CDTI0 #2 | | |
| 80 | PF4 | LCD_SEG 2 | EBI_WEn #0 | TIM0_CDTI1 #2 | | |
| 81 | PF5 | LCD_SEG 3 | EBI_REn #0 | TIM0_CDTI2 #2 | | |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | LCD_SEG 24 | | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | LCD_SEG 25 | | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | LCD_SEG 26 | | TIM0_CC2 #2 | | |
| 87 | PF9 | LCD_SEG 27 | | | | |
| 88 | PD9 | LCD_SEG 28 | EBI_CS0 #0 | | | |
| 89 | PD10 | LCD_SEG 29 | EBI_CS1 #0 | | | |
| 90 | PD11 | LCD_SEG 30 | EBI_CS2 #0 | | | |
| 91 | PD12 | LCD_SEG 31 | EBI_CS3 #0 | | | |
| 92 | PE8 | LCD_SEG 4 | EBI_AD00 #0 | PCNT2_S0IN #1 | | |
| 93 | PE9 | LCD_SEG 5 | EBI_AD01 #0 | PCNT2_S1IN #1 | | |
| 94 | PE10 | LCD_SEG 6 | EBI_AD02 #0 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | LCD_SEG 7 | EBI_AD03 #0 | TIM1_CC1 #1 | US0_RX #0 | BOOT_RX |
| 96 | PE12 | LCD_SEG 8 | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |
| 97 | PE13 | LCD_SEG 9 | EBI_AD05 #0 | | US0_CS #0 | ACMP0_O #0 |
| 98 | PE14 | LCD_SEG 10 | EBI_AD06 #0 | | LEU0_TX #2 | |
| 99 | PE15 | LCD_SEG 11 | EBI_AD07 #0 | | LEU0_RX #2 | |

## 5.10 EFM32G890 (BGA112)

### 5.10.1 Pinout

The EFM32G890 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

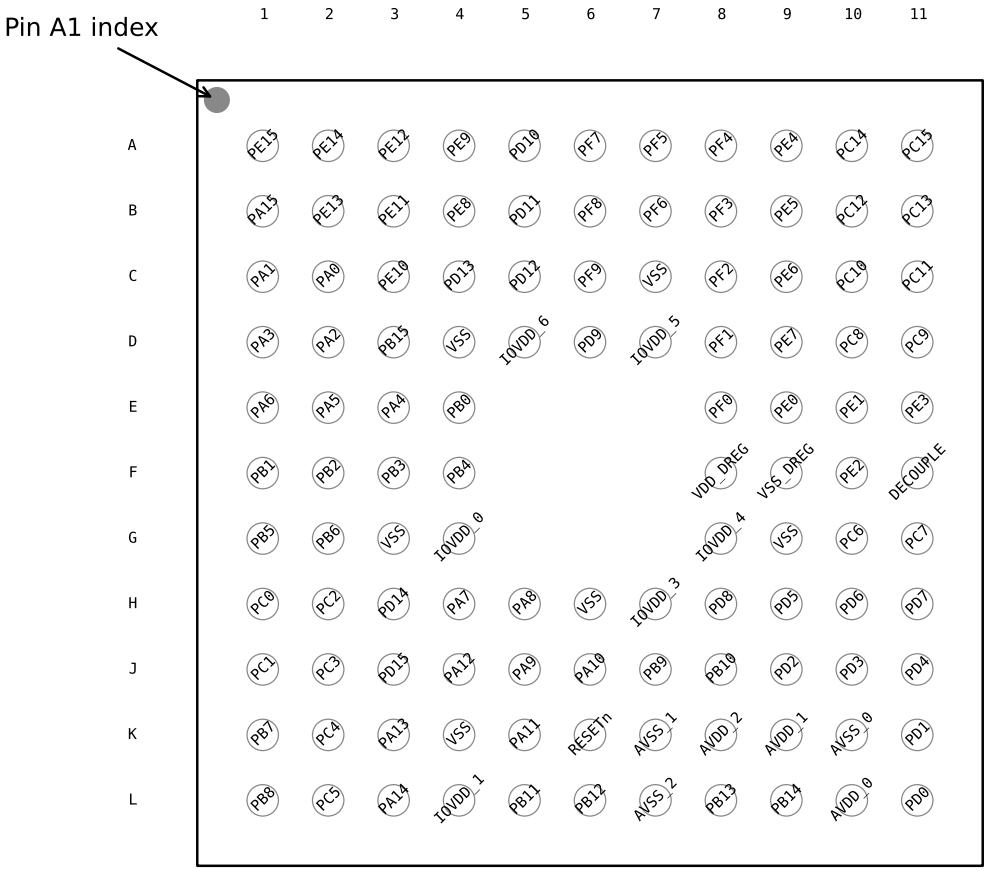


**Figure 5.10. EFM32G890 Pinout (top view, not to scale)**

**Table 5.28. Device Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG 11 | EBI_AD07 #0 | | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG 10 | EBI_AD06 #0 | | LEU0_TX #2 | |
| A3 | PE12 | LCD_SEG 8 | EBI_AD04 #0 | TIM1_CC2 #1 | US0_CLK #0 | |

### 6.2 BGA112 PCB Layout

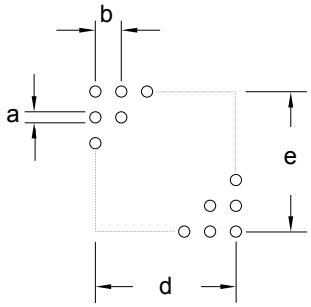


**Figure 6.2. BGA112 PCB Land Pattern**

**Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.35 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

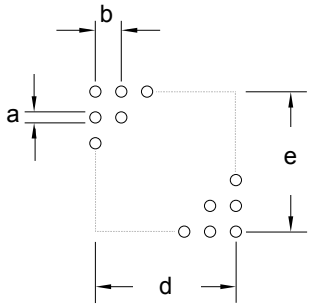


**Figure 6.3. BGA112 PCB Solder Mask**

**Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.48 |
| b | 0.80 |
| d | 8.00 |
| e | 8.00 |

### 9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

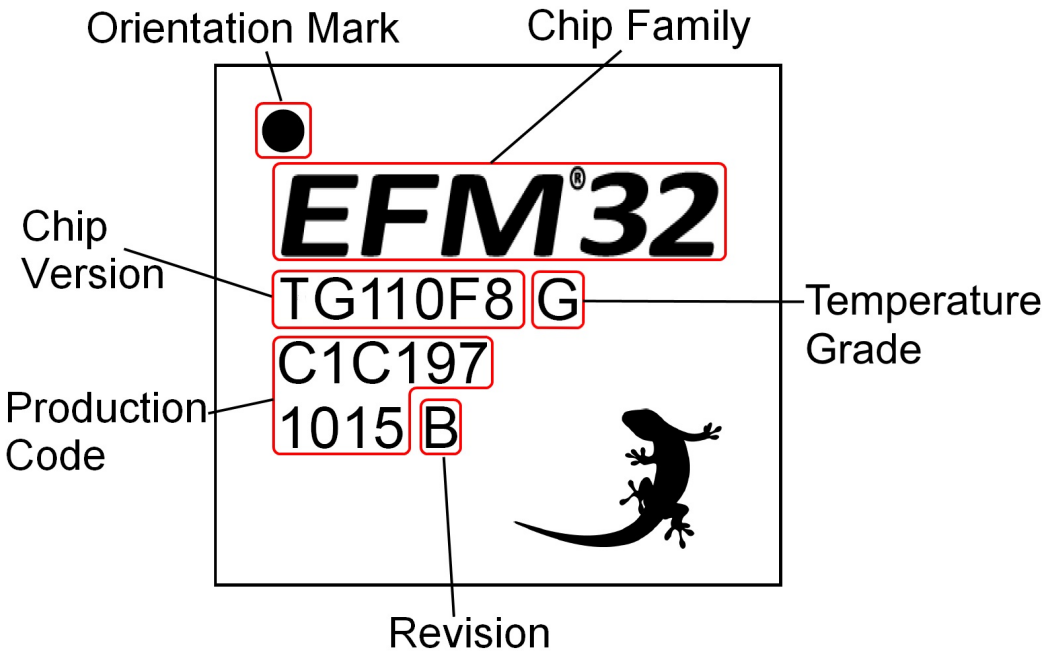


**Figure 9.5. Example Chip Marking (Top View)**

### 11.2 QFN32 PCB Layout

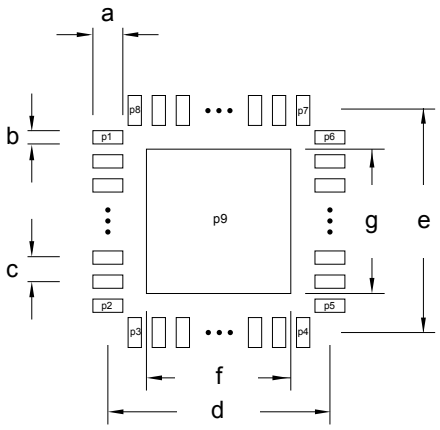


**Figure 11.2. QFN32 PCB Land Pattern**

**Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|---|---|---|---|---|---|
| a | 0.80 | P1 | 1 | P6 | 24 |
| b | 0.35 | P2 | 8 | P7 | 25 |
| c | 0.65 | P3 | 9 | P8 | 32 |
| d | 6.00 | P4 | 16 | P9 | 33 |
| e | 6.00 | P5 | 17 | | |
| f | 4.40 | | | | |
| g | 4.40 | | | | |

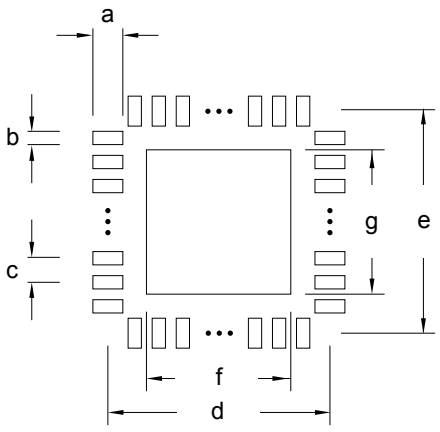


**Figure 11.3. QFN32 PCB Solder Mask**

**Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.92 |
| b | 0.47 |
| c | 0.65 |