Silicon Labs - EFM32G222F128G-E-QFP48 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g222f128g-e-qfp48

3. System Overview

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32G Reference Manual.

The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

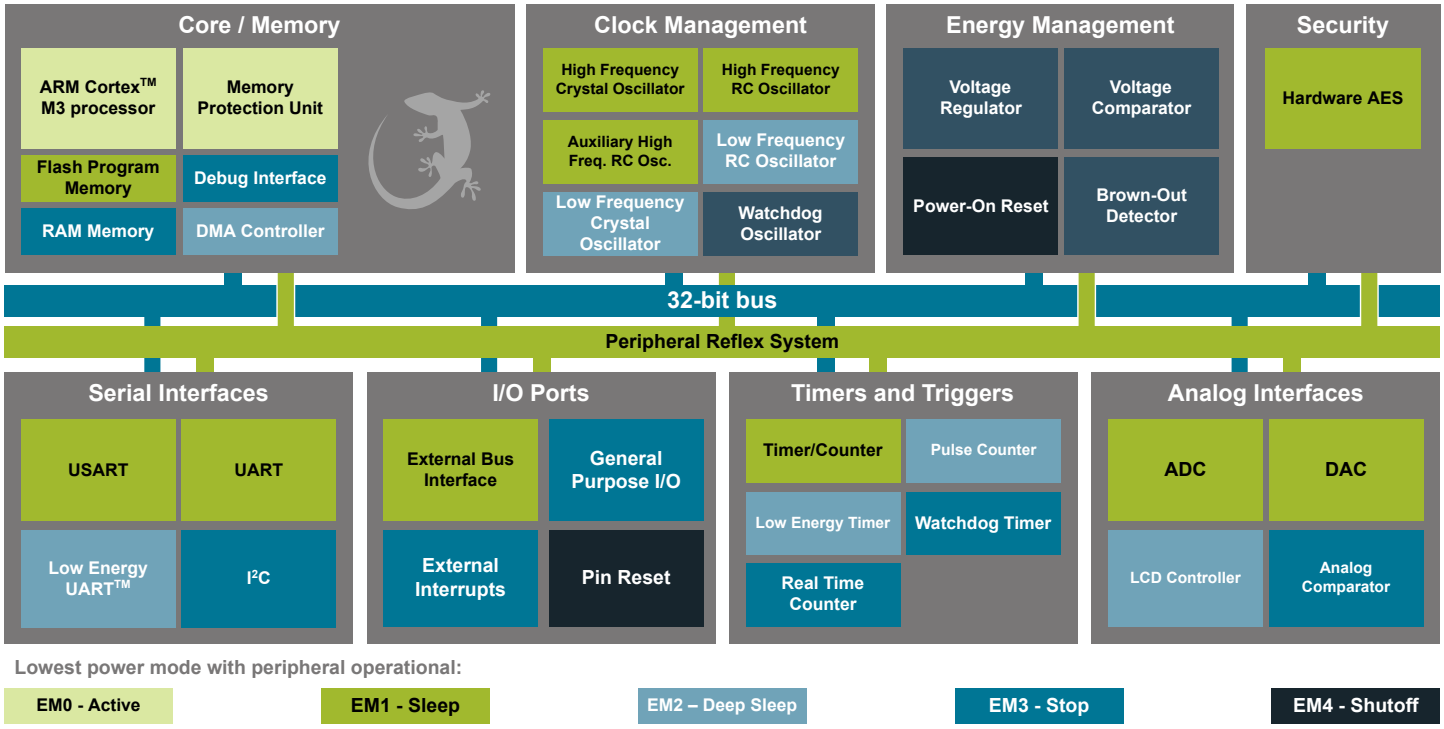

Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32G Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.2.6 EFM32G280

The features of the EFM32G280 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.6. EFM32G280 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	86 pins	Available pins are shown in Table 4.3 (p. 57)

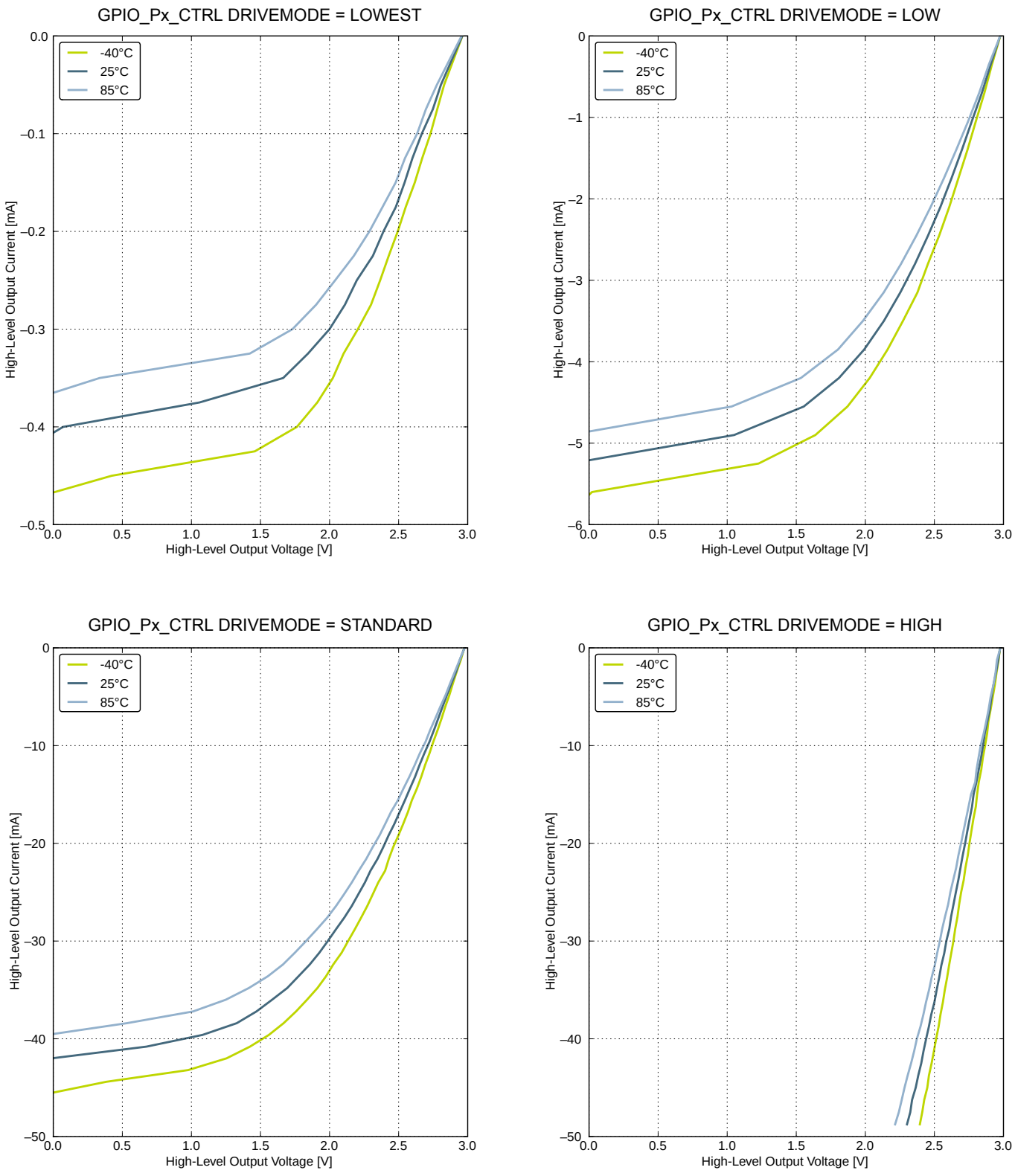

Figure 4.17. Typical High-Level Output Current, 3V Supply Voltage

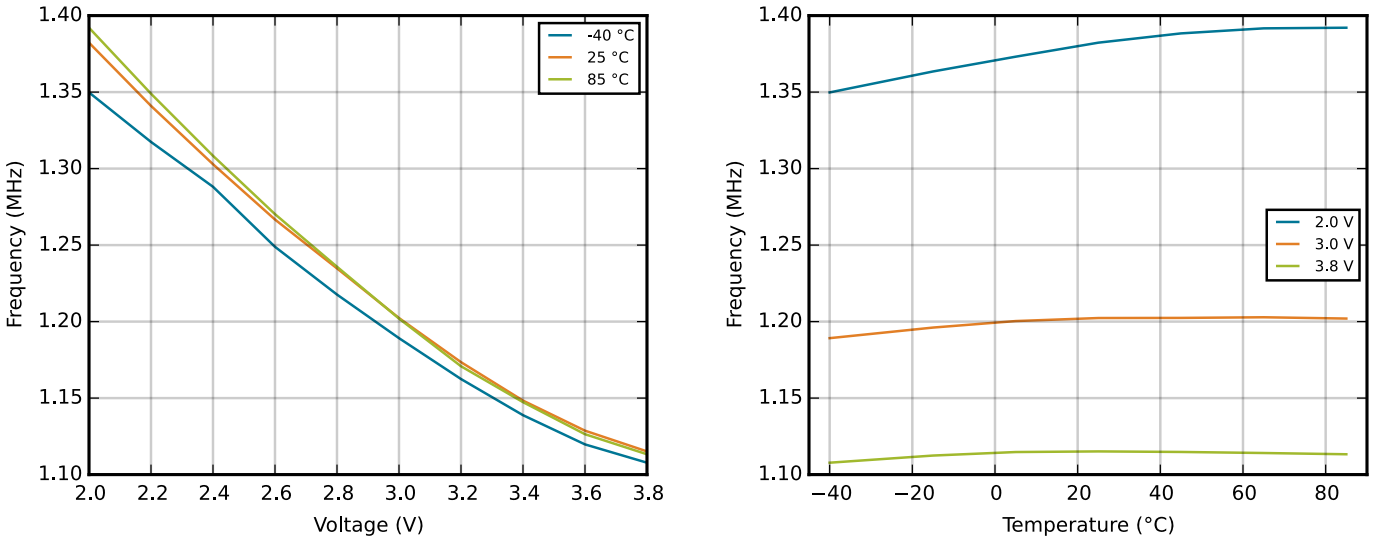

Figure 4.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

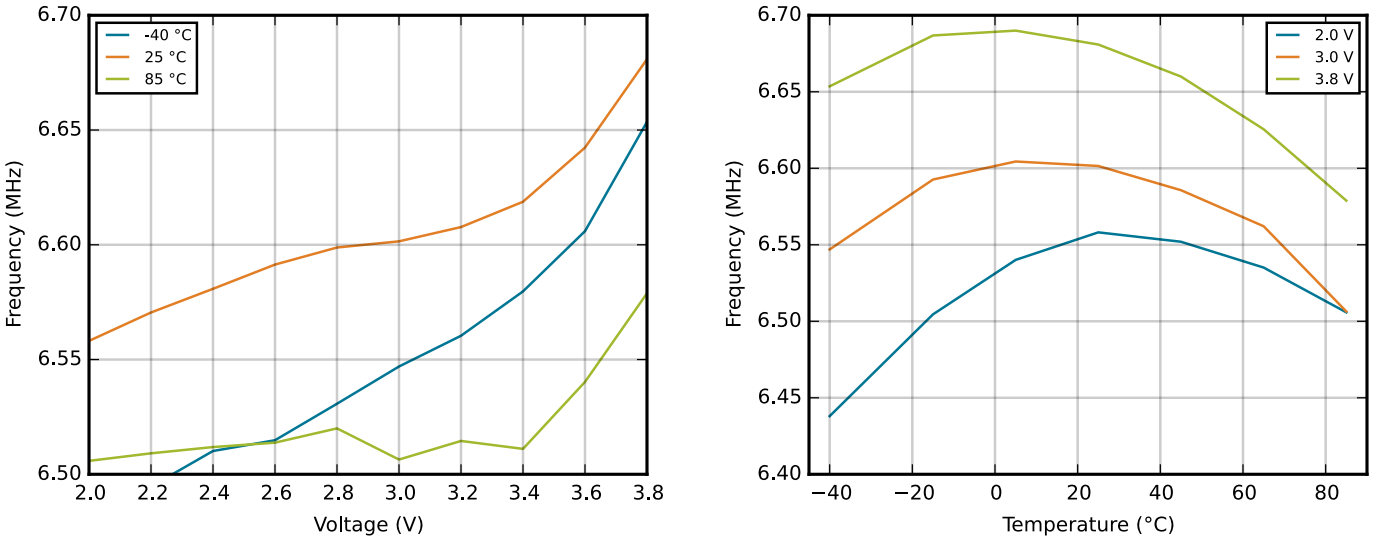

Figure 4.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

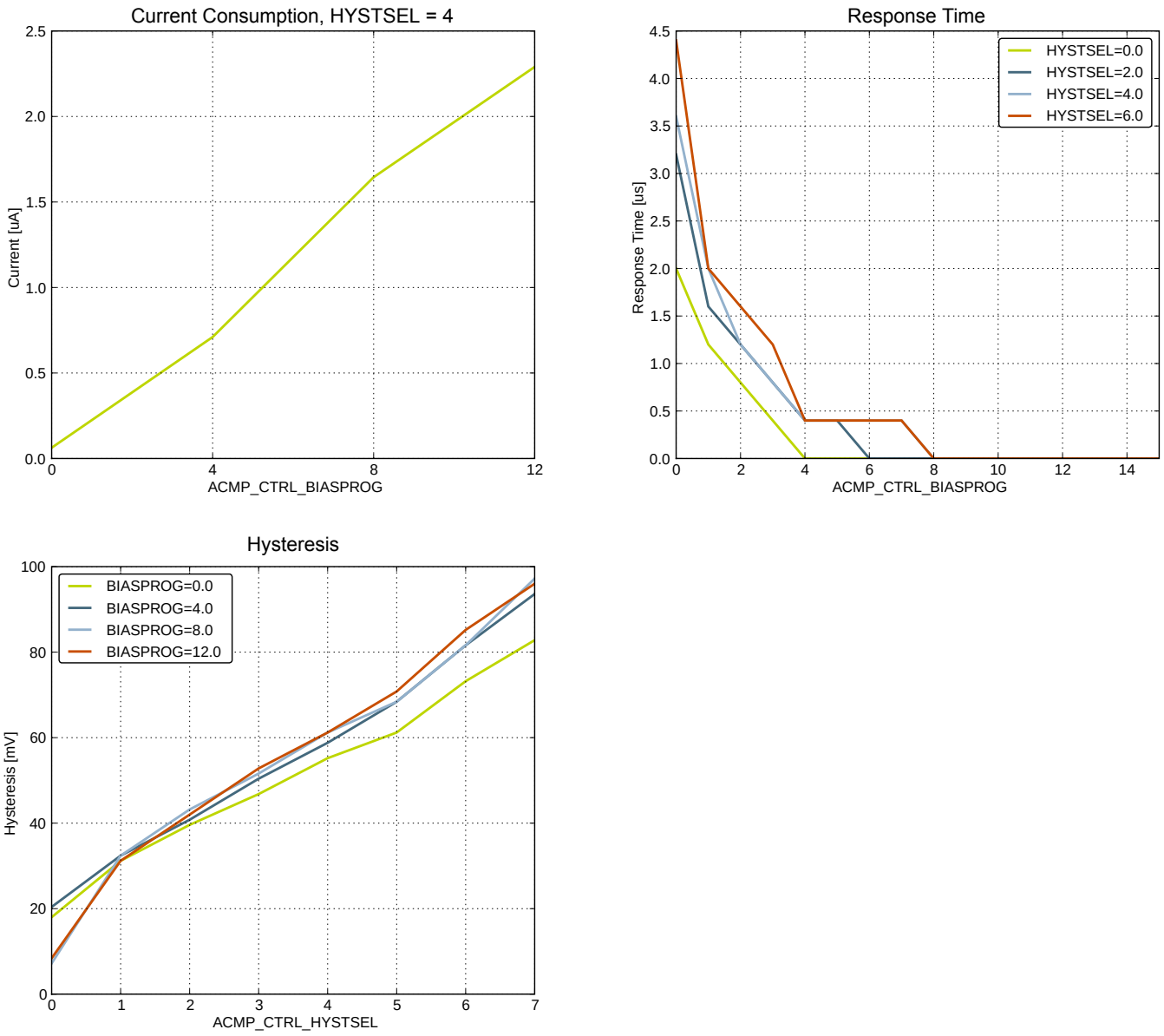

Figure 4.34. ACMP Characteristics, VDD = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1

4.14 LCD

Table 4.18. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		30	—	200	Hz
Number of segments supported	NUM_{SEG}		—	4×40	—	seg
LCD supply voltage range	V_{LCD}	Internal boost circuit enabled	2.0	—	3.8	V
Steady state current consumption.	I_{LCD}	Display disconnected, static mode, framerate 32 Hz, all segments on.	—	250	—	nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONE-THIRD in LCD_DISPCTRL register.	—	550	—	nA
Steady state Current contribution of internal boost.	$I_{LCDBOOST}$	Internal voltage boost off	—	0	—	µA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.	—	8.4	—	µA
Boost Voltage	V_{BOOST}	VBLEV of LCD_DISPCTRL register to LEVEL0	—	3.0	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL1	—	3.08	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL2	—	3.17	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL3	—	3.26	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL4	—	3.34	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL5	—	3.43	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL6	—	3.52	—	V
		VBLEV of LCD_DISPCTRL register to LEVEL7	—	3.6	—	V

The total LCD current is given by the following equation. $I_{LCDBOOST}$ is zero if internal boost is off.

$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$

Table 4.21. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000[1]	kHz
SCL clock low time	t_{LOW}	0.5	—	—	µs
SCL clock high time	t_{HIGH}	0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

4.16 Digital Peripherals

Table 4.22. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	µA/MHz
UART current	I_{UART}	UART idle current, clock enabled	—	5.63	—	µA/MHz
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	µA/MHz
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	µA/MHz
LETIMER current	$I_{LETIMER}$	LETIMER idle current, clock enabled	—	150	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
LCD current	I_{LCD}	LCD idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	µA/MHz
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	µA/MHz
EBI current	I_{EBI}	EBI idle current, clock enabled	—	1.56	—	µA/MHz
PRS current	I_{PRS}	PRS idle current	—	2.81	—	µA/MHz
DMA current	I_{DMA}	Clock enable	—	8.12	—	µA/MHz

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" forguidelines on designing Printed Circuit Boards (PCB's) for the EFM32G.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LETIM0_OUT1	PD7		PF1		Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14			LEUART0 Receive input.
LEU0_TX	PD4	PB13			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
TIM0_CC0	PA0	PA0			Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13		PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14		PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15		PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12				USART0 clock input / output.
US0_CS	PE13				USART0 chip select input / output.
US0_RX	PE11				USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10				USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7				USART1 clock input / output.
US1_CS	PB8				USART1 chip select input / output.
US1_RX	PC1				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G200 and EFM32G210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	—	—	—	—	—	—	—	—	—	—	—	—	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	—	—	—	—	—	—	—	—	—	—	—	PC1	PC0
Port D	—	—	—	—	—	—	—	—	PD7	PD6	PD5	PD4	—	—	—	—
Port E	—	—	PE13	PE12	PE11	PE10	—	—	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	—	—	—	PF2	PF1	PF0

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
7	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
8	PC2	ACMP0_CH2			
9	PC3	ACMP0_CH3			
10	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0		
11	PB7	LFXTAL_P		US1_CLK #0	
12	PB8	LFXTAL_N		US1_CS #0	
13	PA8		TIM2_CC0 #0		
14	PA9		TIM2_CC1 #0		
15	PA10		TIM2_CC2 #0		
16	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		LEU0_TX #1	
21	PB14	HFXTAL_N		LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
27	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
30	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
31	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
32	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
33	PC11	ACMP1_CH3		US0_TX #2	
34	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
35	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
36	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
37	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
D3	PB15					
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG 28	EBI_CS0 #0			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7				US0_TX #1	
D10	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6		EBI_AD15 #0		LEU1_RX #1	
E2	PA5		EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4		EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0			TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1
E9	PE0			PCNT0_S0IN #1	U0_TX #1	
E10	PE1			PCNT0_S1IN #1	U0_RX #1	
E11	PE3					ACMP1_O #1
F1	PB1			TIM1_CC1 #2		
F2	PB2			TIM1_CC2 #2		
F3	PB3			PCNT1_S0IN #1	US2_TX #1	
F4	PB4			PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2					ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5				US2_CLK #1	
G2	PB6				US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				

Alternate	LOCATION				
Functionality	0	1	2	3	Description
US2_TX		PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.7.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G840 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.21. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	—	—	—	—	—	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	PC15	PC14	PC13	PC12	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

Alternate	LOCATION				
Functionality	0	1	2	3	Description
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C3	PE10	LCD_SEG 6	EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					
C5	PD12	LCD_SEG 31	EBI_CS3 #0			
C6	PF9	LCD_SEG 27				
C7	VSS	Ground.				
C8	PF2	LCD_SEG 0	EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6	LCD_COM 2			US0_RX #1	
C10	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_CH3			US0_TX #2	
D1	PA3	LCD_SEG 16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2	LCD_SEG 15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
D3	PB15					
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG 28	EBI_CS0 #0			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7	LCD_COM 3			US0_TX #1	
D10	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6	LCD_SEG 19	EBI_AD15 #0		LEU1_RX #1	
E2	PA5	LCD_SEG 18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4	LCD_SEG 17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0	LCD_SEG 32		TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG30	PD11				LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12				LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0				LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1				LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2				LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7				LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8				LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9				LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10				LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11				LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.

6.2 BGA112 PCB Layout

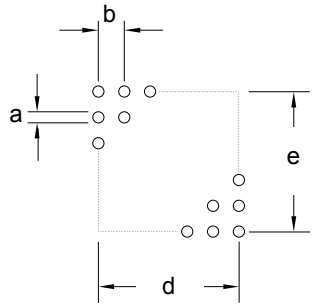

Figure 6.2. BGA112 PCB Land Pattern

Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.35
b	0.80
d	8.00
e	8.00

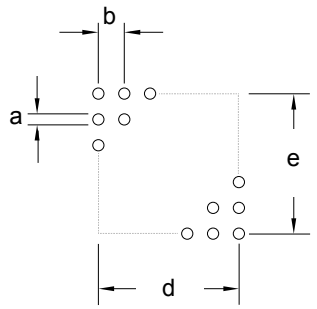

Figure 6.3. BGA112 PCB Solder Mask

Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.48
b	0.80
d	8.00
e	8.00

9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

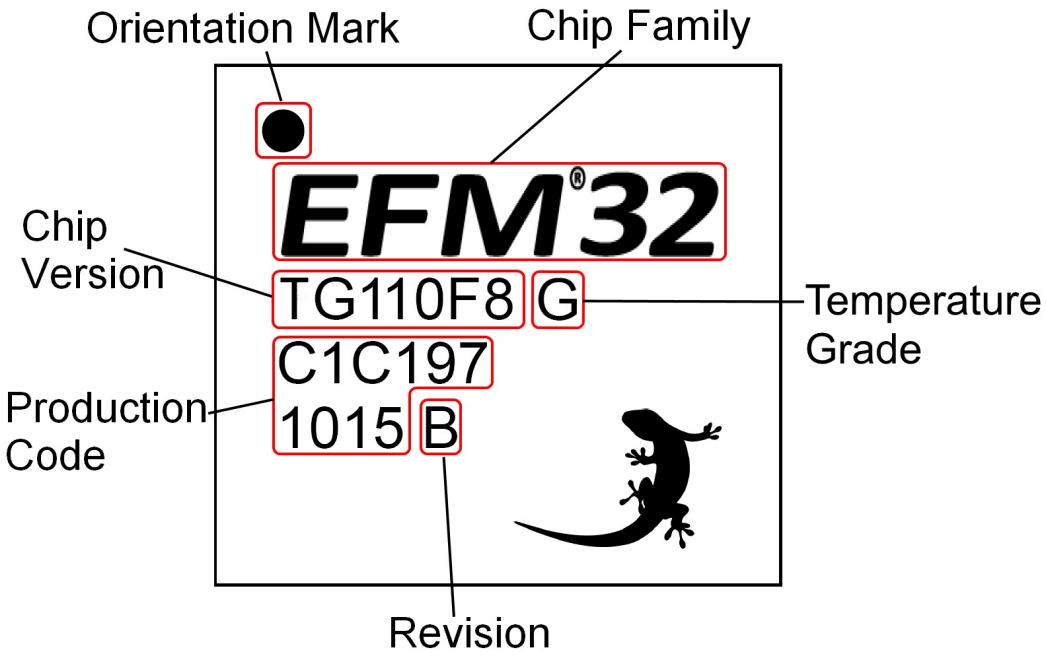

Figure 9.5. Example Chip Marking (Top View)

13.2 Revision 2.00

May 10th, 2017

Consolidated all EFM32G data sheets:

- EFM32G200
- EFM32G210
- EFM32G222
- EFM32G230
- EFM32G232
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G842
- EFM32G880
- EFM32G890

New formatting throughout.

Added 1. Feature List.

Updated ordering codes in 2. Ordering Information for Revision E and tape and reel.

Added Figure 2.1 Ordering Code Decoder on page 5.

Separated Memory Map figure into Figure 3.2 System Address Space with Core and Code Space Listing on page 27 and Figure 3.3 System Address Space with Peripheral Listing on page 28 for readability.

Removed footnote for storage temperature range in 4.2 Absolute Maximum Ratings.

In 4.6 Power Management:

- Updated EM0 condition for $V_{BODextthr-}$ specification.
- Added $V_{BODextthr-}$ in EM1 and EM2 specifications.
- Updated EM0 condition for $V_{BODextthr+}$ specification.

Updated Flash page erase time and device erase time in 4.7 Flash and added footnotes.

Updated figures in 4.9.3 LFRCO.

Updated figures and HFRCO current consumption typical values in 4.9.4 HFRCO.

In 4.10 Analog Digital Converter (ADC):

- Updated test conditions, updated specifications, and added footnote for average active current.
- Added input bias current.
- Added input offset current.
- Updated ADC clock frequency.
- Updated SNR, SINAD and SFDR.
- Updated offset voltage.
- Updated missing codes.
- Added gain error drift and offset error drift.
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

In 4.11 Digital Analog Converter (DAC):

- Updated I_{DAC} parameter, test conditions, and footnote.
- Added DAC load current specification to 4.11 Digital Analog Converter (DAC).
- Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

Updated ACMP active current (BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register) typical value in 4.12 Analog Comparator (ACMP).

Updated VCMP hysteresis typical value in 4.13 Voltage Comparator (VCMP).

13.13 Revision 1.10

September 13th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

For LQFP100 devices, corrected number of GPIO pins.

Added typical values for $R_{ADCFILT}$ and $C_{ADCFILT}$.

Added two conditions for DAC clock frequency; one for sample/hold and one for sample/off.

Added RoHS information and specified leadframe/solderballs material.

Added Serial Bootloader to feature list and system summary.

Updated ADC characterization data.

Updated DAC characterization data.

Updated RCO characterization data.

Updated ACMP characterization data.

Updated VCMP characterization data.

13.14 Revision 1.00

April 23rd, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

ADC_VCM line removed.

Added pinout illustration and additional pinout table.

Changed "Errata" chapter. Errata description moved to separate document.

Document changed status from "Preliminary".

Updated "Electrical Characteristics" chapter.

For EFM32G222

May 20th, 2011

Updated LFXO load capacitance section.