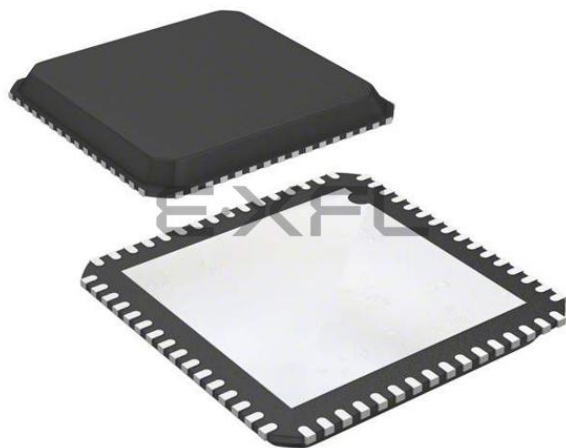




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#### Details

|                            |                                                                                                                                                             |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Discontinued at Digi-Key                                                                                                                                    |
| Core Processor             | ARM® Cortex®-M3                                                                                                                                             |
| Core Size                  | 32-Bit Single-Core                                                                                                                                          |
| Speed                      | 32MHz                                                                                                                                                       |
| Connectivity               | I <sup>2</sup> C, IrDA, SmartCard, SPI, UART/USART                                                                                                          |
| Peripherals                | Brown-out Detect/Reset, DMA, POR, PWM, WDT                                                                                                                  |
| Number of I/O              | 56                                                                                                                                                          |
| Program Memory Size        | 128KB (128K x 8)                                                                                                                                            |
| Program Memory Type        | FLASH                                                                                                                                                       |
| EEPROM Size                | -                                                                                                                                                           |
| RAM Size                   | 16K x 8                                                                                                                                                     |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V                                                                                                                                                |
| Data Converters            | A/D 8x12b; D/A 2x12b                                                                                                                                        |
| Oscillator Type            | Internal                                                                                                                                                    |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                           |
| Mounting Type              | Surface Mount                                                                                                                                               |
| Package / Case             | 64-VFQFN Exposed Pad                                                                                                                                        |
| Supplier Device Package    | 64-QFN (9x9)                                                                                                                                                |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/silicon-labs/efm32g230f128-qfn64t">https://www.e-xfl.com/product-detail/silicon-labs/efm32g230f128-qfn64t</a> |

- Supply Voltage Comparator
- Ultra efficient Power-on Reset and Brown-Out Detector
- 2-pin Serial Wire Debug Interface
  - 1-pin Serial Wire Viewer
- Pre-Programmed USB/UART Bootloader
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- Packages
  - BGA112
  - LQFP100
  - TQFP64
  - TQFP48
  - QFN64
  - QFN32

### 3.2.2 EFM32G210

The features of the EFM32G210 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

**Table 3.2. EFM32G210 Configuration Summary**

| Module    | Configuration                            | Pin Connections                               |
|-----------|------------------------------------------|-----------------------------------------------|
| Cortex-M3 | Full configuration                       | NA                                            |
| DBG       | Full configuration                       | DBG_SWCLK, DBG_SWDIO, DBG_SWO                 |
| MSC       | Full configuration                       | NA                                            |
| DMA       | Full configuration                       | NA                                            |
| RMU       | Full configuration                       | NA                                            |
| EMU       | Full configuration                       | NA                                            |
| CMU       | Full configuration                       | CMU_OUT0, CMU_OUT1                            |
| WDOG      | Full configuration                       | NA                                            |
| PRS       | Full configuration                       | NA                                            |
| I2C0      | Full configuration                       | I2C0_SDA, I2C0_SCL                            |
| USART0    | Full configuration with IrDA             | US0_TX, US0_RX, US0_CLK, US0_CS               |
| USART1    | Full configuration                       | US1_TX, US1_RX, US1_CLK, US1_CS               |
| LEUART0   | Full configuration                       | LEU0_TX, LEU0_RX                              |
| TIMER0    | Full configuration with DTI              | TIM0_CC[2:0], TIM0_CDTI[2:0]                  |
| TIMER1    | Full configuration                       | TIM1_CC[2:0]                                  |
| RTC       | Full configuration                       | NA                                            |
| LETIMER0  | Full configuration                       | LET0_O[1:0]                                   |
| PCNT0     | Full configuration, 8-bit count register | PCNT0_S[1:0]                                  |
| ACMP0     | Full configuration                       | ACMP0_CH[1:0], ACMP0_O                        |
| ACMP1     | Full configuration                       | ACMP1_CH[7:5], ACMP1_O                        |
| VCMP      | Full configuration                       | NA                                            |
| ADC0      | Full configuration                       | ADC0_CH[7:4]                                  |
| DAC0      | Full configuration                       | DAC0_OUT[0]                                   |
| AES       | Full configuration                       | NA                                            |
| GPIO      | 24 pins                                  | Available pins are shown in Table 4.3 (p. 57) |

### 3.2.10 EFM32G880

The features of the EFM32G880 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

**Table 3.10. EFM32G880 Configuration Summary**

| Module    | Module                                   | Module                                                         |
|-----------|------------------------------------------|----------------------------------------------------------------|
| Cortex-M3 | Full configuration                       | NA                                                             |
| DBG       | Full configuration                       | DBG_SWCLK, DBG_SWDIO, DBG_SWO                                  |
| MSC       | Full configuration                       | NA                                                             |
| DMA       | Full configuration                       | NA                                                             |
| RMU       | Full configuration                       | NA                                                             |
| EMU       | Full configuration                       | NA                                                             |
| CMU       | Full configuration                       | CMU_OUT0, CMU_OUT1                                             |
| WDOG      | Full configuration                       | NA                                                             |
| PRS       | Full configuration                       | NA                                                             |
| EBI       | Full configuration                       | EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0] |
| I2C0      | Full configuration                       | I2C0_SDA, I2C0_SCL                                             |
| USART0    | Full configuration with IrDA             | US0_TX, US0_RX, US0_CLK, US0_CS                                |
| USART1    | Full configuration                       | US1_TX, US1_RX, US1_CLK, US1_CS                                |
| USART2    | Full configuration                       | US2_TX, US2_RX, US2_CLK, US2_CS                                |
| UART0     | Full configuration                       | U0_TX, U0_RX                                                   |
| LEUART0   | Full configuration                       | LEU0_TX, LEU0_RX                                               |
| LEUART1   | Full configuration                       | LEU1_TX, LEU1_RX                                               |
| TIMER0    | Full configuration with DTI              | TIM0_CC[2:0], TIM0_CDTI[2:0]                                   |
| TIMER1    | Full configuration                       | TIM1_CC[2:0]                                                   |
| TIMER2    | Full configuration                       | TIM2_CC[2:0]                                                   |
| RTC       | Full configuration                       | NA                                                             |
| LETIMER0  | Full configuration                       | LET0_O[1:0]                                                    |
| PCNT0     | Full configuration, 8-bit count register | PCNT0_S[1:0]                                                   |
| PCNT1     | Full configuration, 8-bit count register | PCNT1_S[1:0]                                                   |
| PCNT2     | Full configuration, 8-bit count register | PCNT2_S[1:0]                                                   |
| ACMP0     | Full configuration                       | ACMP0_CH[7:0], ACMP0_O                                         |
| ACMP1     | Full configuration                       | ACMP1_CH[7:0], ACMP1_O                                         |
| VCMP      | Full configuration                       | NA                                                             |
| ADC0      | Full configuration                       | ADC0_CH[7:0]                                                   |
| DAC0      | Full configuration                       | DAC0_OUT[1:0]                                                  |
| AES       | Full configuration                       | NA                                                             |
| GPIO      | 86 pins                                  | Available pins are shown in Table 4.3 (p. 57)                  |

### 3.3 Memory Map

The EFM32G memory map is shown in the figure below. RAM and Flash sizes are for the largest memory configuration.

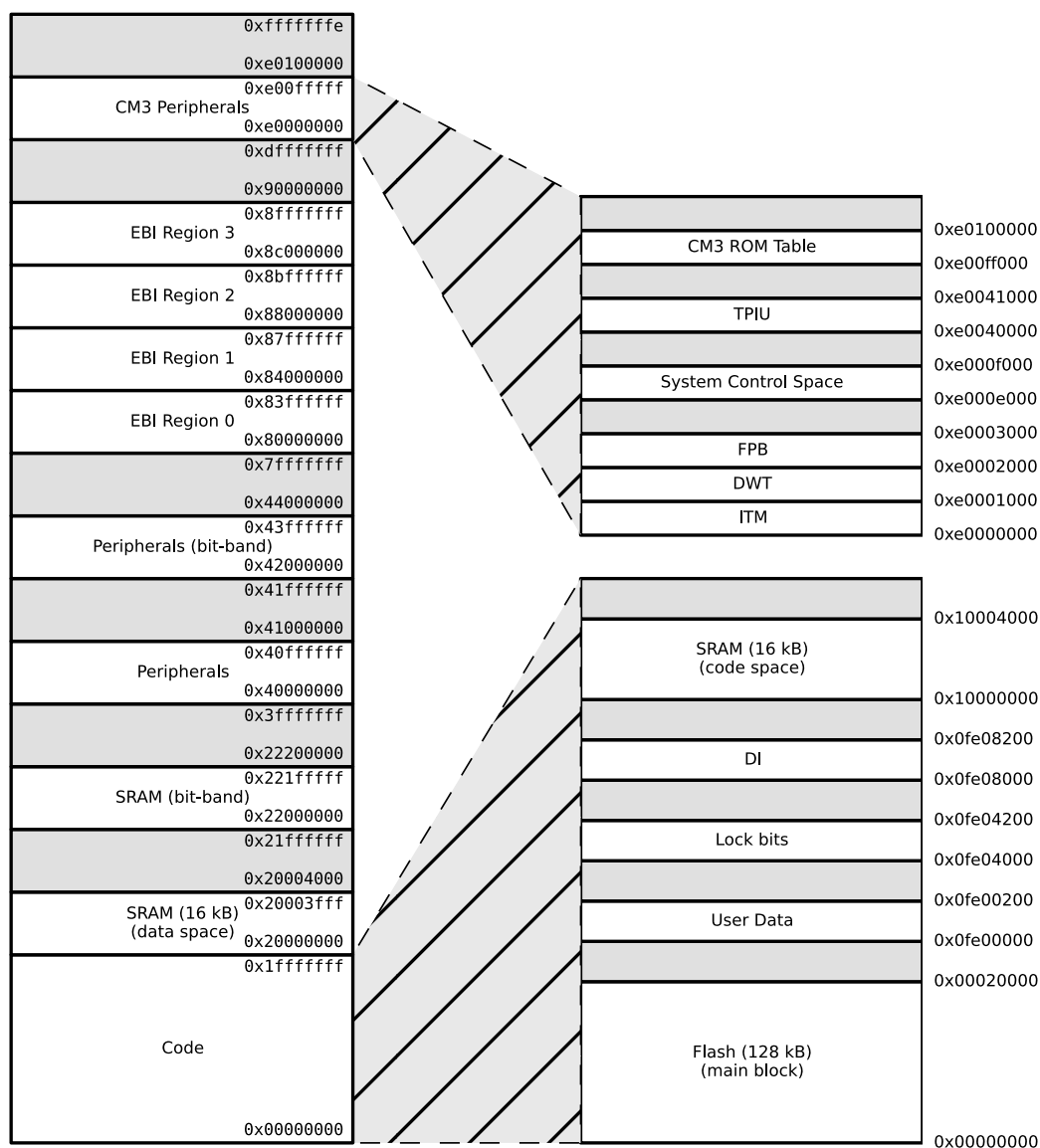
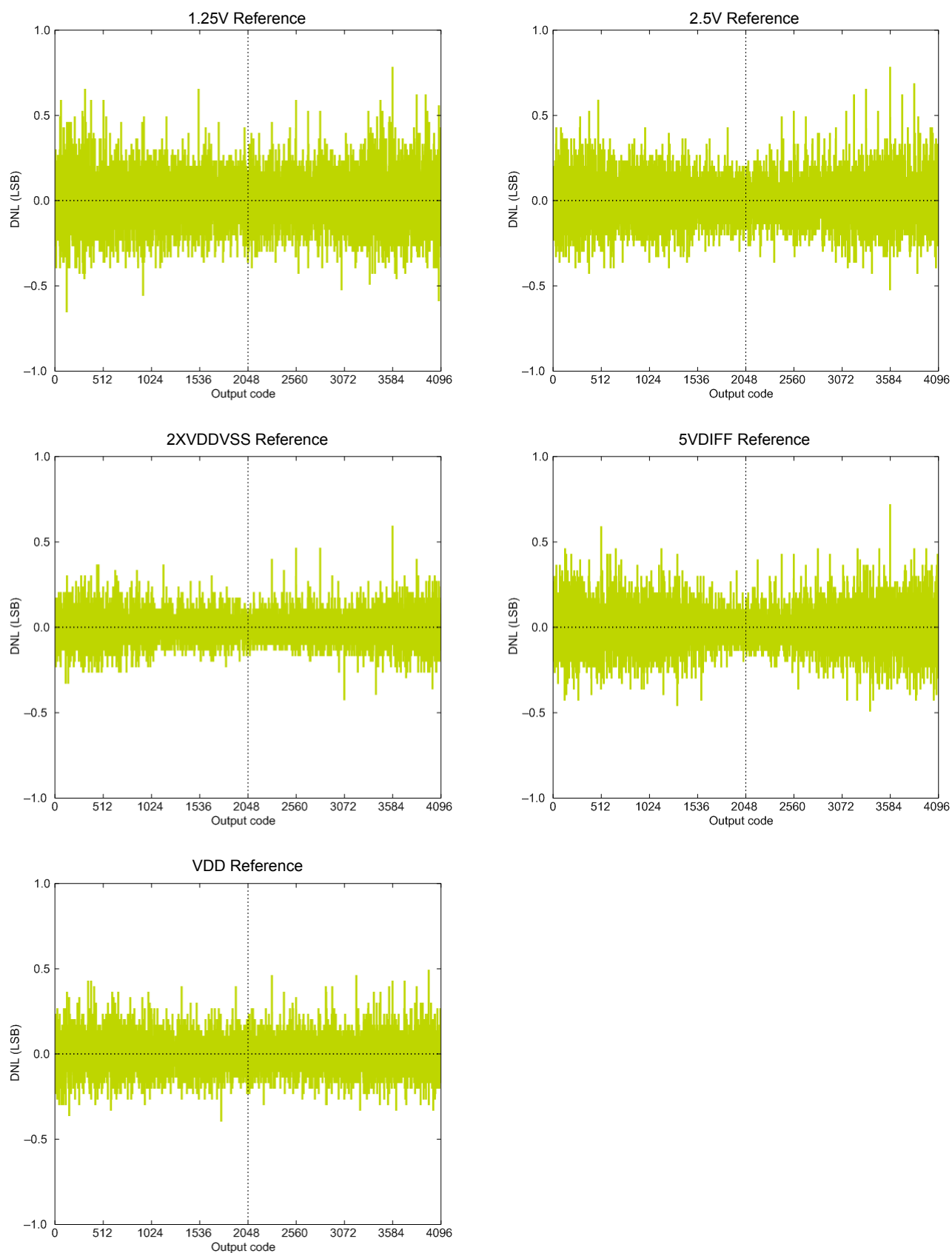


Figure 3.2. System Address Space with Core and Code Space Listing

| Parameter                                                                                                                                    | Symbol         | Test Condition                                                         | Min                 | Typ                  | Max                  | Unit       |
|----------------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------------------------------------------------------------|---------------------|----------------------|----------------------|------------|
| Output low voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD)                                                                | $V_{IOOL}$     | Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST       | —                   | $0.20 \times V_{DD}$ | —                    | V          |
|                                                                                                                                              |                | Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST        | —                   | $0.10 \times V_{DD}$ | —                    | V          |
|                                                                                                                                              |                | Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW            | —                   | $0.10 \times V_{DD}$ | —                    | V          |
|                                                                                                                                              |                | Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW             | —                   | $0.05 \times V_{DD}$ | —                    | V          |
|                                                                                                                                              |                | Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD       | —                   | —                    | $0.30 \times V_{DD}$ | V          |
|                                                                                                                                              |                | Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD        | —                   | —                    | $0.20 \times V_{DD}$ | V          |
|                                                                                                                                              |                | Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH          | —                   | —                    | $0.35 \times V_{DD}$ | V          |
|                                                                                                                                              |                | Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH           | —                   | —                    | $0.25 \times V_{DD}$ | V          |
| Input leakage current                                                                                                                        | $I_{IOLEAK}$   | High Impedance IO connected to GROUND or $V_{DD}$                      | —                   | $\pm 0.1$            | $\pm 40$             | nA         |
| I/O pin pull-up resistor                                                                                                                     | $R_{PU}$       |                                                                        | —                   | 40                   | —                    | k $\Omega$ |
| I/O pin pull-down resistor                                                                                                                   | $R_{PD}$       |                                                                        | —                   | 40                   | —                    | k $\Omega$ |
| Internal ESD series resistor                                                                                                                 | $R_{IOESD}$    |                                                                        | —                   | 200                  | —                    | $\Omega$   |
| Pulse width of pulses to be removed by the glitch suppression filter                                                                         | $t_{IOGLITCH}$ |                                                                        | 10                  | —                    | 50                   | ns         |
| Output fall time                                                                                                                             | $t_{IOOF}$     | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5$ -25pF. | $20+0.1C_L$         | —                    | 250                  | ns         |
|                                                                                                                                              |                | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350$ -600pF     | $20+0.1C_L$         | —                    | 250                  | ns         |
| I/O pin hysteresis ( $V_{IOTHR+}$ - $V_{IOTHR-}$ )                                                                                           | $V_{IOHYST}$   | $V_{DD} = 1.98 - 3.8$ V                                                | $0.1 \times V_{DD}$ | —                    | —                    | V          |
| <b>Note:</b><br>1. If the GPIO input voltage is between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$ , the current consumption will increase. |                |                                                                        |                     |                      |                      |            |

| Parameter                                    | Symbol               | Test Condition                                                                                       | Min | Typ | Max | Unit |
|----------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Signal-to-Noise And Distortion Ratio (SINAD) | SINAD <sub>ADC</sub> | 200 kSamples/s, 12 bit, differential, V <sub>DD</sub> reference, ADC_CLK = 7 MHz, BIASPROG = 0x747   | 62  | 68  | —   | dB   |
|                                              |                      | 200 kSamples/s, 12 bit, differential, 2xV <sub>DD</sub> reference, ADC_CLK = 7 MHz, BIASPROG = 0x747 | —   | 69  | —   | dB   |



**Figure 4.31. ADC Differential Linearity Error vs Code, VDD = 3V, Temp = 25°C**

## 5. Pin Definitions

**Note:** Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32G.

### 5.1 EFM32G200 & EFM32G210 (QFN32)

#### 5.1.1 Pinout

The EFM32G200 and EFM32G210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bit-field in the \*\_ROUTE register in the module in question.

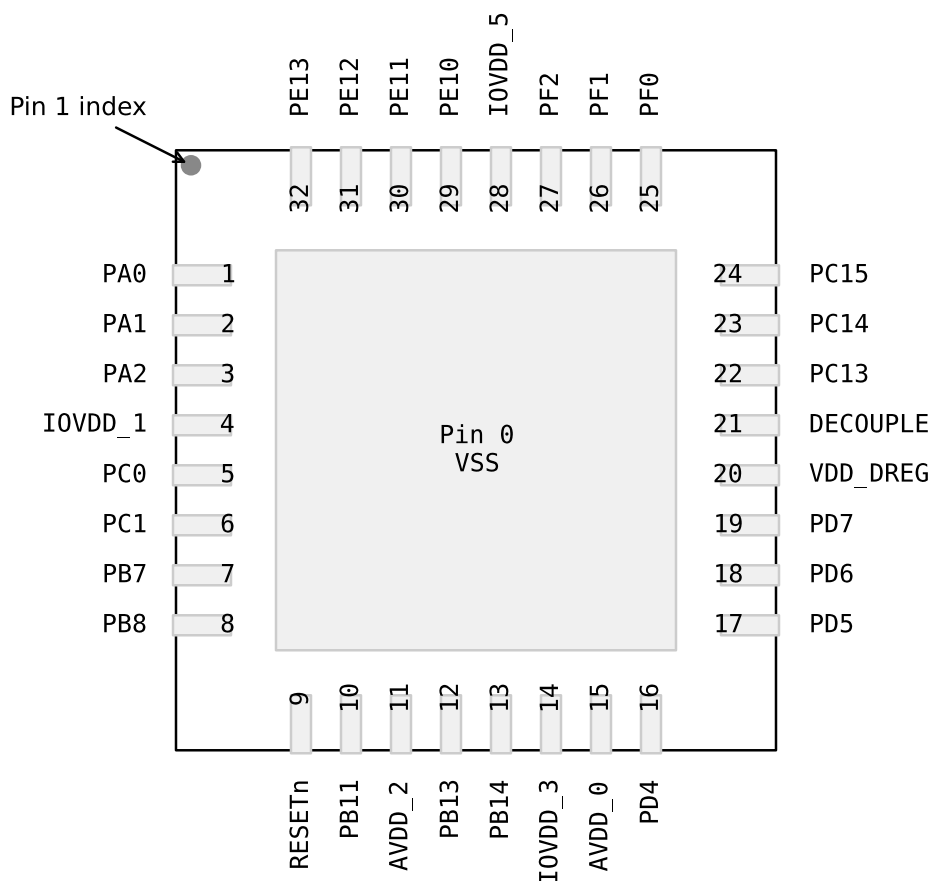


Figure 5.1. EFM32G200 & EFM32G210 Pinout (top view, not to scale)

### 5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G200 and EFM32G210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.3. GPIO Pinout**

| Port   | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | —      | —      | —      | —      | —      | —      | —     | —     | —     | —     | —     | —     | —     | PA2   | PA1   | PA0   |
| Port B | —      | PB14   | PB13   | —      | PB11   | —      | —     | PB8   | PB7   | —     | —     | —     | —     | —     | —     | —     |
| Port C | PC15   | PC14   | PC13   | —      | —      | —      | —     | —     | —     | —     | —     | —     | —     | —     | PC1   | PC0   |
| Port D | —      | —      | —      | —      | —      | —      | —     | —     | PD7   | PD6   | PD5   | PD4   | —     | —     | —     | —     |
| Port E | —      | —      | PE13   | PE12   | PE11   | PE10   | —     | —     | —     | —     | —     | —     | —     | —     | —     | —     |
| Port F | —      | —      | —      | —      | —      | —      | —     | —     | —     | —     | —     | —     | —     | PF2   | PF1   | PF0   |

### 5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.8. Alternate functionality overview**

| Alternate     | LOCATION |      |   |   |                                                           |
|---------------|----------|------|---|---|-----------------------------------------------------------|
| Functionality | 0        | 1    | 2 | 3 | Description                                               |
| ACMP0_CH0     | PC0      |      |   |   | Analog comparator ACMP0, channel 0.                       |
| ACMP0_CH1     | PC1      |      |   |   | Analog comparator ACMP0, channel 1.                       |
| ACMP0_CH2     | PC2      |      |   |   | Analog comparator ACMP0, channel 2.                       |
| ACMP0_CH3     | PC3      |      |   |   | Analog comparator ACMP0, channel 3.                       |
| ACMP0_CH4     | PC4      |      |   |   | Analog comparator ACMP0, channel 4.                       |
| ACMP0_CH5     | PC5      |      |   |   | Analog comparator ACMP0, channel 5.                       |
| ACMP0_CH6     | PC6      |      |   |   | Analog comparator ACMP0, channel 6.                       |
| ACMP0_CH7     | PC7      |      |   |   | Analog comparator ACMP0, channel 7.                       |
| ACMP0_O       | PE13     |      |   |   | Analog comparator ACMP0, digital output.                  |
| ACMP1_CH0     | PC8      |      |   |   | Analog comparator ACMP1, channel 0.                       |
| ACMP1_CH1     | PC9      |      |   |   | Analog comparator ACMP2, channel 1.                       |
| ACMP1_CH2     | PC10     |      |   |   | Analog comparator ACMP3, channel 2.                       |
| ACMP1_CH3     | PC11     |      |   |   | Analog comparator ACMP4, channel 3.                       |
| ACMP1_CH4     | PC12     |      |   |   | Analog comparator ACMP1, channel 4.                       |
| ACMP1_CH5     | PC13     |      |   |   | Analog comparator ACMP1, channel 5.                       |
| ACMP1_CH6     | PC14     |      |   |   | Analog comparator ACMP1, channel 6.                       |
| ACMP1_CH7     | PC15     |      |   |   | Analog comparator ACMP1, channel 7.                       |
| ACMP1_O       | PF2      |      |   |   | Analog comparator ACMP1, digital output.                  |
| ADC0_CH0      | PD0      |      |   |   | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1      | PD1      |      |   |   | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2      | PD2      |      |   |   | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3      | PD3      |      |   |   | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4      | PD4      |      |   |   | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5      | PD5      |      |   |   | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6      | PD6      |      |   |   | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7      | PD7      |      |   |   | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX       | PE11     |      |   |   | Bootloader RX.                                            |
| BOOT_TX       | PE10     |      |   |   | Bootloader TX.                                            |
| CMU_CLK0      | PA2      | PC12 |   |   | Clock Management Unit, clock output number 0.             |
| CMU_CLK1      | PA1      | PD8  |   |   | Clock Management Unit, clock output number 1.             |

## 5.5 EFM32G280 (LQFP100)

### 5.5.1 Pinout

The EFM32G280 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the \*\_ROUTE register in the module in question.

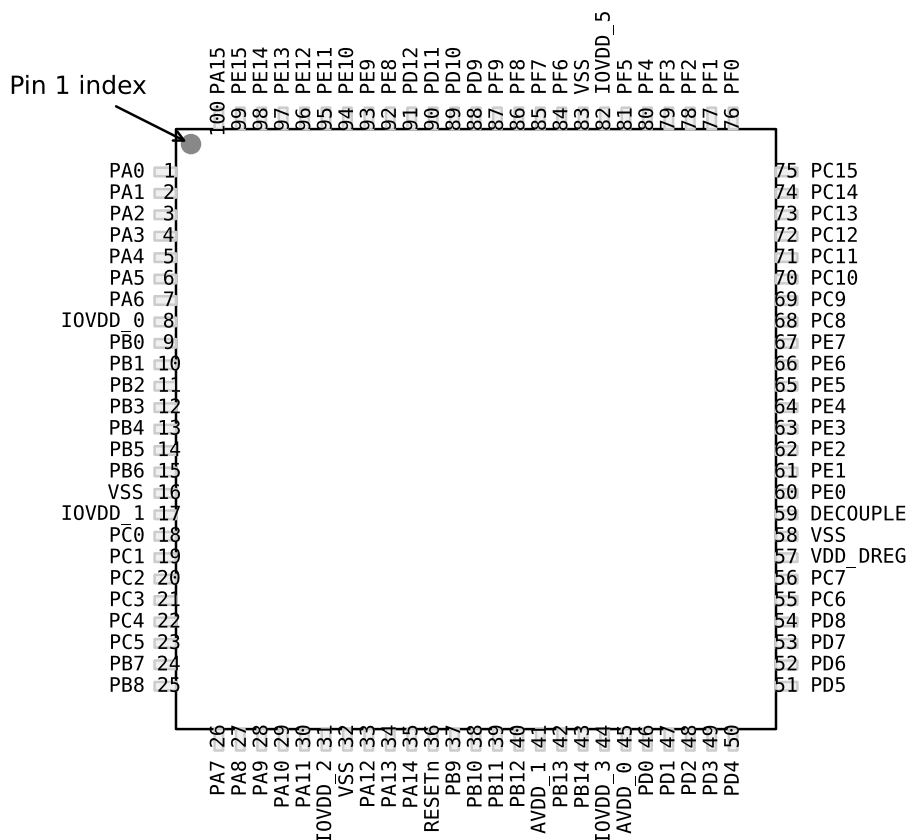


Figure 5.5. EFM32G280 Pinout (top view, not to scale)

Table 5.13. Device Pinout

| LQFP100 Pin# and Name |          | Pin Alternate Functionality / Description |             |               |               |             |
|-----------------------|----------|-------------------------------------------|-------------|---------------|---------------|-------------|
| Pin #                 | Pin Name | Analog                                    | EBI         | Timers        | Communication | Other       |
| 1                     | PA0      |                                           | EBI_AD09 #0 | TIM0_CC0 #0/1 | I2C0_SDA #0   |             |
| 2                     | PA1      |                                           | EBI_AD10 #0 | TIM0_CC1 #0/1 | I2C0_SCL #0   | CMU_CLK1 #0 |
| 3                     | PA2      |                                           | EBI_AD11 #0 | TIM0_CC2 #0/1 |               | CMU_CLK0 #0 |
| 4                     | PA3      |                                           | EBI_AD12 #0 | TIM0_CDTI0 #0 | U0_TX #2      |             |
| 5                     | PA4      |                                           | EBI_AD13 #0 | TIM0_CDTI1 #0 | U0_RX #2      |             |

| Alternate     | LOCATION |      |   |   |                                                                                                                                               |
|---------------|----------|------|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Functionality | 0        | 1    | 2 | 3 | Description                                                                                                                                   |
| DAC0_OUT0     | PB11     |      |   |   | Digital to Analog Converter DAC0 output channel number 0.                                                                                     |
| DAC0_OUT1     | PB12     |      |   |   | Digital to Analog Converter DAC0 output channel number 1.                                                                                     |
| DBG_SWCLK     | PF0      | PF0  |   |   | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down.             |
| DBG_SWDIO     | PF1      | PF1  |   |   | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up.       |
| DBG_SWO       | PF2      | PC15 |   |   | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_AD00      | PE8      |      |   |   | External Bus Interface (EBI) address and data input / output pin 00.                                                                          |
| EBI_AD01      | PE9      |      |   |   | External Bus Interface (EBI) address and data input / output pin 01.                                                                          |
| EBI_AD02      | PE10     |      |   |   | External Bus Interface (EBI) address and data input / output pin 02.                                                                          |
| EBI_AD03      | PE11     |      |   |   | External Bus Interface (EBI) address and data input / output pin 03.                                                                          |
| EBI_AD04      | PE12     |      |   |   | External Bus Interface (EBI) address and data input / output pin 04.                                                                          |
| EBI_AD05      | PE13     |      |   |   | External Bus Interface (EBI) address and data input / output pin 05.                                                                          |
| EBI_AD06      | PE14     |      |   |   | External Bus Interface (EBI) address and data input / output pin 06.                                                                          |
| EBI_AD07      | PE15     |      |   |   | External Bus Interface (EBI) address and data input / output pin 07.                                                                          |
| EBI_AD08      | PA15     |      |   |   | External Bus Interface (EBI) address and data input / output pin 08.                                                                          |
| EBI_AD09      | PA0      |      |   |   | External Bus Interface (EBI) address and data input / output pin 09.                                                                          |
| EBI_AD10      | PA1      |      |   |   | External Bus Interface (EBI) address and data input / output pin 10.                                                                          |
| EBI_AD11      | PA2      |      |   |   | External Bus Interface (EBI) address and data input / output pin 11.                                                                          |
| EBI_AD12      | PA3      |      |   |   | External Bus Interface (EBI) address and data input / output pin 12.                                                                          |
| EBI_AD13      | PA4      |      |   |   | External Bus Interface (EBI) address and data input / output pin 13.                                                                          |
| EBI_AD14      | PA5      |      |   |   | External Bus Interface (EBI) address and data input / output pin 14.                                                                          |
| EBI_AD15      | PA6      |      |   |   | External Bus Interface (EBI) address and data input / output pin 15.                                                                          |
| EBI_ALE       | PF3      |      |   |   | External Bus Interface (EBI) Address Latch Enable output.                                                                                     |

### 5.7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.20. Alternate functionality overview**

| Alternate     | LOCATION |      |   |   |                                                                                                                                         |
|---------------|----------|------|---|---|-----------------------------------------------------------------------------------------------------------------------------------------|
| Functionality | 0        | 1    | 2 | 3 | Description                                                                                                                             |
| ACMP0_CH4     | PC4      |      |   |   | Analog comparator ACMP0, channel 4.                                                                                                     |
| ACMP0_CH5     | PC5      |      |   |   | Analog comparator ACMP0, channel 5.                                                                                                     |
| ACMP0_CH6     | PC6      |      |   |   | Analog comparator ACMP0, channel 6.                                                                                                     |
| ACMP0_CH7     | PC7      |      |   |   | Analog comparator ACMP0, channel 7.                                                                                                     |
| ACMP0_O       | PE13     |      |   |   | Analog comparator ACMP0, digital output.                                                                                                |
| ACMP1_CH4     | PC12     |      |   |   | Analog comparator ACMP1, channel 4.                                                                                                     |
| ACMP1_CH5     | PC13     |      |   |   | Analog comparator ACMP1, channel 5.                                                                                                     |
| ACMP1_CH6     | PC14     |      |   |   | Analog comparator ACMP1, channel 6.                                                                                                     |
| ACMP1_CH7     | PC15     |      |   |   | Analog comparator ACMP1, channel 7.                                                                                                     |
| ACMP1_O       | PF2      |      |   |   | Analog comparator ACMP1, digital output.                                                                                                |
| ADC0_CH0      | PD0      |      |   |   | Analog to digital converter ADC0, input channel number 0.                                                                               |
| ADC0_CH1      | PD1      |      |   |   | Analog to digital converter ADC0, input channel number 1.                                                                               |
| ADC0_CH2      | PD2      |      |   |   | Analog to digital converter ADC0, input channel number 2.                                                                               |
| ADC0_CH3      | PD3      |      |   |   | Analog to digital converter ADC0, input channel number 3.                                                                               |
| ADC0_CH4      | PD4      |      |   |   | Analog to digital converter ADC0, input channel number 4.                                                                               |
| ADC0_CH5      | PD5      |      |   |   | Analog to digital converter ADC0, input channel number 5.                                                                               |
| ADC0_CH6      | PD6      |      |   |   | Analog to digital converter ADC0, input channel number 6.                                                                               |
| ADC0_CH7      | PD7      |      |   |   | Analog to digital converter ADC0, input channel number 7.                                                                               |
| BOOT_RX       | PE11     |      |   |   | Bootloader RX.                                                                                                                          |
| BOOT_TX       | PE10     |      |   |   | Bootloader TX.                                                                                                                          |
| CMU_CLK0      | PA2      | PC12 |   |   | Clock Management Unit, clock output number 0.                                                                                           |
| CMU_CLK1      | PA1      | PD8  |   |   | Clock Management Unit, clock output number 1.                                                                                           |
| DAC0_OUT0     | PB11     |      |   |   | Digital to Analog Converter DAC0 output channel number 0.                                                                               |
| DAC0_OUT1     | PB12     |      |   |   | Digital to Analog Converter DAC0 output channel number 1.                                                                               |
| DBG_SWCLK     | PF0      | PF0  |   |   | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down.       |
| DBG_SWDIO     | PF1      | PF1  |   |   | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| LQFP100 Pin# and Name |          | Pin Alternate Functionality / Description |             |                |               |                          |
|-----------------------|----------|-------------------------------------------|-------------|----------------|---------------|--------------------------|
| Pin #                 | Pin Name | Analog                                    | EBI         | Timers         | Communication | Other                    |
| 77                    | PF1      |                                           |             | LETIM0_OUT1 #2 |               | DBG_SWDIO #0/1           |
| 78                    | PF2      | LCD_SEG<br>0                              | EBI_ARDY #0 |                |               | ACMP1_O #0<br>DBG_SWO #0 |
| 79                    | PF3      | LCD_SEG<br>1                              | EBI_ALE #0  | TIM0_CDT10 #2  |               |                          |
| 80                    | PF4      | LCD_SEG<br>2                              | EBI_WEn #0  | TIM0_CDT11 #2  |               |                          |
| 81                    | PF5      | LCD_SEG<br>3                              | EBI_REn #0  | TIM0_CDT12 #2  |               |                          |
| 82                    | IOVDD_5  | Digital IO power supply 5.                |             |                |               |                          |
| 83                    | VSS      | Ground.                                   |             |                |               |                          |
| 84                    | PF6      | LCD_SEG<br>24                             |             | TIM0_CC0 #2    | U0_TX #0      |                          |
| 85                    | PF7      | LCD_SEG<br>25                             |             | TIM0_CC1 #2    | U0_RX #0      |                          |
| 86                    | PF8      | LCD_SEG<br>26                             |             | TIM0_CC2 #2    |               |                          |
| 87                    | PF9      | LCD_SEG<br>27                             |             |                |               |                          |
| 88                    | PD9      | LCD_SEG<br>28                             | EBI_CS0 #0  |                |               |                          |
| 89                    | PD10     | LCD_SEG<br>29                             | EBI_CS1 #0  |                |               |                          |
| 90                    | PD11     | LCD_SEG<br>30                             | EBI_CS2 #0  |                |               |                          |
| 91                    | PD12     | LCD_SEG<br>31                             | EBI_CS3 #0  |                |               |                          |
| 92                    | PE8      | LCD_SEG<br>4                              | EBI_AD00 #0 | PCNT2_S0IN #1  |               |                          |
| 93                    | PE9      | LCD_SEG<br>5                              | EBI_AD01 #0 | PCNT2_S1IN #1  |               |                          |
| 94                    | PE10     | LCD_SEG<br>6                              | EBI_AD02 #0 | TIM1_CC0 #1    | US0_TX #0     | BOOT_TX                  |
| 95                    | PE11     | LCD_SEG<br>7                              | EBI_AD03 #0 | TIM1_CC1 #1    | US0_RX #0     | BOOT_RX                  |
| 96                    | PE12     | LCD_SEG<br>8                              | EBI_AD04 #0 | TIM1_CC2 #1    | US0_CLK #0    |                          |
| 97                    | PE13     | LCD_SEG<br>9                              | EBI_AD05 #0 |                | US0_CS #0     | ACMP0_O #0               |
| 98                    | PE14     | LCD_SEG<br>10                             | EBI_AD06 #0 |                | LEU0_TX #2    |                          |
| 99                    | PE15     | LCD_SEG<br>11                             | EBI_AD07 #0 |                | LEU0_RX #2    |                          |

## 5.9.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.26. Alternate functionality overview**

| Alternate     | LOCATION |      |   |   |                                                           |
|---------------|----------|------|---|---|-----------------------------------------------------------|
| Functionality | 0        | 1    | 2 | 3 | Description                                               |
| ACMP0_CH0     | PC0      |      |   |   | Analog comparator ACMP0, channel 0.                       |
| ACMP0_CH1     | PC1      |      |   |   | Analog comparator ACMP0, channel 1.                       |
| ACMP0_CH2     | PC2      |      |   |   | Analog comparator ACMP0, channel 2.                       |
| ACMP0_CH3     | PC3      |      |   |   | Analog comparator ACMP0, channel 3.                       |
| ACMP0_CH4     | PC4      |      |   |   | Analog comparator ACMP0, channel 4.                       |
| ACMP0_CH5     | PC5      |      |   |   | Analog comparator ACMP0, channel 5.                       |
| ACMP0_CH6     | PC6      |      |   |   | Analog comparator ACMP0, channel 6.                       |
| ACMP0_CH7     | PC7      |      |   |   | Analog comparator ACMP0, channel 7.                       |
| ACMP0_O       | PE13     | PE2  |   |   | Analog comparator ACMP0, digital output.                  |
| ACMP1_CH0     | PC8      |      |   |   | Analog comparator ACMP1, channel 0.                       |
| ACMP1_CH1     | PC9      |      |   |   | Analog comparator ACMP1, channel 1.                       |
| ACMP1_CH2     | PC10     |      |   |   | Analog comparator ACMP1, channel 2.                       |
| ACMP1_CH3     | PC11     |      |   |   | Analog comparator ACMP1, channel 3.                       |
| ACMP1_CH4     | PC12     |      |   |   | Analog comparator ACMP1, channel 4.                       |
| ACMP1_CH5     | PC13     |      |   |   | Analog comparator ACMP1, channel 5.                       |
| ACMP1_CH6     | PC14     |      |   |   | Analog comparator ACMP1, channel 6.                       |
| ACMP1_CH7     | PC15     |      |   |   | Analog comparator ACMP1, channel 7.                       |
| ACMP1_O       | PF2      | PE3  |   |   | Analog comparator ACMP1, digital output.                  |
| ADC0_CH0      | PD0      |      |   |   | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1      | PD1      |      |   |   | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2      | PD2      |      |   |   | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3      | PD3      |      |   |   | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4      | PD4      |      |   |   | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5      | PD5      |      |   |   | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6      | PD6      |      |   |   | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7      | PD7      |      |   |   | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX       | PE11     |      |   |   | Bootloader RX.                                            |
| BOOT_TX       | PE10     |      |   |   | Bootloader TX.                                            |
| CMU_CLK0      | PA2      | PC12 |   |   | Clock Management Unit, clock output number 0.             |
| CMU_CLK1      | PA1      | PD8  |   |   | Clock Management Unit, clock output number 1.             |

| Alternate     | LOCATION |      |      |      |                                                                                                                                                       |
|---------------|----------|------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| Functionality | 0        | 1    | 2    | 3    | Description                                                                                                                                           |
| TIM0_CDTI1    | PA4      | PC14 | PF4  | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1.                                                                                                  |
| TIM0_CDTI2    | PA5      | PC15 | PF5  | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2.                                                                                                  |
| TIM1_CC0      | PC13     | PE10 | PB0  |      | Timer 1 Capture Compare input / output channel 0.                                                                                                     |
| TIM1_CC1      | PC14     | PE11 | PB1  |      | Timer 1 Capture Compare input / output channel 1.                                                                                                     |
| TIM1_CC2      | PC15     | PE12 | PB2  |      | Timer 1 Capture Compare input / output channel 2.                                                                                                     |
| TIM2_CC0      | PA8      | PA12 | PC8  |      | Timer 2 Capture Compare input / output channel 0.                                                                                                     |
| TIM2_CC1      | PA9      | PA13 | PC9  |      | Timer 2 Capture Compare input / output channel 1.                                                                                                     |
| TIM2_CC2      | PA10     | PA14 | PC10 |      | Timer 2 Capture Compare input / output channel 2.                                                                                                     |
| U0_RX         | PF7      | PE1  | PA4  | PC15 | UART0 Receive input.                                                                                                                                  |
| U0_TX         | PF6      | PE0  | PA3  | PC14 | UART0 Transmit output. Also used as receive input in half duplex communication.                                                                       |
| US0_CLK       | PE12     | PE5  | PC9  |      | USART0 clock input / output.                                                                                                                          |
| US0_CS        | PE13     | PE4  | PC8  |      | USART0 chip select input / output.                                                                                                                    |
| US0_RX        | PE11     | PE6  | PC10 |      | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MI-SO).                                                          |
| US0_TX        | PE10     | PE7  | PC11 |      | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK       | PB7      | PD2  |      |      | USART1 clock input / output.                                                                                                                          |
| US1_CS        | PB8      | PD3  |      |      | USART1 chip select input / output.                                                                                                                    |
| US1_RX        | PC1      | PD1  |      |      | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MI-SO).                                                          |
| US1_TX        | PC0      | PD0  |      |      | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK       | PC4      | PB5  |      |      | USART2 clock input / output.                                                                                                                          |
| US2_CS        | PC5      | PB6  |      |      | USART2 chip select input / output.                                                                                                                    |
| US2_RX        | PC3      | PB4  |      |      | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MI-SO).                                                          |
| US2_TX        | PC2      | PB3  |      |      | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

| BGA112 Pin# and Name |               | Pin Alternate Functionality / Description                                                                                     |     |               |                           |             |
|----------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------|-----|---------------|---------------------------|-------------|
| Pin #                | Pin Name      | Analog                                                                                                                        | EBI | Timers        | Communication             | Other       |
| E9                   | PE0           |                                                                                                                               |     | PCNT0_S0IN #1 | U0_TX #1                  |             |
| E10                  | PE1           |                                                                                                                               |     | PCNT0_S1IN #1 | U0_RX #1                  |             |
| E11                  | PE3           |                                                                                                                               |     |               |                           | ACMP1_O #1  |
| F1                   | PB1           | LCD_SEG 33                                                                                                                    |     | TIM1_CC1 #2   |                           |             |
| F2                   | PB2           | LCD_SEG 34                                                                                                                    |     | TIM1_CC2 #2   |                           |             |
| F3                   | PB3           | LCD_SEG 20                                                                                                                    |     | PCNT1_S0IN #1 | US2_TX #1                 |             |
| F4                   | PB4           | LCD_SEG 21                                                                                                                    |     | PCNT1_S1IN #1 | US2_RX #1                 |             |
| F8                   | VDD_DRE<br>G  | Power supply for on-chip voltage regulator.                                                                                   |     |               |                           |             |
| F9                   | VSS_DRE<br>G  | Ground for on-chip voltage regulator.                                                                                         |     |               |                           |             |
| F10                  | PE2           |                                                                                                                               |     |               |                           | ACMP0_O #1  |
| F11                  | DECOU-<br>PLE | Decouple output for on-chip voltage regulator. An external capacitance of size C <sub>DECOUPLE</sub> is required at this pin. |     |               |                           |             |
| G1                   | PB5           | LCD_SEG 22                                                                                                                    |     |               | US2_CLK #1                |             |
| G2                   | PB6           | LCD_SEG 23                                                                                                                    |     |               | US2_CS #1                 |             |
| G3                   | VSS           | Ground.                                                                                                                       |     |               |                           |             |
| G4                   | IOVDD_0       | Digital IO power supply 0.                                                                                                    |     |               |                           |             |
| G8                   | IOVDD_4       | Digital IO power supply 4.                                                                                                    |     |               |                           |             |
| G9                   | VSS           | Ground.                                                                                                                       |     |               |                           |             |
| G10                  | PC6           | ACMP0_C<br>H6                                                                                                                 |     |               | LEU1_TX #0<br>I2C0_SDA #2 |             |
| G11                  | PC7           | ACMP0_C<br>H7                                                                                                                 |     |               | LEU1_RX #0<br>I2C0_SCL #2 |             |
| H1                   | PC0           | ACMP0_C<br>H0                                                                                                                 |     | PCNT0_S0IN #2 | US1_TX #0                 |             |
| H2                   | PC2           | ACMP0_C<br>H2                                                                                                                 |     |               | US2_TX #0                 |             |
| H3                   | PD14          |                                                                                                                               |     |               | I2C0_SDA #3               |             |
| H4                   | PA7           | LCD_SEG 35                                                                                                                    |     |               |                           |             |
| H5                   | PA8           | LCD_SEG 36                                                                                                                    |     | TIM2_CC0 #0   |                           |             |
| H6                   | VSS           | Ground.                                                                                                                       |     |               |                           |             |
| H7                   | IOVDD_3       | Digital IO power supply 3.                                                                                                    |     |               |                           |             |
| H8                   | PD8           |                                                                                                                               |     |               |                           | CMU_CLK1 #1 |

## 6. BGA112 Package Specifications

### 6.1 BGA112 Package Dimensions

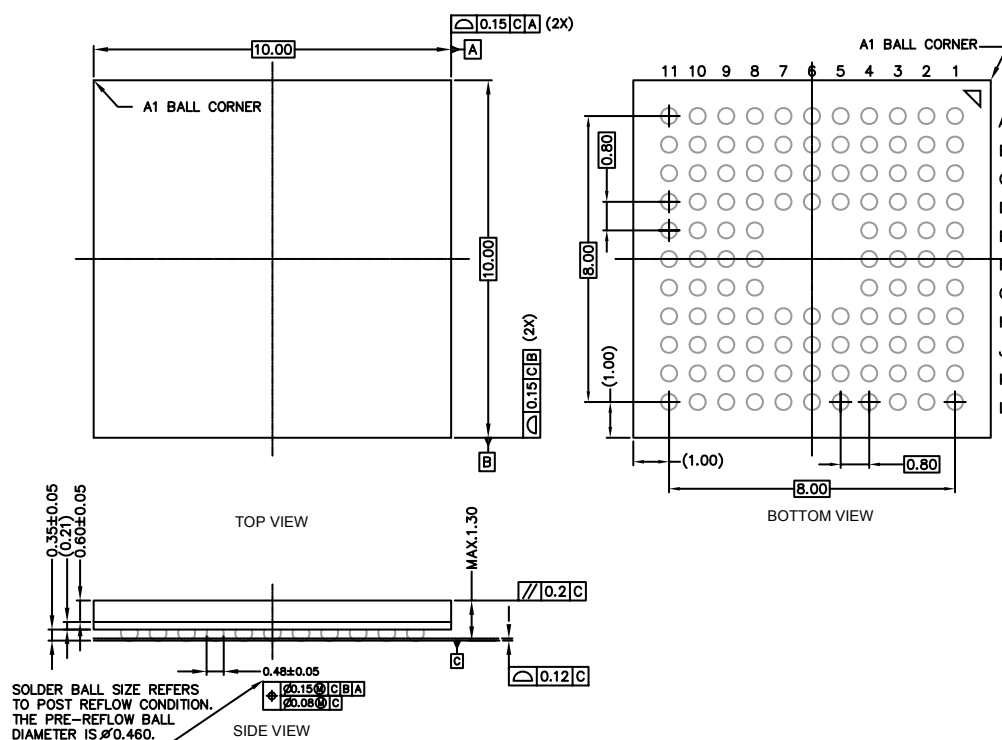


Figure 6.1. BGA112

**Note:**

1. The dimensions in parenthesis are reference.
2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

The BGA112 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

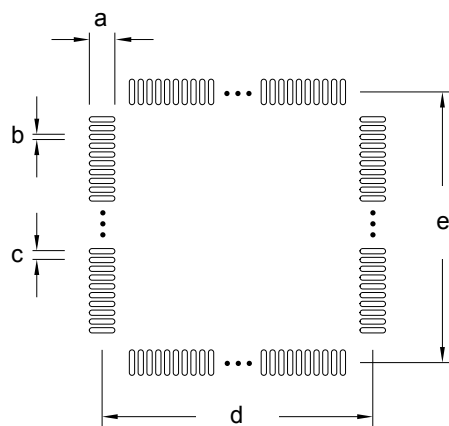


Figure 9.4. TQFP48 PCB Stencil Design

Table 9.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a      | 1.50      |
| b      | 0.20      |
| c      | 0.50      |
| d      | 8.50      |
| e      | 8.50      |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see [5. Pin Definitions](#).

## 12. Chip Revision, Solder Information, Errata

### 12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

### 12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

### 12.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and on-line at: <http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>