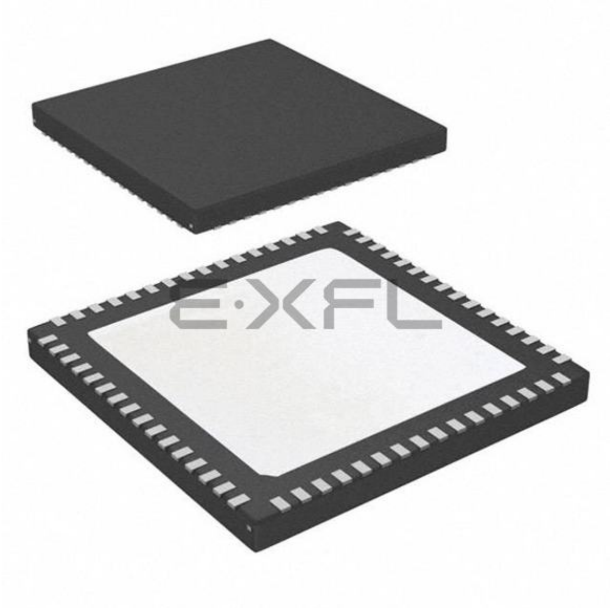

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g230f128g-e-qfn64r

1. Feature List

- ARM Cortex-M3 CPU platform
  - High Performance 32-bit processor @ up to 32 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
  - SysTick System Timer
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 μA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 μA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 μA/MHz @ 3 V Sleep Mode
  - 180 μA/MHz @ 3 V Run Mode, with code executed from flash
- 128/64/32 KB Flash
- 16/8 KB RAM
- Up to 90 General Purpose I/O pins
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- 8 Channel DMA Controller
- 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware AES with 128/256-bit keys in 54/75 cycles
- Timers/Counters
  - 3 × 16-bit Timer/Counter
    - 3×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 1× 24-bit Real-Time Counter
  - 3× 8-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Integrated LCD Controller for up to 4×40 segments
  - Voltage boost, adjustable contrast and autonomous animation
- External Bus Interface for up to 4x64 MB of external memory mapped space
  - TFT Controller with Direct Drive
- Communication interfaces
  - Up to 3× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - 1× Universal Asynchronous Receiver/Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single-ended channels/4 differential channels
    - On-chip temperature sensor
  - 12-bit 500 ksamples/s Digital to Analog Converter
    - 2 single-ended channels/1 differential channel
  - 2× Analog Comparator
    - Capacitive sensing with up to 16 inputs

3.2.5 EFM32G232

The features of the EFM32G232 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.5. EFM32G232 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[15:8], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[0]
AES	Full configuration	NA
GPIO	53 pins	Available pins are shown in Table 4.3 (p. 57)

3.2.6 EFM32G280

The features of the EFM32G280 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.6. EFM32G280 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	86 pins	Available pins are shown in Table 4.3 (p. 57)

4.4.1 EM0 Current Consumption

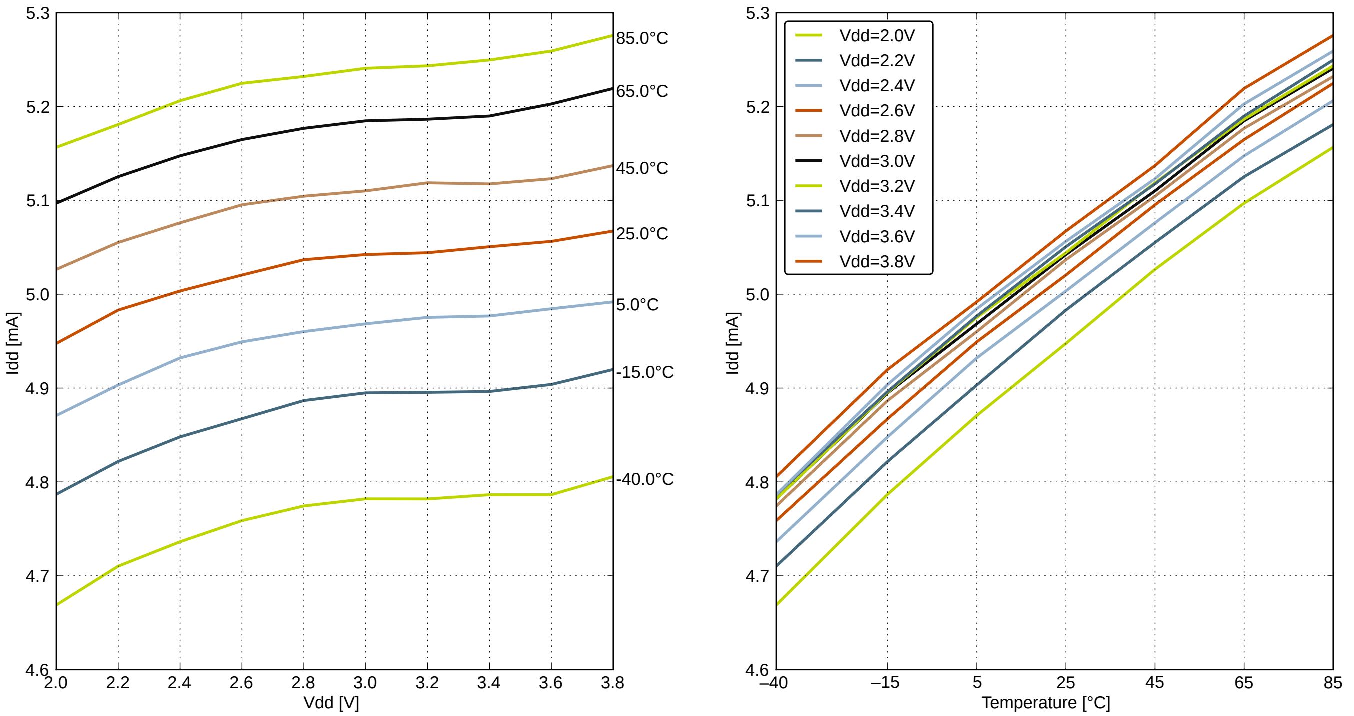

Figure 4.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28 MHz

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	$0.30 \times V_{DD}$[1]	V
Input high voltage	V_{IOIH}		$0.70 \times V_{DD}$[1]	—	—	V
Output high voltage (Production test condition = 3.0 V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.80 \times V_{DD}$	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	$0.90 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.85 \times V_{DD}$	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.90 \times V_{DD}$	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75 \times V_{DD}$	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60 \times V_{DD}$	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80 \times V_{DD}$	—	—	V

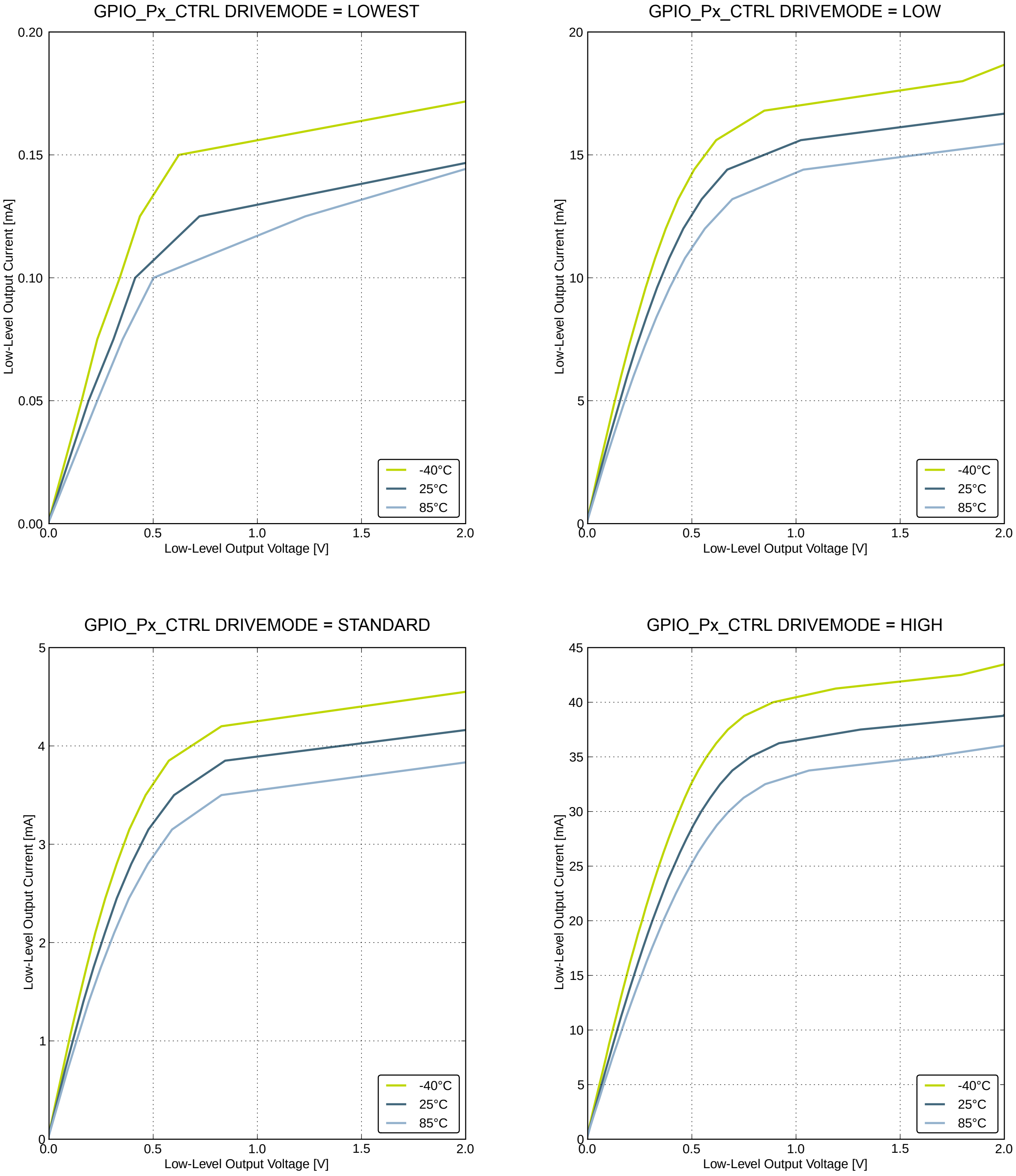

Figure 4.14. Typical Low-Level Output Current, 2V Supply Voltage

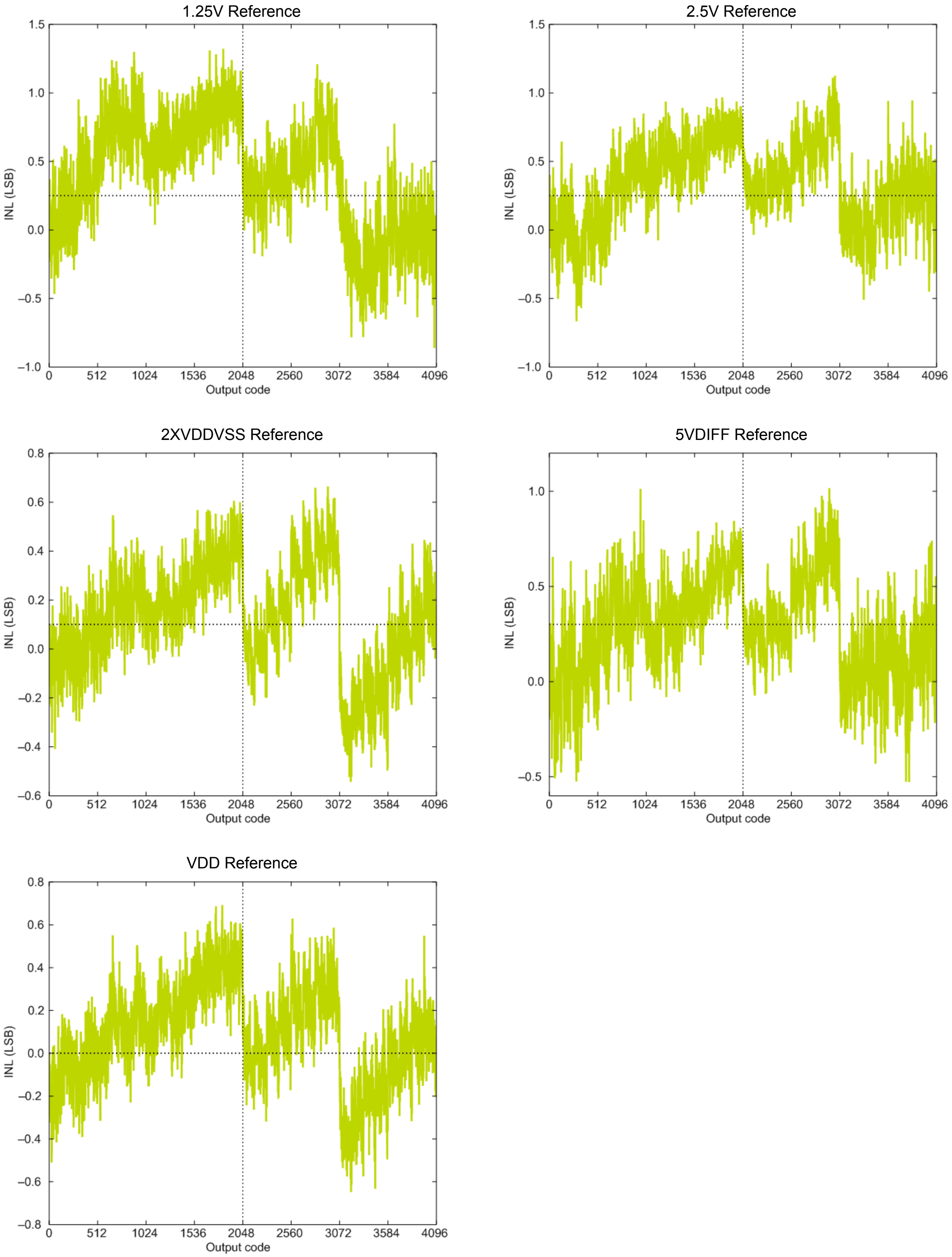

Figure 4.30. ADC Integral Linearity Error vs Code, VDD = 3V, Temp = 25°C

Table 4.21. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000[1]	kHz
SCL clock low time	t_{LOW}	0.5	—	—	µs
SCL clock high time	t_{HIGH}	0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	µs

Note:

1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

4.16 Digital Peripherals

Table 4.22. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	µA/MHz
UART current	I_{UART}	UART idle current, clock enabled	—	5.63	—	µA/MHz
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	µA/MHz
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	µA/MHz
LETIMER current	$I_{LETIMER}$	LETIMER idle current, clock enabled	—	150	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
LCD current	I_{LCD}	LCD idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	µA/MHz
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	µA/MHz
EBI current	I_{EBI}	EBI idle current, clock enabled	—	1.56	—	µA/MHz
PRS current	I_{PRS}	PRS idle current	—	2.81	—	µA/MHz
DMA current	I_{DMA}	Clock enable	—	8.12	—	µA/MHz

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" forguidelines on designing Printed Circuit Boards (PCB's) for the EFM32G.

5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.2. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1				Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0		Low Energy Timer LETIM0, output channel 0.

5.2 EFM32G222 (TQFP48)

5.2.1 Pinout

The EFM32G222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

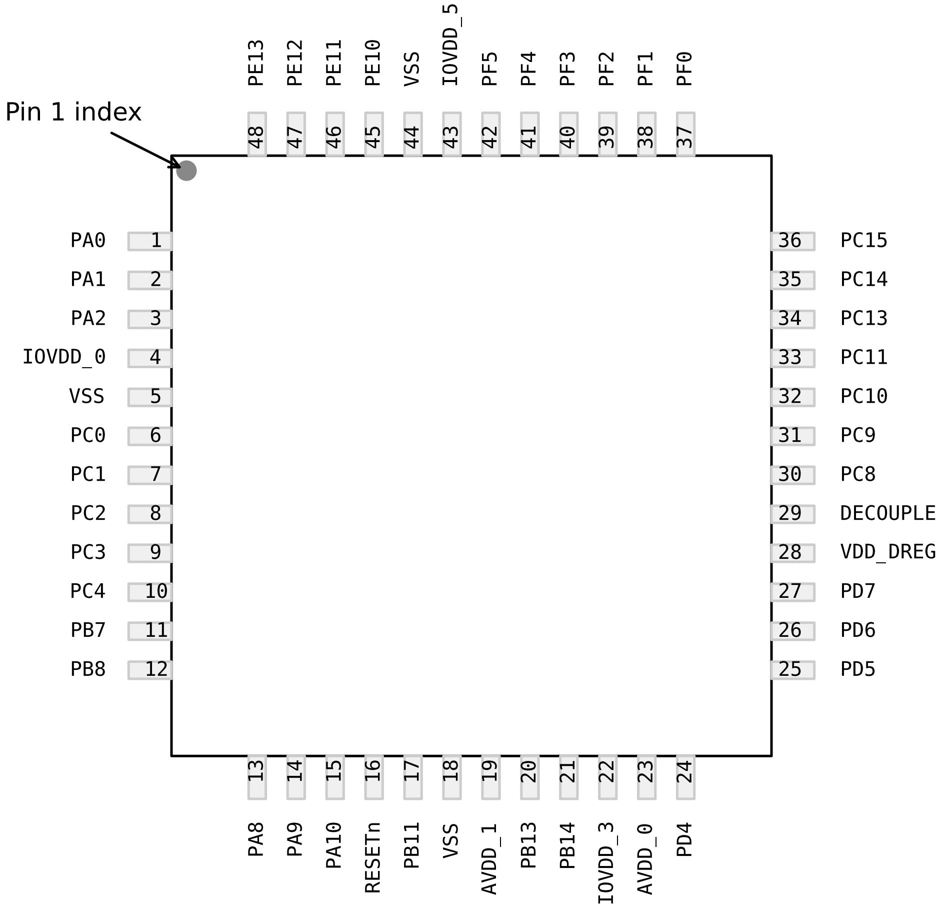

Figure 5.2. EFM32G222 Pinout (top view, not to scale)

Table 5.4. Device Pinout

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_0	Digital IO power supply 0.			
5	VSS	Ground.			

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
G10	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
G11	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
H1	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
H2	PC2	ACMP0_CH2			US2_TX #0	
H3	PD14				I2C0_SDA #3	
H4	PA7					
H5	PA8			TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8					CMU_CLK1 #1
H9	PD5	ADC0_CH5			LEU0_RX #0	
H10	PD6	ADC0_CH6		LETIM0_OUT0 #0	I2C0_SDA #1	
H11	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
J1	PC1	ACMP0_CH1		PCNT0_S1IN #2	US1_RX #0	
J2	PC3	ACMP0_CH3			US2_RX #0	
J3	PD15				I2C0_SCL #3	
J4	PA12			TIM2_CC0 #1		
J5	PA9			TIM2_CC1 #0		
J6	PA10			TIM2_CC2 #0		
J7	PB9					
J8	PB10					
J9	PD2	ADC0_CH2		TIM0_CC1 #3	US1_CLK #1	
J10	PD3	ADC0_CH3		TIM0_CC2 #3	US1_CS #1	
J11	PD4	ADC0_CH4			LEU0_TX #0	
K1	PB7	LFXTAL_P			US1_CLK #0	
K2	PC4	ACMP0_CH4		LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
K3	PA13			TIM2_CC1 #1		
K4	VSS	Ground.				

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	**Pin Name**	**Analog**	**Timers**	**Communication**	**Other**
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2	LCD_SEG0			ACMP1_O #0 DBG_SWO #0
52	PF3	LCD_SEG1	TIM0_CDTI0 #2		
53	PF4	LCD_SEG2	TIM0_CDTI1 #2		
54	PF5	LCD_SEG3	TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8	LCD_SEG4	PCNT2_S0IN #1		
58	PE9	LCD_SEG5	PCNT2_S1IN #1		
59	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	BOOT_RX
61	PE12	LCD_SEG8	TIM1_CC2 #1	US0_CLK #0	
62	PE13	LCD_SEG9		US0_CS #0	ACMP0_O #0
63	PE14	LCD_SEG10		LEU0_TX #2	
64	PE15	LCD_SEG11		LEU0_RX #2	

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C3	PE10	LCD_SEG6	EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					
C5	PD12	LCD_SEG31	EBI_CS3 #0			
C6	PF9	LCD_SEG27				
C7	VSS	Ground.				
C8	PF2	LCD_SEG0	EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6	LCD_COM2			US0_RX #1	
C10	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_CH3			US0_TX #2	
D1	PA3	LCD_SEG16	EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2	LCD_SEG15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
D3	PB15					
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG28	EBI_CS0 #0			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7	LCD_COM3			US0_TX #1	
D10	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6	LCD_SEG19	EBI_AD15 #0		LEU1_RX #1	
E2	PA5	LCD_SEG18	EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4	LCD_SEG17	EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0	LCD_SEG32		TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1

Alternate	LOCATION				
Functionality	0	1	2	3	Description
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LCD_BCAP_N	PA13				LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12				LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14				LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4				LCD driver common line number 0.
LCD_COM1	PE5				LCD driver common line number 1.
LCD_COM2	PE6				LCD driver common line number 2.
LCD_COM3	PE7				LCD driver common line number 3.
LCD_SEG0	PF2				LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3				LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4				LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5				LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8				LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9				LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10				LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.

7. LQFP100 Package Specifications

7.1 LQFP100 Package Dimensions

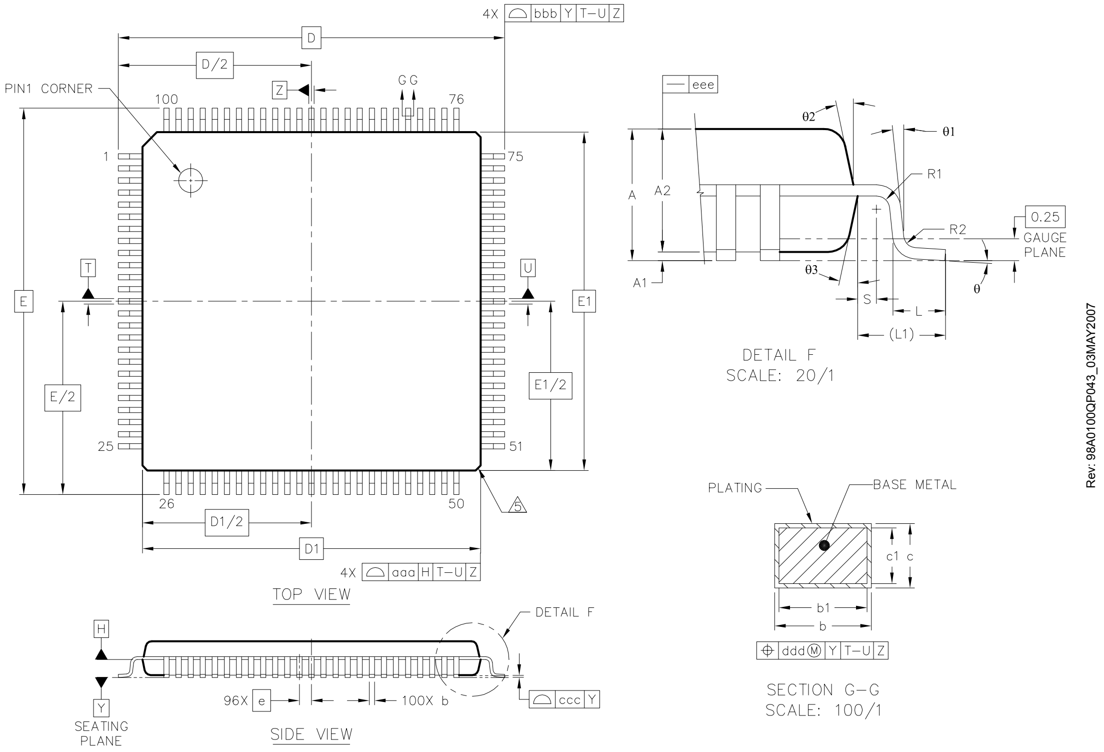

Figure 7.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause thelead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be locatedon the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 7.1. LQFP100 (Dimensions in mm)

	SYMBOL	MIN	NOM	MAX
total thickness	A	—	—	1.6
stand off	A1	0.05	—	0.15
mold thickness	A2	1.35	1.4	1.45
lead width (plating)	b	0.17	0.2	0.27
lead width	b1	0.17	—	0.23
L/F thickness (plating)	c	0.09	—	0.2
lead thickness	c1	0.09	—	0.16

7.3 LQFP100 Package Marking

In the illustration below package fields and position are shown.

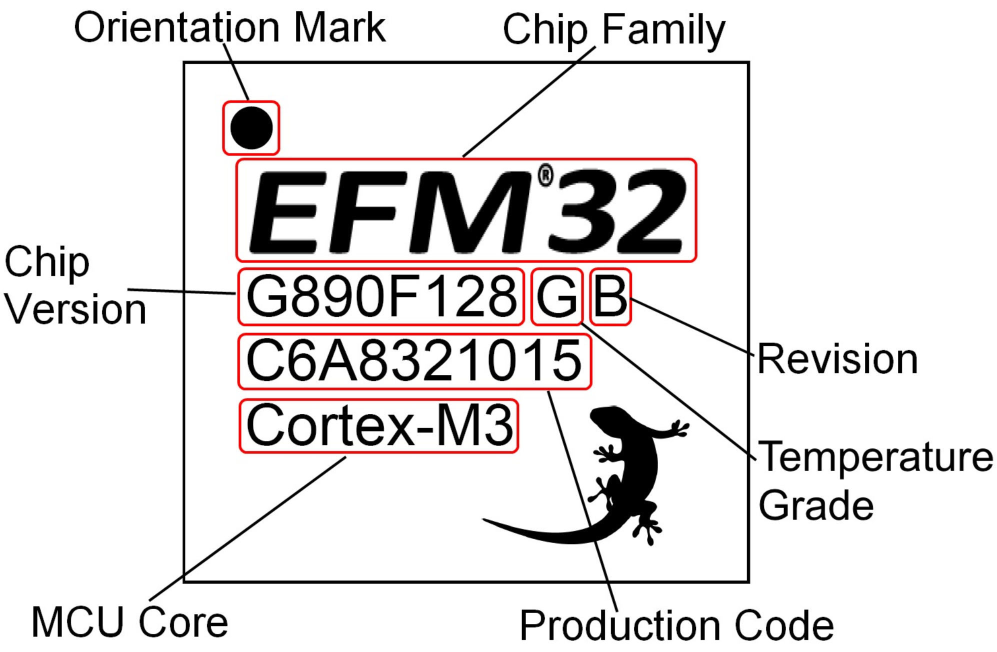

Figure 7.5. Example Chip Marking (Top View)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	—	—
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	—	0.20	θ1	0°	—	—
C1	0.09	—	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1	10.0 BSC						
e	0.50 BSC						
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

8.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

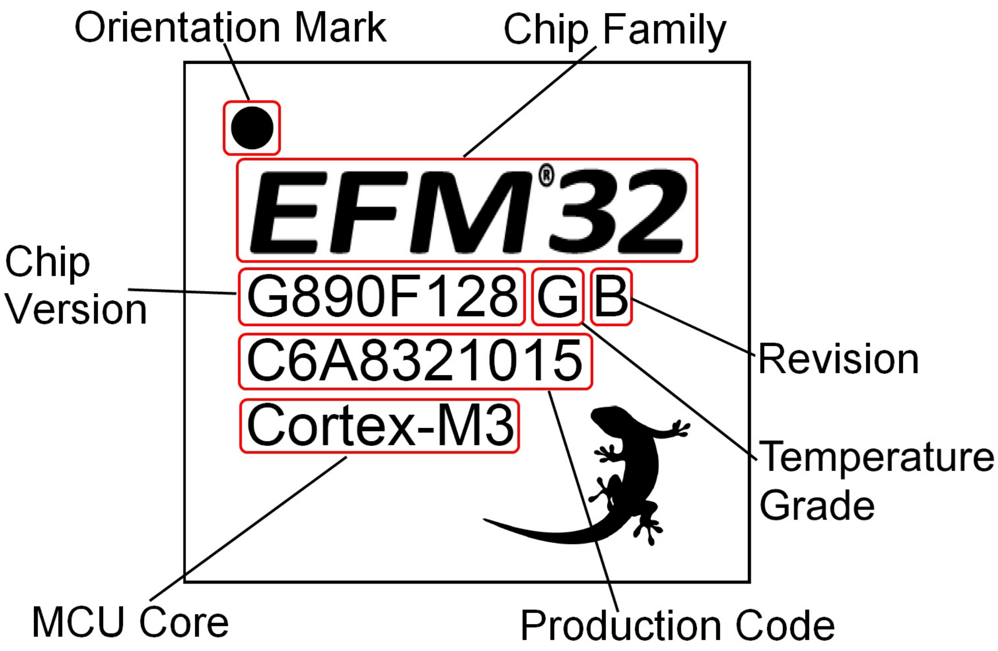

Figure 8.5. Example Chip Marking (Top View)

10.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

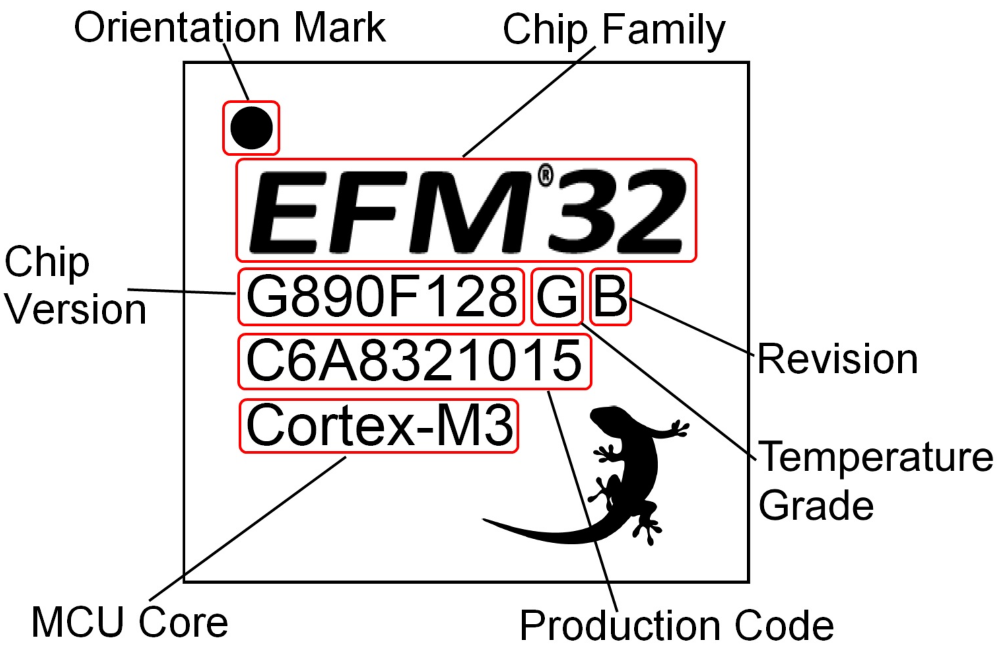

Figure 10.5. Example Chip Marking (Top View)

13.9 Revision 1.40

February 27th, 2012

Updated Power Management section.

Corrected operating voltage from 1.8 V to 1.85 V.

Corrected $TGRAD_{ADCTH}$ parameter.

Corrected package drawing.

Updated PCB land pattern, solder mask and stencil design.

For LQFP48 devices, corrected available Pulse Counters from 3 to 2.

For LQFP48 devices, corrected available LEUARTs from 2 to 1.

For LQFP64 devices, corrected ordering codes in the ordering information table.

13.10 Revision 1.30

May 20th, 2011

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Updated LFXO load capacitance section.