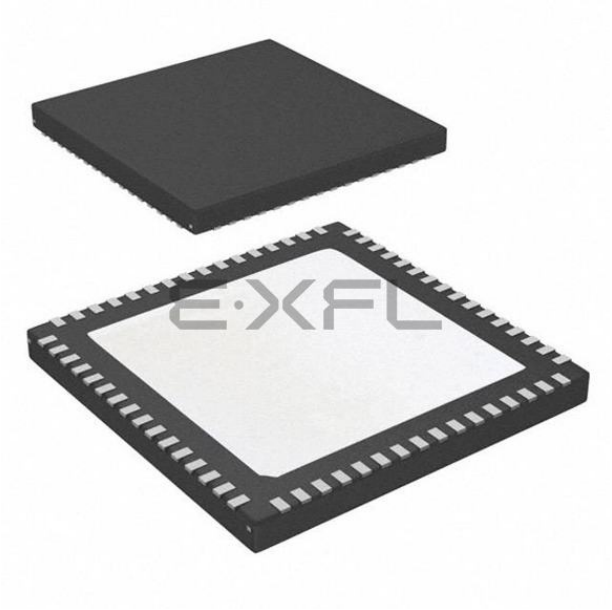
Silicon Labs - EFM32G230F64G-E-QFN64R Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g230f64g-e-qfn64r

2. Ordering Information

The following table shows the available EFM32G devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32G200F16G-E-QFN32	16	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F32G-E-QFN32	32	8	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G200F64G-E-QFN32	64	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G210F128G-E-QFN32	128	16	32	1.98 - 3.8	-40 - 85	QFN32
EFM32G222F32G-E-QFP48	32	8	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F64G-E-QFP48	64	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G222F128G-E-QFP48	128	16	32	1.98 - 3.8	-40 - 85	TQFP48
EFM32G230F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G230F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G232F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G280F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G280F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G290F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G290F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G840F32G-E-QFN64	32	8	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F64G-E-QFN64	64	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G840F128G-E-QFN64	128	16	32	1.98 - 3.8	-40 - 85	QFN64
EFM32G842F32G-E-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F64G-E-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G842F128G-E-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G880F32G-E-QFP100	32	8	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F64G-E-QFP100	64	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G880F128G-E-QFP100	128	16	32	1.98 - 3.8	-40 - 85	LQFP100
EFM32G890F32G-E-BGA112	32	8	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F64G-E-BGA112	64	16	32	1.98 - 3.8	-40 - 85	BGA112
EFM32G890F128G-E-BGA112	128	16	32	1.98 - 3.8	-40 - 85	BGA112

3.2.11 EFM32G890

The features of the EFM32G890 is a subset of the feature set described in the EFM32G Reference Manual. The following table describes device specific implementation of the features.

Table 3.11. EFM32G890 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_ARDY, EBI_ALE, EBI_WEn, EBI_REn, EBI_CS[3:0], EBI_AD[15:0]
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 57)

Module	Configuration	Pin Connections
LCD	Full configuration	LCD_SEG[39:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

3.3 Memory Map

The EFM32G memory map is shown in the figure below. RAM and Flash sizes are for the largest memory configuration.

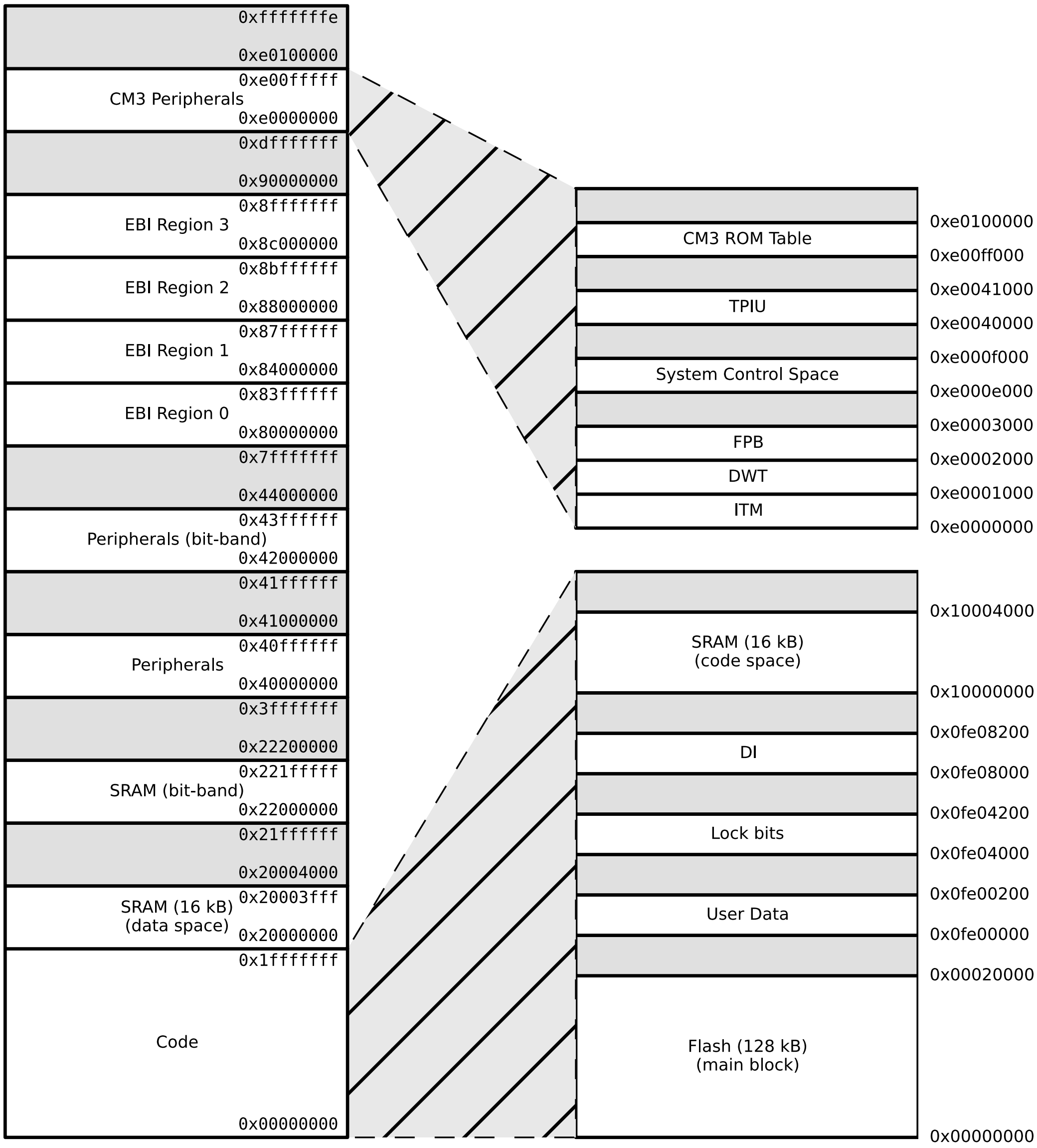


Figure 3.2. System Address Space with Core and Code Space Listing

4.4.3 EM2 Current Consumption

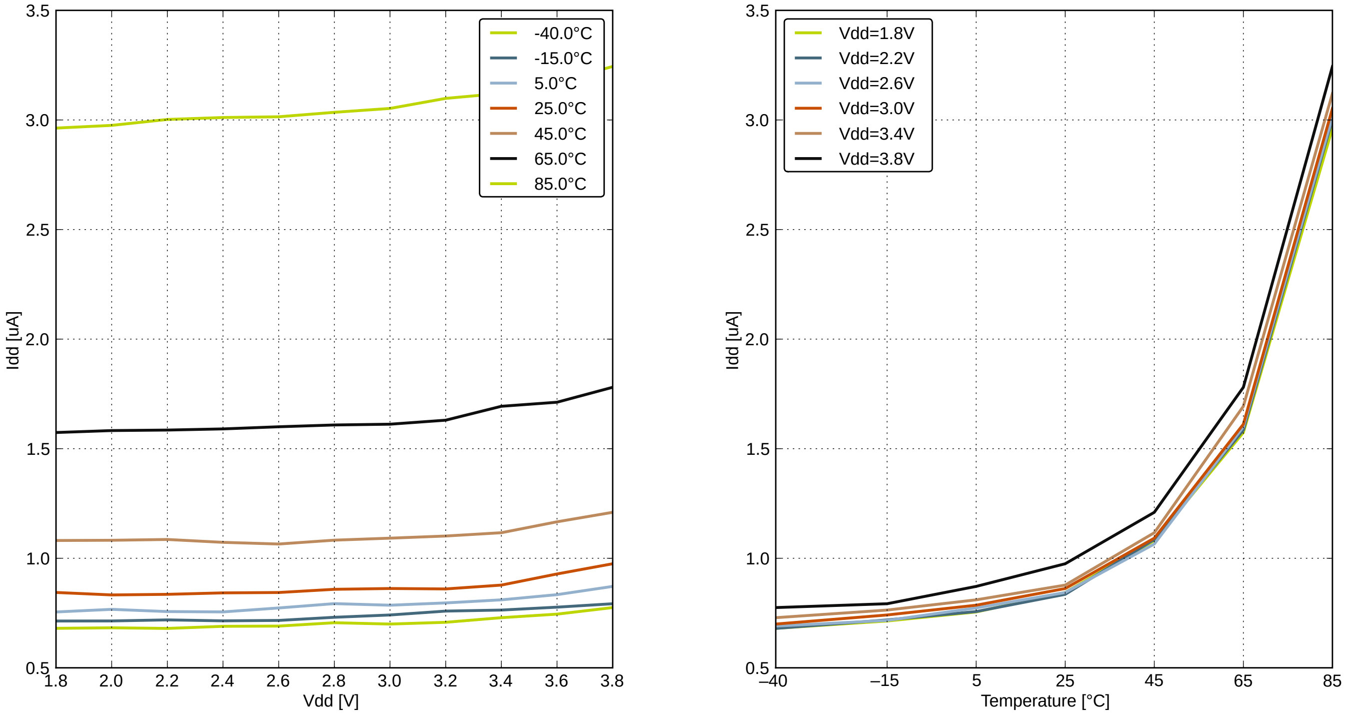


Figure 4.11. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

4.4.5 EM4 Current Consumption

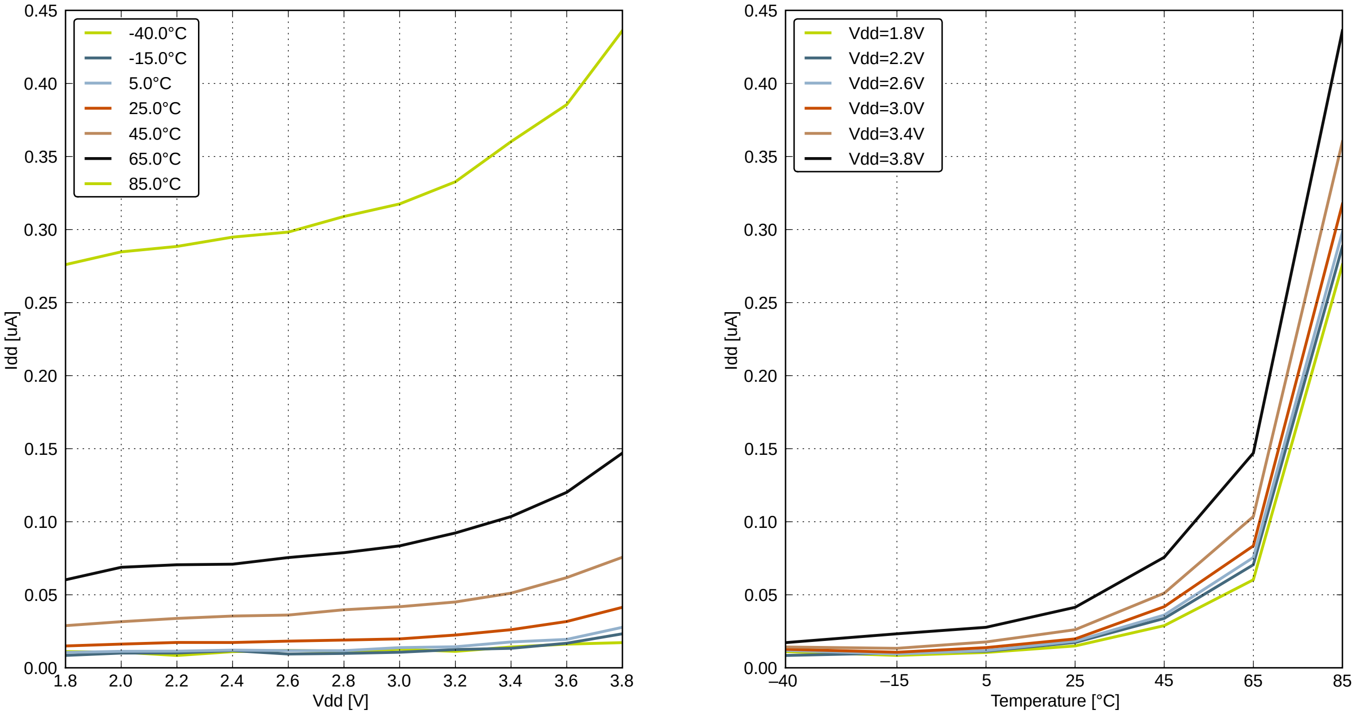


Figure 4.13. EM4 Current Consumption

4.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.4. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	µs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	µs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	µs

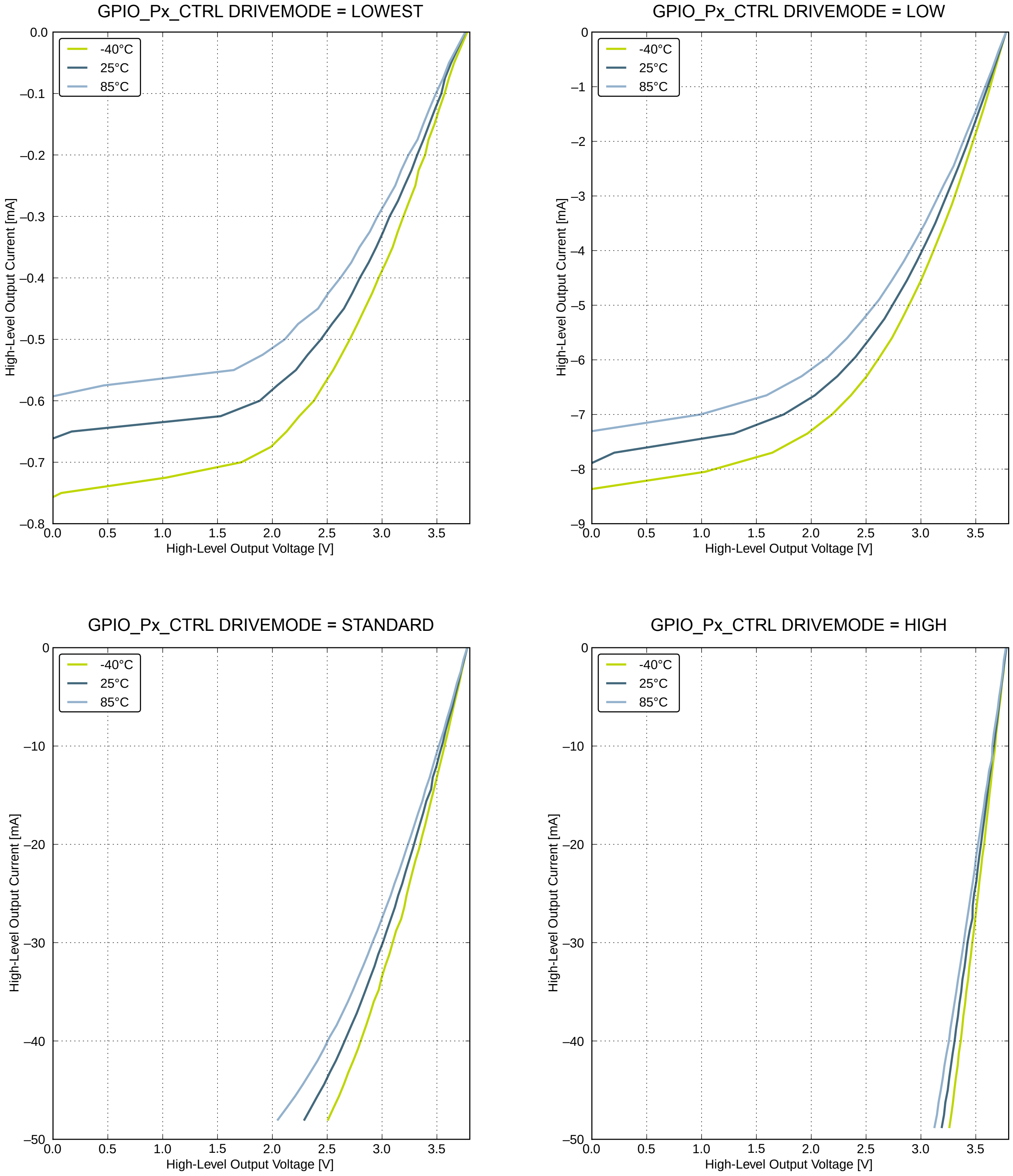


Figure 4.19. Typical High-Level Output Current, 3.8V Supply Voltage

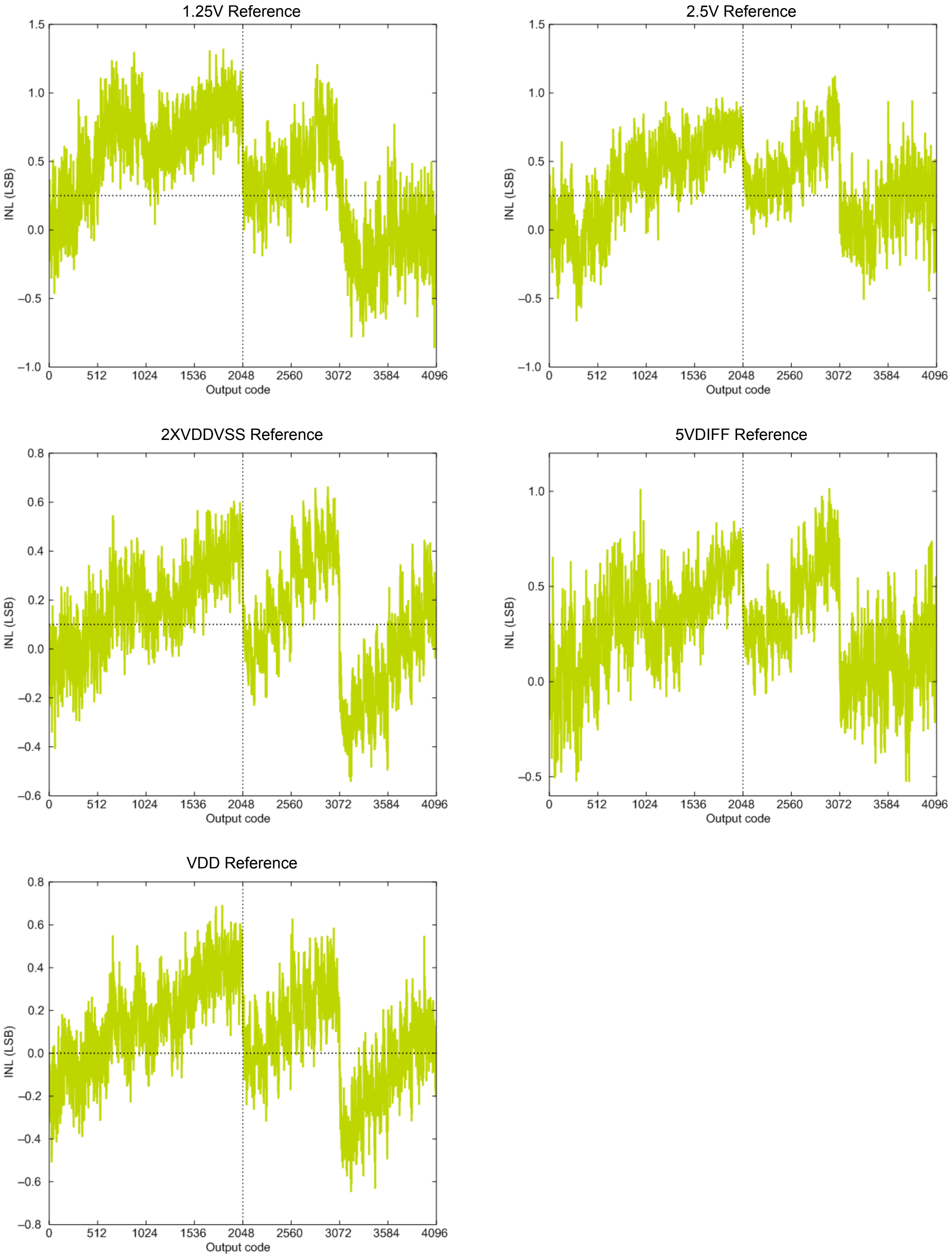
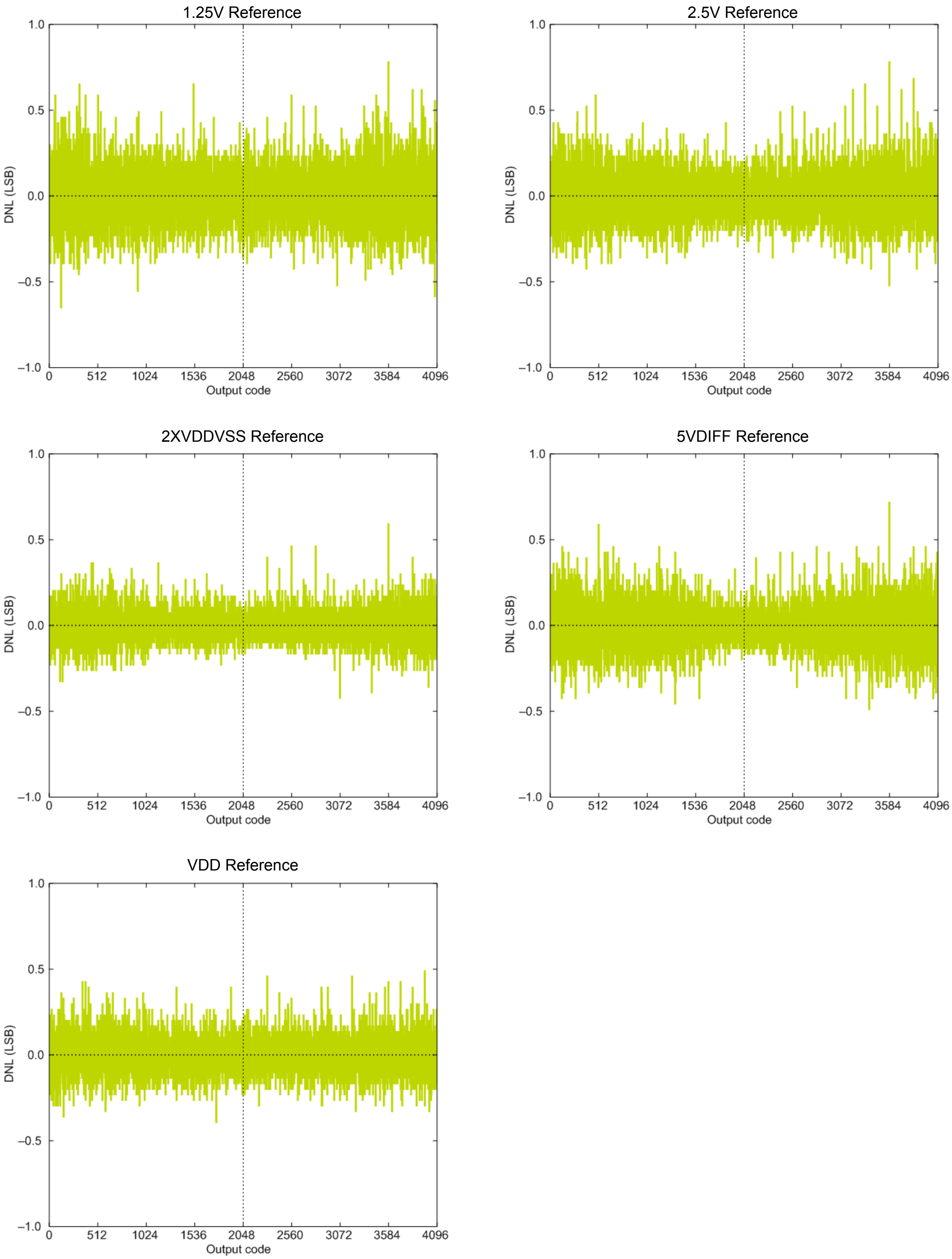


Figure 4.30. ADC Integral Linearity Error vs Code, VDD = 3V, Temp = 25°C



1.25V Reference

2.5V Reference

2XVDDVSS Reference

5VDIFF Reference

VDD Reference

Figure 4.31. ADC Differential Linearity Error vs Code, VDD = 3V, Temp = 25°C

Table 4.21. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000[1]	kHz
SCL clock low time	t_{LOW}	0.5	—	—	µs
SCL clock high time	t_{HIGH}	0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	µs

Note:

1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

4.16 Digital Peripherals

Table 4.22. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	µA/MHz
UART current	I_{UART}	UART idle current, clock enabled	—	5.63	—	µA/MHz
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	µA/MHz
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	µA/MHz
LETIMER current	$I_{LETIMER}$	LETIMER idle current, clock enabled	—	150	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
LCD current	I_{LCD}	LCD idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	µA/MHz
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	µA/MHz
EBI current	I_{EBI}	EBI idle current, clock enabled	—	1.56	—	µA/MHz
PRS current	I_{PRS}	PRS idle current	—	2.81	—	µA/MHz
DMA current	I_{DMA}	Clock enable	—	8.12	—	µA/MHz

Note: Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" forguidelines on designing Printed Circuit Boards (PCB's) for the EFM32G.

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
38	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
39	PF2				ACMP1_O #0 DBG_SWO #0
40	PF3		TIM0_CDTI0 #2		
41	PF4		TIM0_CDTI1 #2		
42	PF5		TIM0_CDTI2 #2		
43	IOVDD_5	Digital IO power supply 5.			
44	VSS	Ground.			
45	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
46	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
47	PE12		TIM1_CC2 #1	US0_CLK #0	
48	PE13			US0_CS #0	ACMP0_O #0

Alternate	LOCATION				
Functionality	**0**	**1**	**2**	**3**	**Description**
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.24. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	PA14	PA13	PA12	—	—	—	—	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	PC15	PC14	PC13	PC12	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

5.9 EFM32G880 (LQFP100)

5.9.1 Pinout

The EFM32G880 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

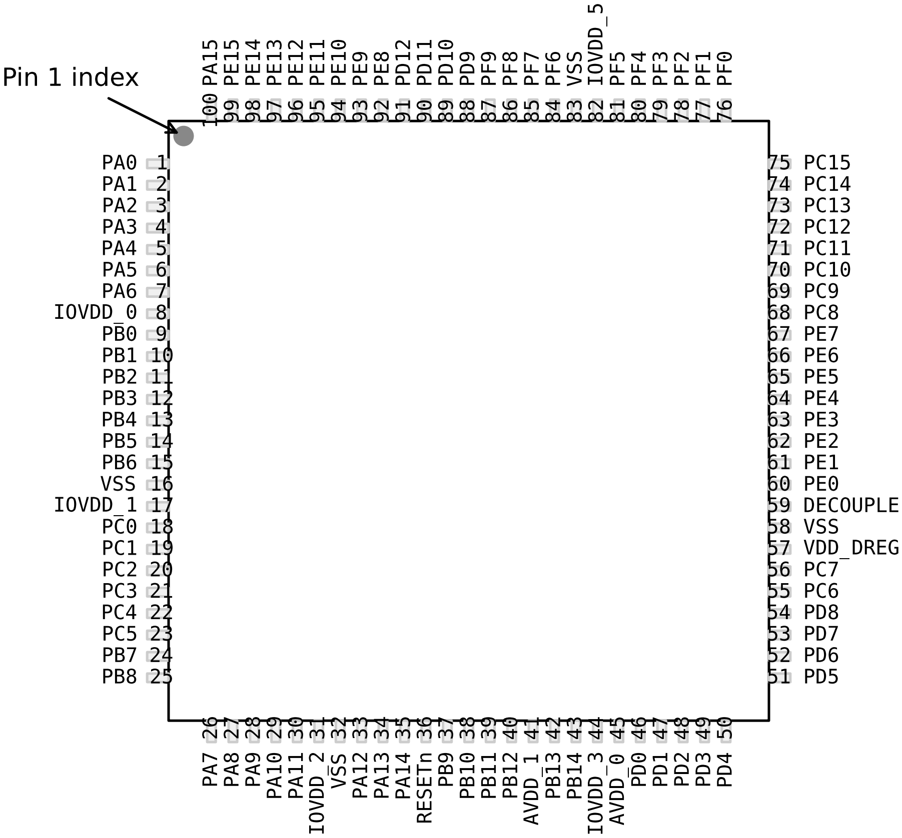


Figure 5.9. EFM32G880 Pinout (top view, not to scale)

Table 5.25. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0	LCD_SEG 13	EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1	LCD_SEG 14	EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2	LCD_SEG 15	EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0

5.10.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.29. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.

6.3 BGA112 Package Marking

In the illustration below package fields and position are shown.

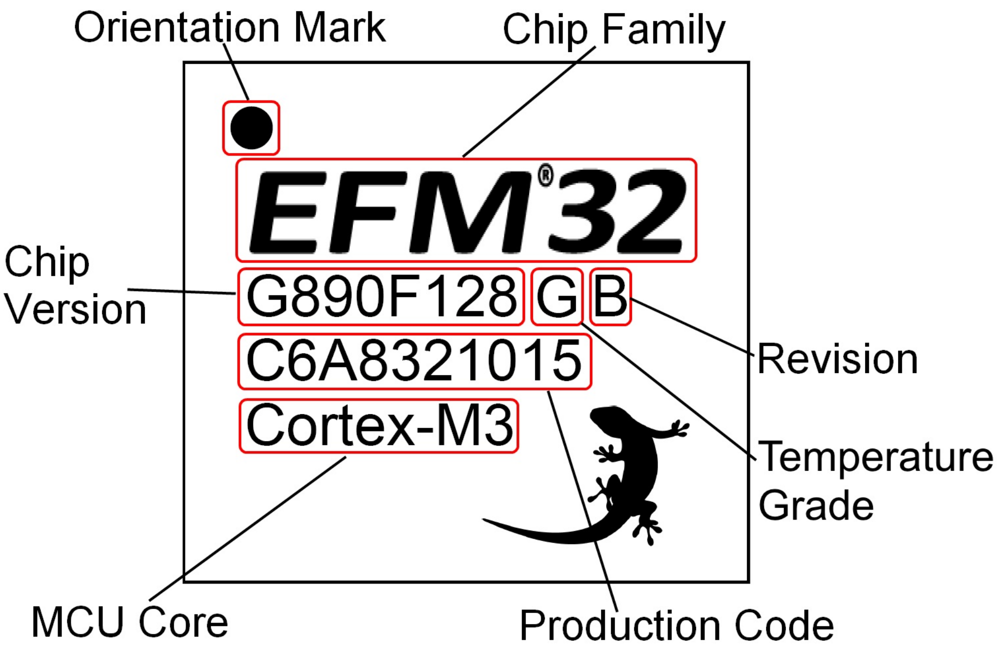


Figure 6.5. Example Chip Marking (Top View)

10. QFN64 Package Specifications

10.1 QFN64 Package Dimensions

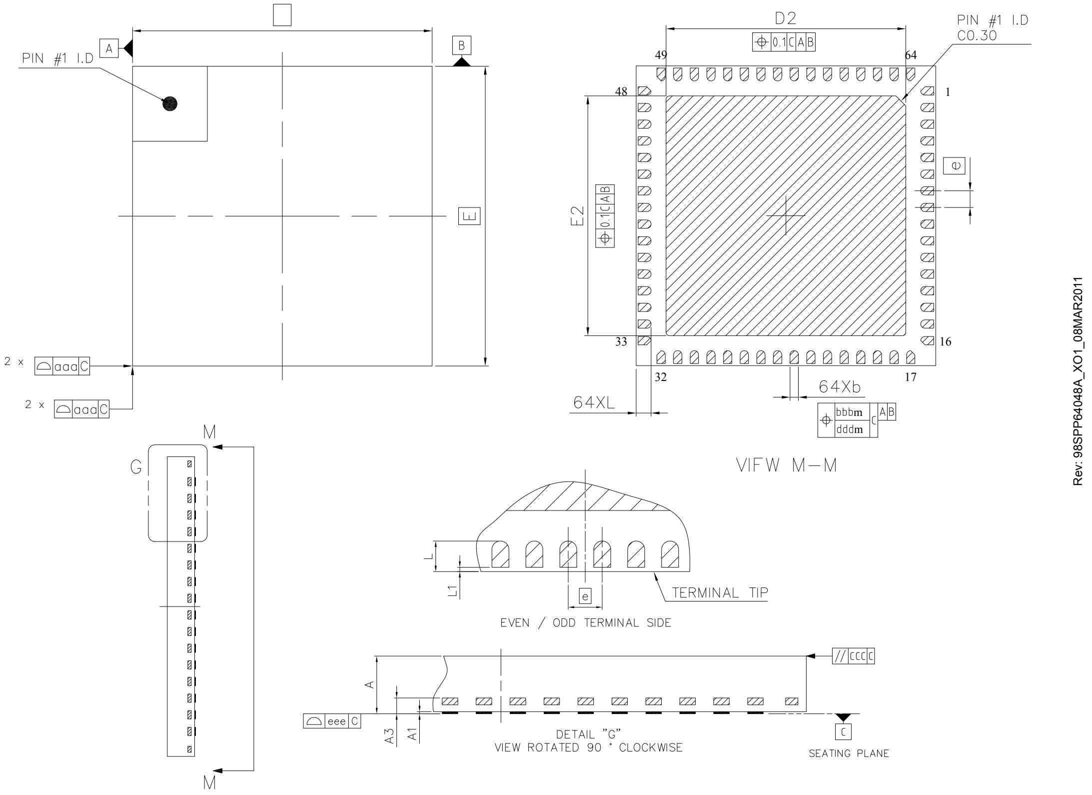


Figure 10.1. QFN64

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm fromthe terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm isacceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 10.1. QFN64 (Dimensions in mm)

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
A3		0.203 REF	
b	0.25	0.30	0.35
D		9.00 BSC	
E		9.00 BSC	
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30

Symbol	Dim. (mm)	Symbol	Dim. (mm)
d	8.90	-	-

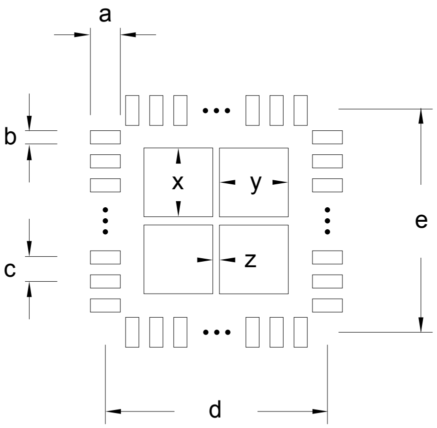


Figure 10.4. QFN64 PCB Stencil Design

Table 10.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.22	x	2.70
c	0.50	y	2.70
d	8.90	z	0.80

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

11.2 QFN32 PCB Layout

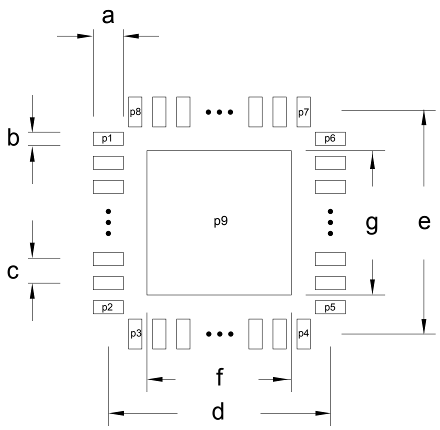


Figure 11.2. QFN32 PCB Land Pattern

Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	9	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17		
f	4.40				
g	4.40				

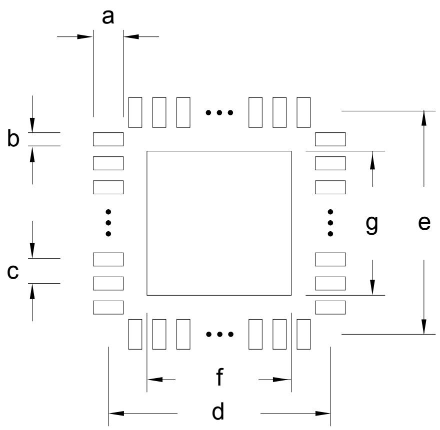


Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit