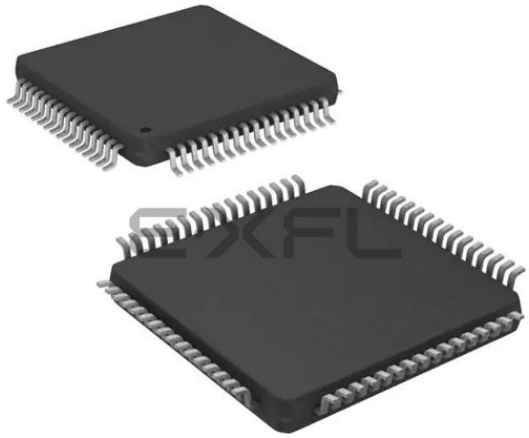
Silicon Labs - EFM32G232F128-QFP64 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32g232f128-qfp64

  - Supply Voltage Comparator
- Ultra efficient Power-on Reset and Brown-Out Detector
- 2-pin Serial Wire Debug Interface
  - 1-pin Serial Wire Viewer
- Pre-Programmed USB/UART Bootloader
- Temperature range -40 to 85 ºC
- Single power supply 1.98 to 3.8 V
- Packages
  - BGA112
  - LQFP100
  - TQFP64
  - TQFP48
  - QFN64
  - QFN32

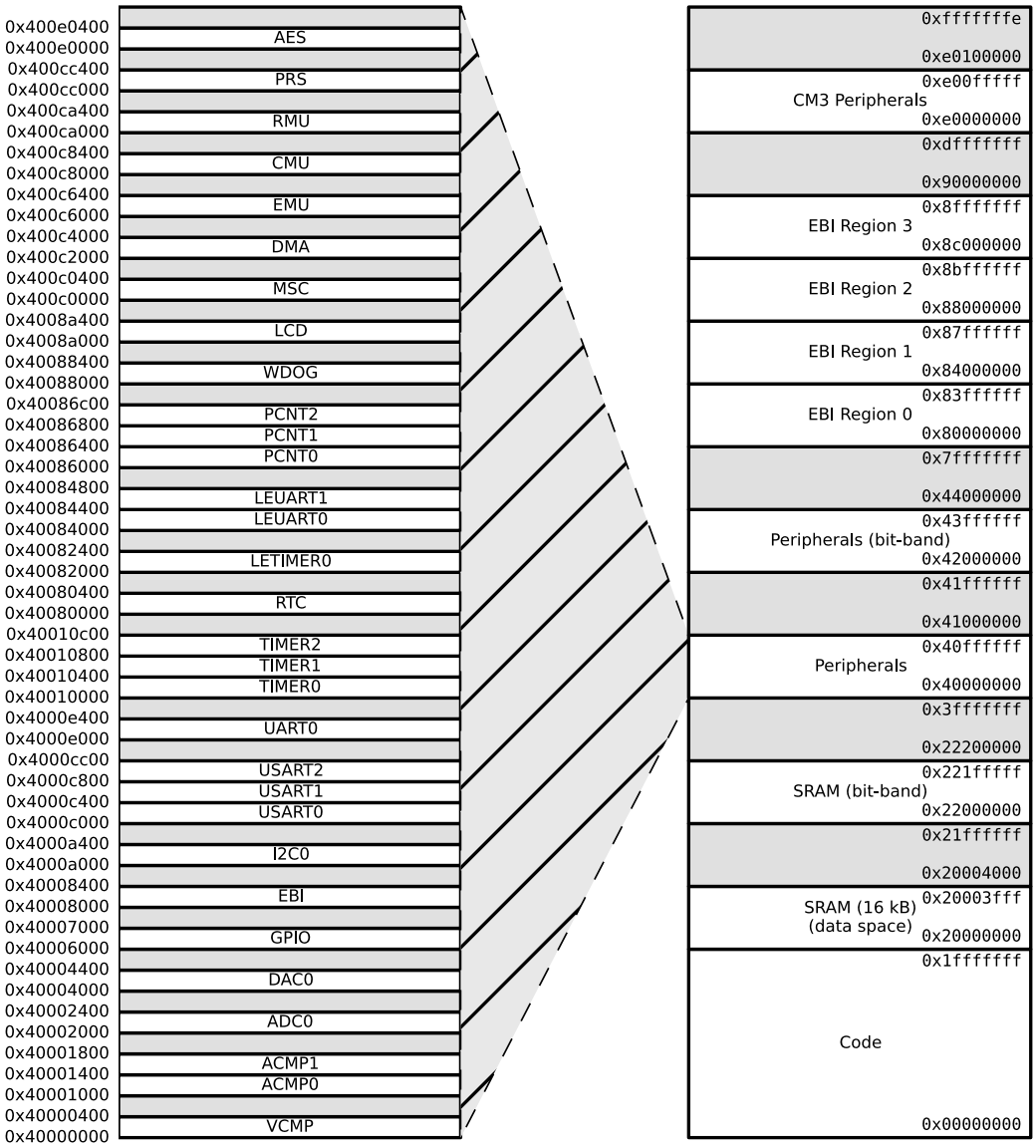

Figure 3.3. System Address Space with Peripheral Listing

4. Electrical Characteristics

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 4.2 General Operating Conditions on page 29, unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 4.2 General Operating Conditions on page 29, unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the following table may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 4.2 General Operating Conditions on page 29.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	150	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V
Current per I/O pin (sink)	I_{IOMAX_SINK}		—	—	100	mA
Current per I/O pin (source)	I_{IOMAX_SOURCE}		—	—	-100	mA

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}	-40	—	85	°C
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V
Internal APB clock frequency	f_{APB}	—	—	32	MHz
Internal AHB clock frequency	f_{AHB}	—	—	32	MHz

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single-ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
Input range of external reference voltage, single-ended and differential	$V_{ADCREFIN}$		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{ADCREFIN\_CH7}$	See $V_{ADCREFIN}$	0	—	V_{DD} - 1.1	V
Input range of external positive reference voltage on channel 6	$V_{ADCREFIN\_CH6}$	See $V_{ADCREFIN}$	0.625	—	V_{DD}	V
Common mode input range	$V_{ADCCMIN}$		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	$CMRR_{ADC}$		—	65	—	dB
Average active current	I_{ADC}	1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	735[1]	—	µA
		1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	760[1]	—	µA
		500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	346[1]	—	µA
		500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	354[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	52[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	50[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	54[1]	—	µA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		1	—	—	MΩ
Input RC filter resistance	$R_{ADCFILT}$		—	10	—	kΩ
Input RC filter/decoupling capacitance	$C_{ADCFILT}$		—	250	—	fF
Input bias current	$I_{ADCBIASIN}$	VSS < VIN < VDD	-40	—	40	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)	SNR_{ADC}	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	59	—	dB
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	67	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK =13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK= 13 MHz, BIASPROG =0xF4B	63	69	—	dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	70	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	62	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	67	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise And Distortion Ratio (SINAD)	$SINAD_{ADC}$	200 kSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	62	68	—	dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	69	—	dB

4.11 Digital Analog Converter (DAC)

Table 4.15. DAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage range	V_{DACOUT}	VDD voltage reference, single-ended	0	—	V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$	—	V_{DD}	V
Output common mode voltage range	V_{DACCM}		0	—	V_{DD}	V
Average active current	I_{DAC}	500 kSamples/s, 12 bit, internal 1.25 V reference, Continuous Mode	—	400[1]	650[1]	µA
		100 kSamples/s, 12 bit, internal 1.25 V reference, Sample/Hold Mode	—	200[1]	250[1]	µA
		1 kSamples/s 12 bit, internal 1.25 V reference, Sample/Off Mode	—	17[1]	25[1]	µA
Sample rate	SR_{DAC}		—	—	500	ksamples/s
DAC clock frequency	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode	—	—	250	kHz
		Sample/Off Mode	—	—	250	kHz
Clock cycles per conversion	$CYC_{DACCONV}$		—	2	—	cycles
Conversion time	$t_{DACCONV}$		2	—	—	µs
Settling time	$t_{DACSETTLE}$		—	5	—	µs
Signal-to-Noise Ratio (SNR)	SNR_{DAC}	500 kSamples/s, 12 bit, single-ended, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, single-ended, internal 2.5 V reference	—	59	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	59	—	dB

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LETIM0_OUT1	PD7		PF1		Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14			LEUART0 Receive input.
LEU0_TX	PD4	PB13			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
TIM0_CC0	PA0	PA0			Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13		PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14		PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15		PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12				USART0 clock input / output.
US0_CS	PE13				USART0 chip select input / output.
US0_RX	PE11				USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10				USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7				USART1 clock input / output.
US1_CS	PB8				USART1 chip select input / output.
US1_RX	PC1				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

TQFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
7	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
8	PC2	ACMP0_CH2			
9	PC3	ACMP0_CH3			
10	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0		
11	PB7	LFXTAL_P		US1_CLK #0	
12	PB8	LFXTAL_N		US1_CS #0	
13	PA8		TIM2_CC0 #0		
14	PA9		TIM2_CC1 #0		
15	PA10		TIM2_CC2 #0		
16	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		LEU0_TX #1	
21	PB14	HFXTAL_N		LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
27	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
30	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
31	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
32	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
33	PC11	ACMP1_CH3		US0_TX #2	
34	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
35	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
36	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
37	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1

5.3 EFM32G230 (QFN64)

5.3.1 Pinout

The EFM32G230 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

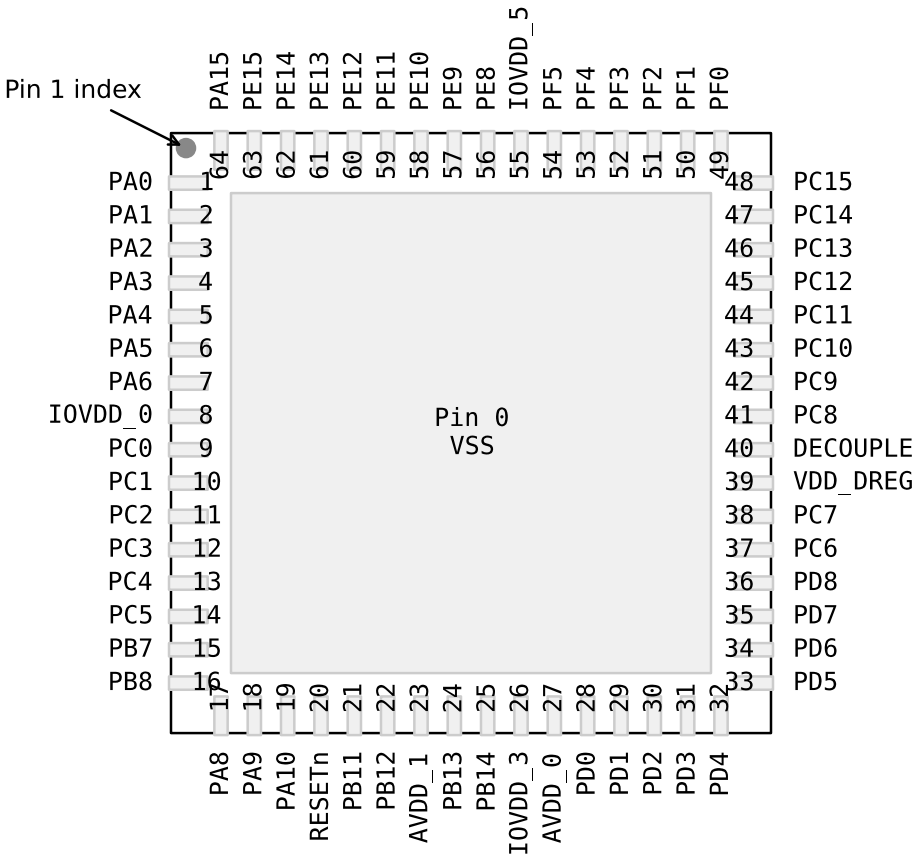

Figure 5.3. EFM32G230 Pinout (top view, not to scale)

Table 5.7. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		

Alternate	LOCATION				
Functionality	0	1	2	3	Description
US0_CS	PE13		PC8		USART0 chip select input / output.
US0_RX	PE11		PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MI-SO).
US0_TX	PE10		PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MI-SO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4				USART2 clock input / output.
US2_CS	PC5				USART2 chip select input / output.
US2_RX	PC3				USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MI-SO).
US2_TX	PC2				USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32G2322 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	—	—	—	—	PA10	PA9	PA8	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	—	—	—	—	—	—	—
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	—	—	—	—	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
63	PE3					ACMP1_O #1
64	PE4				US0_CS #1	
65	PE5				US0_CLK #1	
66	PE6				US0_RX #1	
67	PE7				US0_TX #1	
68	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
69	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
70	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
71	PC11	ACMP1_CH3			US0_TX #2	
72	PC12	ACMP1_CH4				CMU_CLK0 #1
73	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
74	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
75	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
76	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1
77	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
78	PF2		EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
79	PF3		EBI_ALE #0	TIM0_CDTI0 #2		
80	PF4		EBI_WEn #0	TIM0_CDTI1 #2		
81	PF5		EBI_REn #0	TIM0_CDTI2 #2		
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground.				
84	PF6			TIM0_CC0 #2	U0_TX #0	
85	PF7			TIM0_CC1 #2	U0_RX #0	
86	PF8			TIM0_CC2 #2		
87	PF9					
88	PD9		EBI_CS0 #0			
89	PD10		EBI_CS1 #0			
90	PD11		EBI_CS2 #0			
91	PD12		EBI_CS3 #0			

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
K5	PA11					
K6	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
K7	AVSS_1	Analog ground 1.				
K8	AVDD_2	Analog power supply 2.				
K9	AVDD_1	Analog power supply 1.				
K10	AVSS_0	Analog ground 0.				
K11	PD1	ADC0_CH 1		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
L1	PB8	LFXTAL_N			US1_CS #0	
L2	PC5	ACMP0_C H5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
L3	PA14			TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OU T0		LETIM0_OUT0 #1		
L6	PB12	DAC0_OU T1		LETIM0_OUT1 #1		
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFXTAL_ P			LEU0_TX #1	
L9	PB14	HFXTAL_ N			LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH 0		PCNT2_S0IN #0	US1_TX #1	

TQFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2	LCD_SEG0			ACMP1_O #0 DBG_SWO #0
52	PF3	LCD_SEG1	TIM0_CDTI0 #2		
53	PF4	LCD_SEG2	TIM0_CDTI1 #2		
54	PF5	LCD_SEG3	TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8	LCD_SEG4	PCNT2_S0IN #1		
58	PE9	LCD_SEG5	PCNT2_S1IN #1		
59	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	BOOT_RX
61	PE12	LCD_SEG8	TIM1_CC2 #1	US0_CLK #0	
62	PE13	LCD_SEG9		US0_CS #0	ACMP0_O #0
63	PE14	LCD_SEG10		LEU0_TX #2	
64	PE15	LCD_SEG11		LEU0_RX #2	

5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.23. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LCD_SEG30	PD11				LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12				LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0				LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1				LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2				LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7				LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8				LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9				LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10				LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11				LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.

		SYMBOL	MIN	NOM	MAX
	x	D		16 BSC	
	y	E		16 BSC	
body size	x	D1		14 BSC	
	y	E1		14 BSC	
lead pitch		e		0.5 BSC	
		L	0.45	0.6	0.75
footprint		L1		1 REF	
		θ	0°	3.5°	7°
		θ1	0°	—	—
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	—	—
		R1	0.08	—	0.2
		S	0.2	—	—
package edge tolerance		aaa		0.2	
lead edge tolerance		bbb		0.2	
coplanarity		ccc		0.08	
lead offset		ddd		0.08	
mold flatness		eee		0.05	

The LQFP100 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

9.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

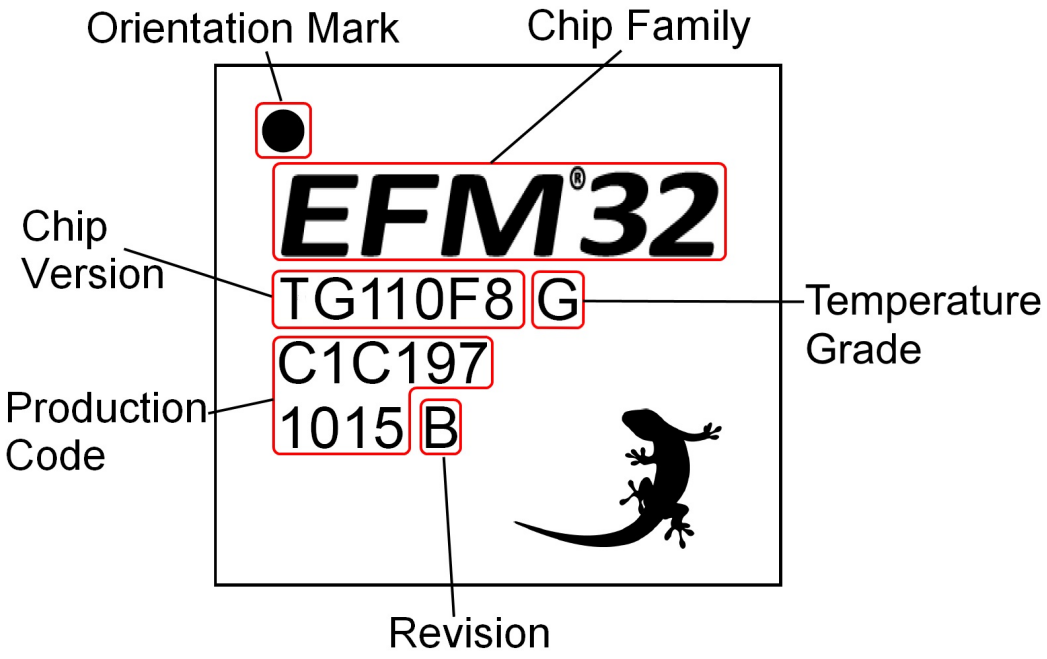

Figure 9.5. Example Chip Marking (Top View)

11.2 QFN32 PCB Layout

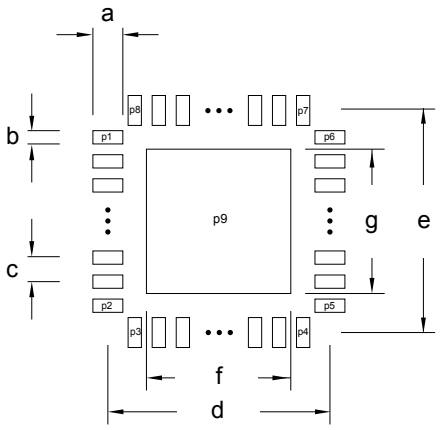

Figure 11.2. QFN32 PCB Land Pattern

Table 11.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
c	0.65	P3	9	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17		
f	4.40				
g	4.40				

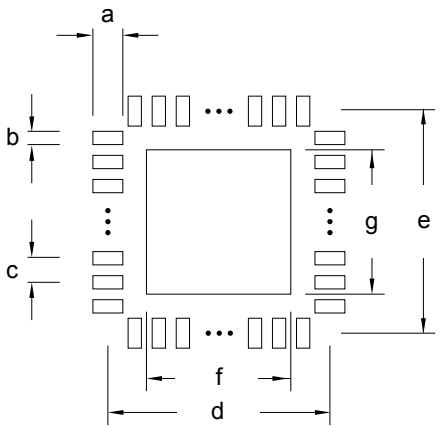

Figure 11.3. QFN32 PCB Solder Mask

Table 11.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.92
b	0.47
c	0.65

13.5 Revision 1.71

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.

13.6 Revision 1.70

September 30th, 2013

For devices with an I2C, added I2C characterization data.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

For devices with an ADC, corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

For QFN64 devices, updated the Max V_{ESDCDM} value to 750 V.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

13.7 Revision 1.60

June 28th, 2013

For BGA devices, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

13.8 Revision 1.50

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

For BGA devices, corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.